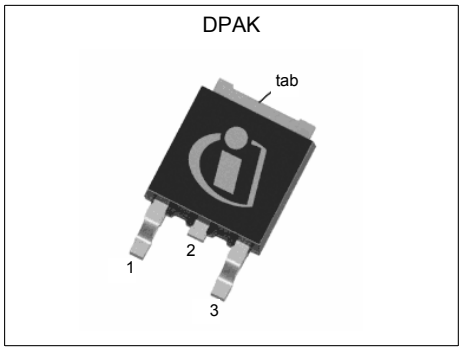
MOSFET

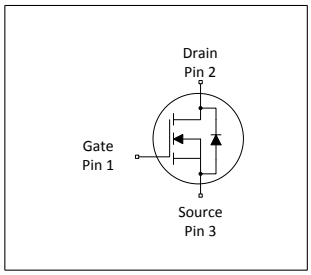
650V CoolMOS™ CFDA Power Transistor



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFDA series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter, and cooler.

Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Easy to use/drive
- Qualified according to AEC Q101
- Green package (RoHS compliant), Pb-free plating, halogen free for mold compound



Applications

650V CoolMOS™ CFDA is designed for switching applications.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	650	V
RDS(on),max	0.66	Ω
Qg,typ	20	nC
ID,pulse	17	A
Eoss @ 400V	1.8	µJ
Body diode di/dt	900	A/µs
Qrr	0.2	µC
trr	65	ns
Irrm	4.5	A

Type / Ordering Code	Package	Marking	Related Links
IPD65R660CFDA	PG-TO 252	65F660A	-

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D			6	A	T_C = 25°C
				3.8		T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$			17	A	T_C = 25°C
Avalanche energy, single pulse	E_{AS}			115	mJ	I_D = 1.2A, V_{DD} = 50V (see table 10)
Avalanche energy, repetitive	E_{AR}			0.21	mJ	I_D = 1.2A, V_{DD} = 50V
Avalanche current, repetitive	I_{AR}			1.2	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	V_{DS} = 0 ... 400V
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC (f > 1 Hz)
Power dissipation (SMD) DPAK	P_{tot}			62.5	W	T_C = 25°C
Operating and storage temperature	T_j, T_{stg}	-40		150	°C	
Continuous diode forward current	I_S			6	A	T_C = 25°C
Diode pulse current	$I_{S,pulse}$			17	A	T_C = 25°C
Reverse diode dv/dt[3]	dv/dt			50	V/ns	V_{DS} = 0 ... 400V, $I_{SD} \le I_D$, T_j = 25°C (see table 8)
Maximum diode commutation speed	di_f/dt			900	A/µs	

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j\,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			2	K/W	
Thermal resistance, junction - ambient[1)]	R_{thJA}			62	K/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

[1)] Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

3 Electrical characteristics

at T_j = 25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage[1]	$V_{(BR)DSS}$	650			V	V_{GS} = 0V, I_D = 1mA
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	V_{DS} = V_{GS}, I_D = 0.2mA
Zero gate voltage drain current	I_{DSS}			1	µA	V_{DS} = 650V, V_{GS} = 0V, T_j = 25°C
			100			V_{DS} = 650V, V_{GS} = 0V, T_j = 150°C
Gate-source leakage current	I_{GSS}			100	nA	V_{GS} = 20V, V_{DS} = 0V
Drain-source on-state resistance	$R_{DS(on)}$		0.594	0.66	Ω	V_{GS} = 10V, I_D = 3.2A, T_j = 25°C
			1.54			V_{GS} = 10V, I_D = 3.2A, T_j = 150°C
Gate resistance	R_G		6.5		Ω	f = 1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		543		pF	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz
Output capacitance	C_{oss}		32		pF	
Effective output capacitance, energy related[2]	$C_{o(er)}$		24		pF	V_{GS} = 0V, V_{DS} = 0 ... 400V
Effective output capacitance, time related[3]	$C_{o(tr)}$		97		pF	I_D = constant, V_{GS} = 0V, V_{DS} = 0 ... 400V
Turn-on delay time	$t_{d(on)}$		9		ns	V_{DD} = 400V, V_{GS} = 13V, I_D = 3.2A, R_G = 6.8Ω (see table 9)
Rise time	t_r		8		ns	
Turn-off delay time	$t_{d(off)}$		40		ns	
Fall time	t_f		10		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		3.5		nC	V_{DD} = 480V, I_D = 3.2A, V_{GS} = 0 to 10V
Gate to drain charge	Q_{gd}		11		nC	
Gate charge total	Q_g		20		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

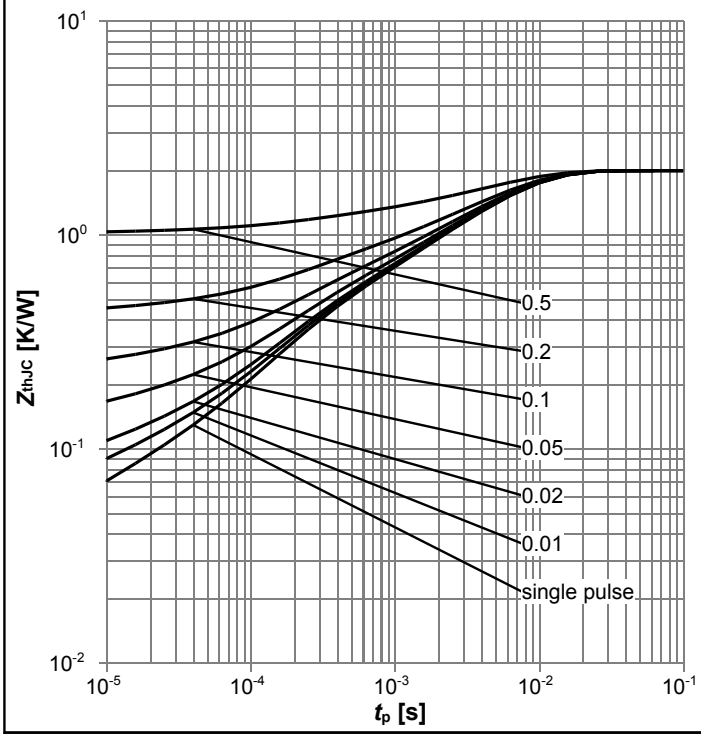
[1] For applications with applied blocking voltage > 65% of the specified blocking voltage, we recommend to evaluate the impact of the cosmic radiation effect in early design phase. For assessment please contact local Infineon sales office.
[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	V_{GS} = 0V, I_F = 3.2A, T_j = 25°C
Reverse recovery time	t_{rr}		65		ns	V_R = 400V, I_F = 3.2A, di_F/dt = 100A/µs (see table 8)
Reverse recovery charge	Q_{rr}		0.2		µC	
Peak reverse recovery current	I_{rrm}		4.5		A	

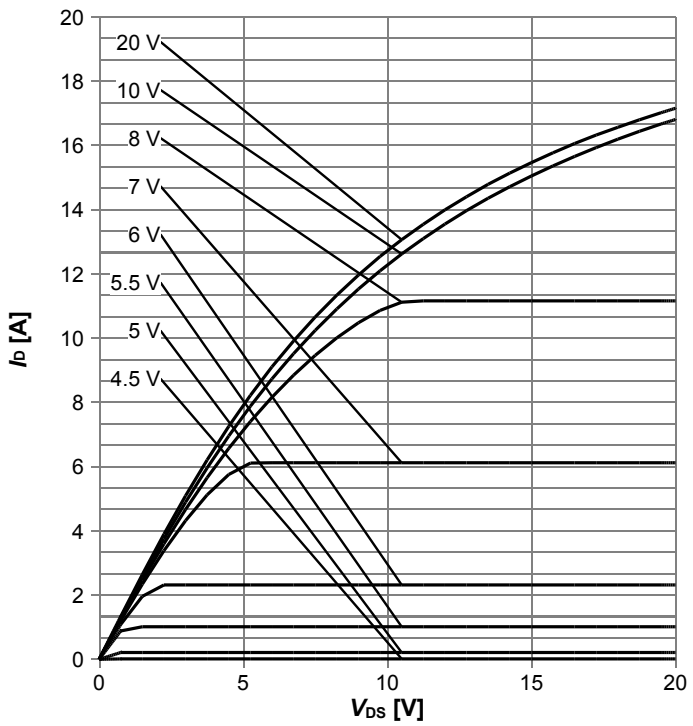
4 Electrical characteristics diagrams

Max. transient thermal impedance



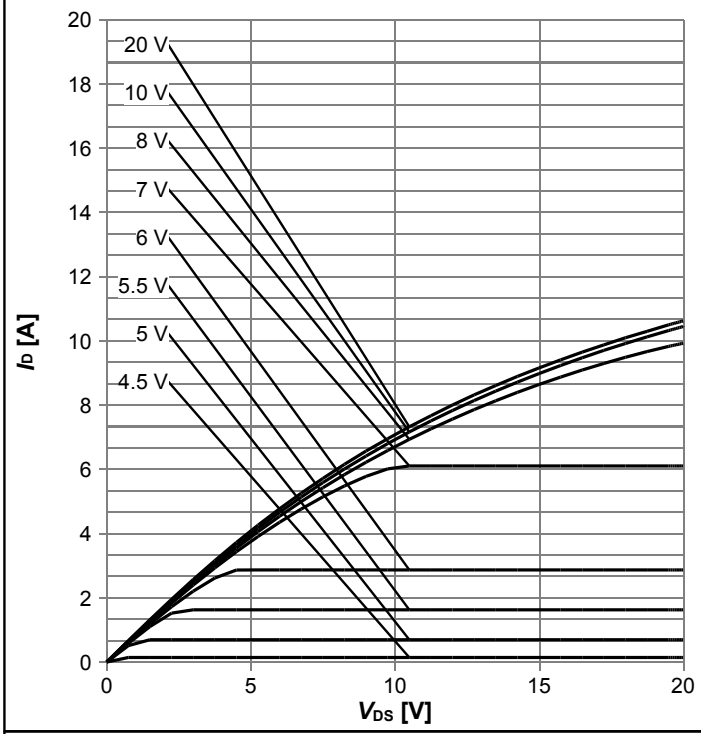
Z_{thJC} =f(t_P); parameter: D=t_p/T

Typ. output characteristics



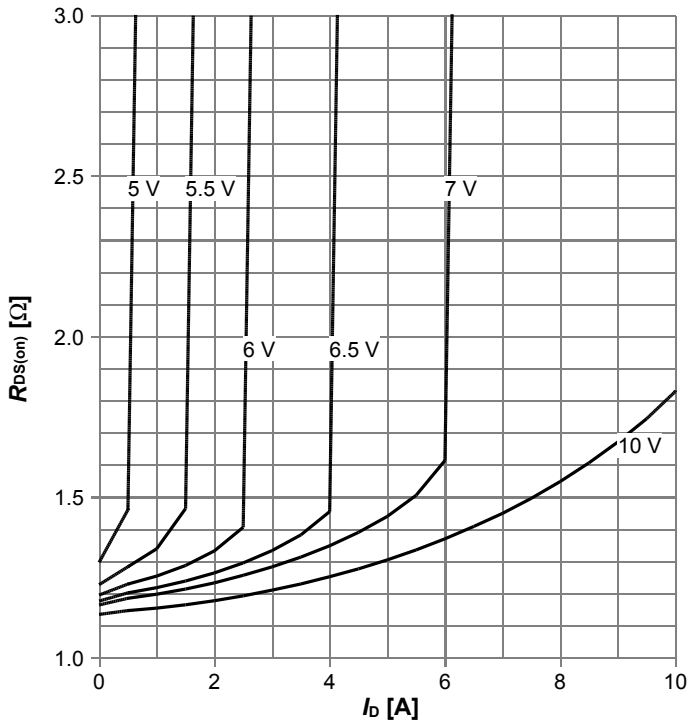
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Typ. output characteristics



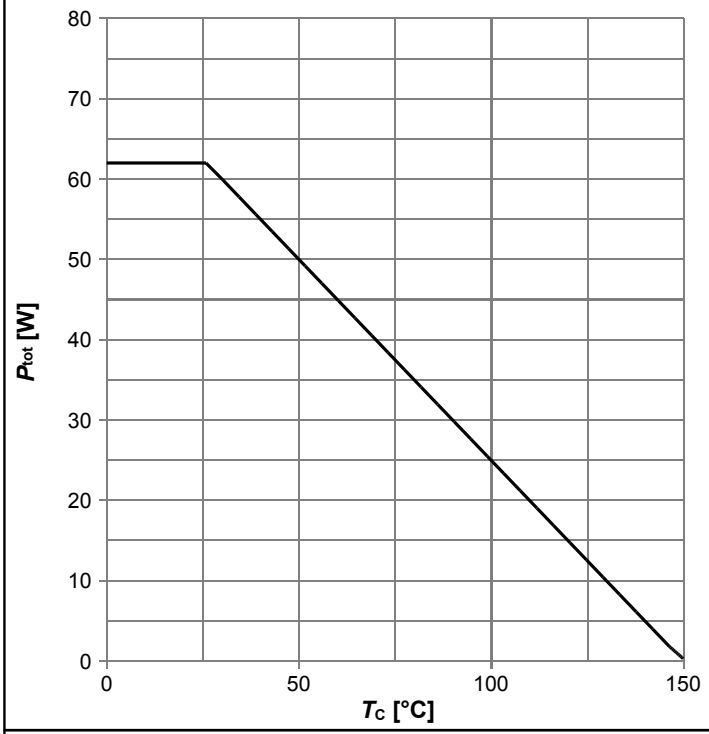
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Typ. drain-source on-state resistance



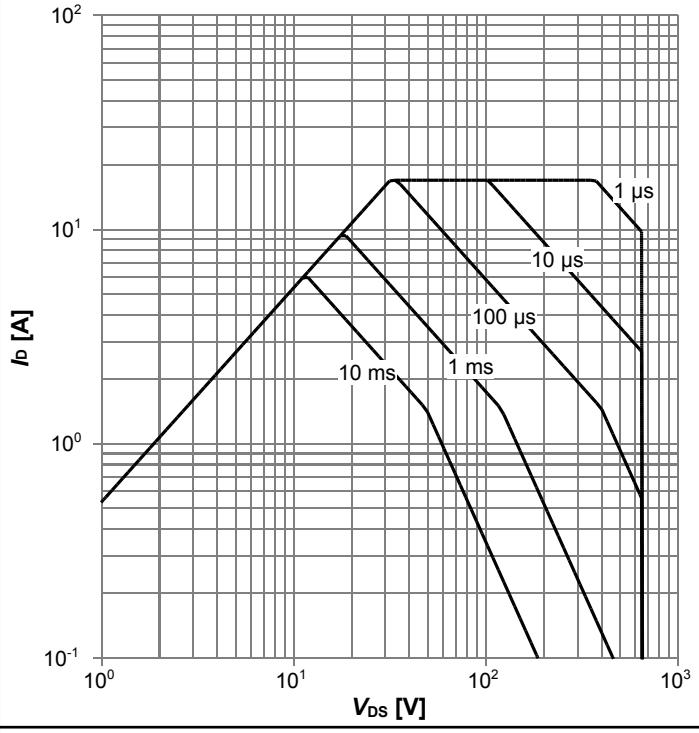
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Power dissipation



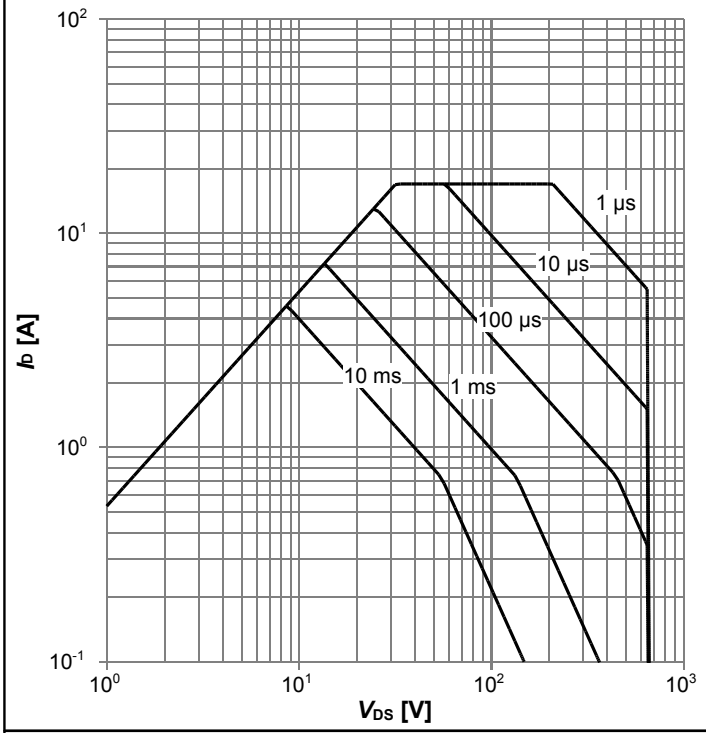
$P_{tot}=f(T_C)$

Diagram 18: Safe operating area



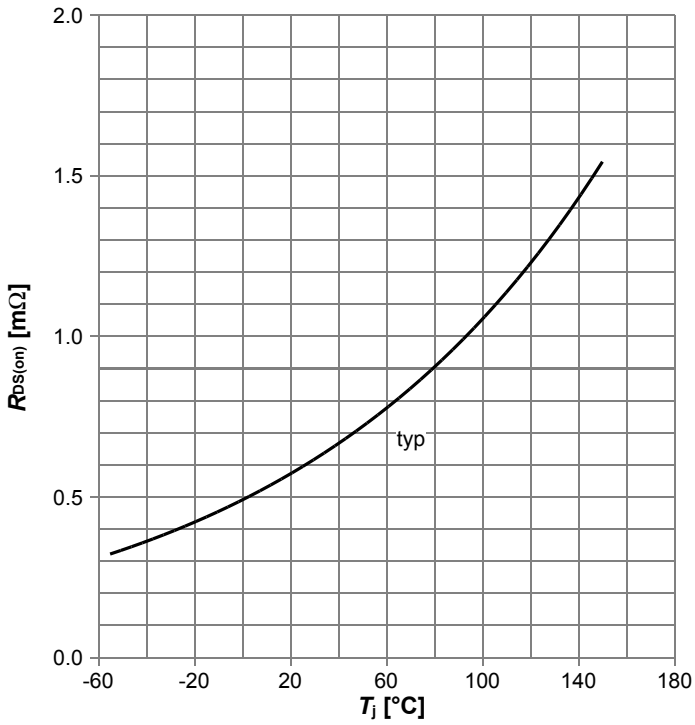
$I_D=f(V_{DS})$; T_C=25 °C; D=0; for V_{gs}>7.5V; parameter: t_p

Diagram 7: Safe operating area



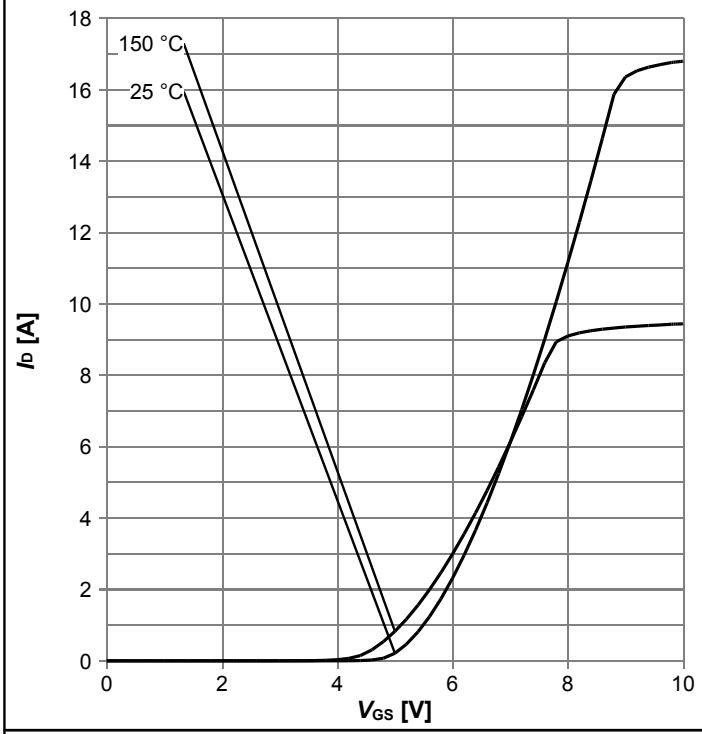
$I_D=f(V_{DS})$; T_C=80 °C; D=0; for V_{gs}>7.5V; parameter: $D=t_p/T$

Typ. drain-source on-state resistance



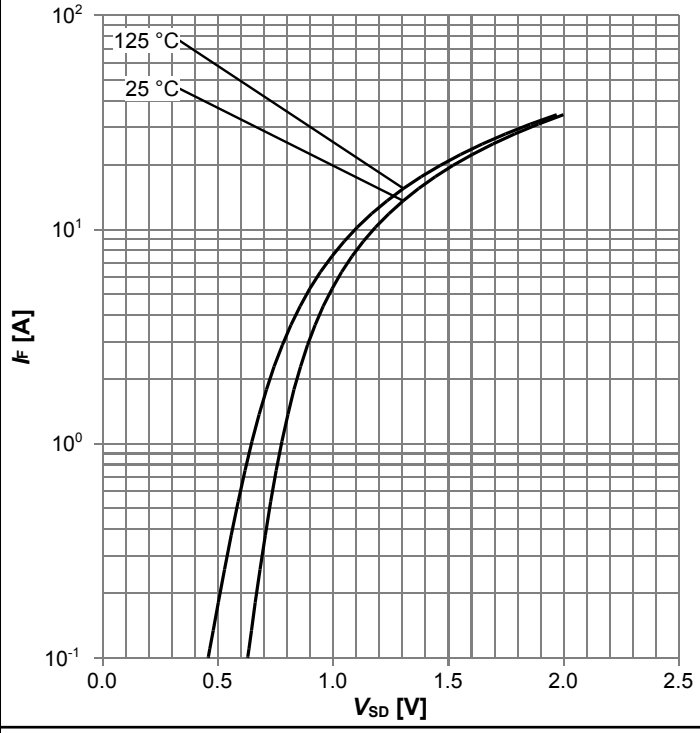
$R_{DS(on)}=f(T_j)$; I_D=3.2 A; V_{GS}=10 V

Typ. transfer characteristics



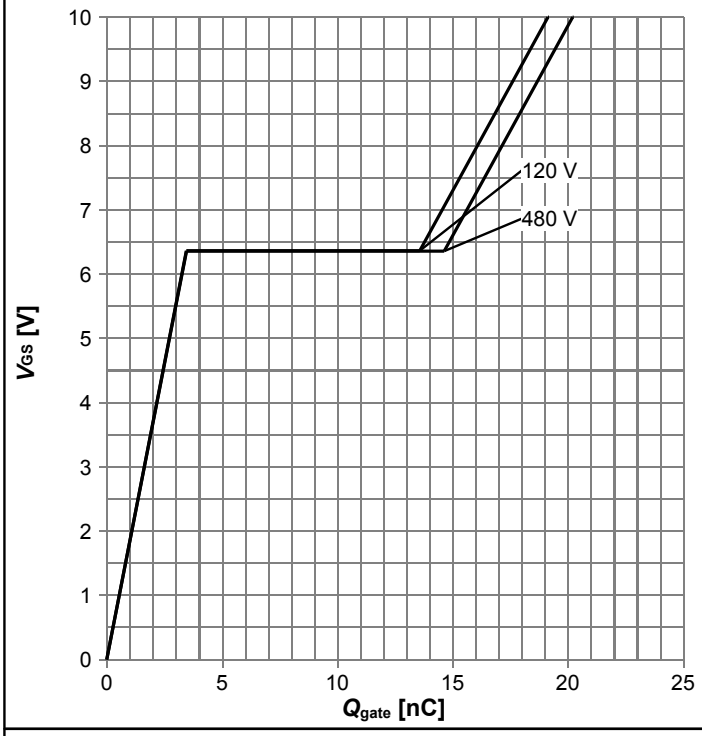
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Typ. forward characteristics of reverse diode



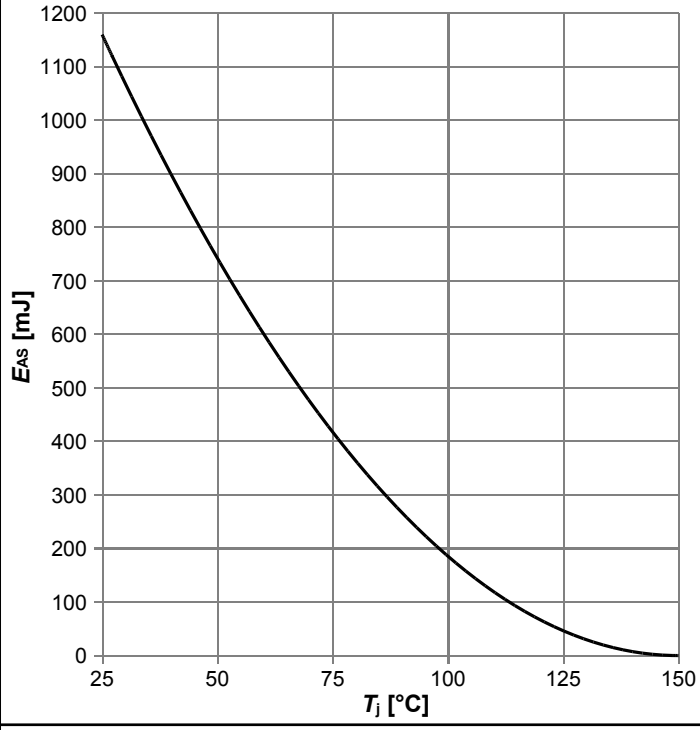
$I_F=f(V_{SD})$; parameter: T_j

Typ. gate charge



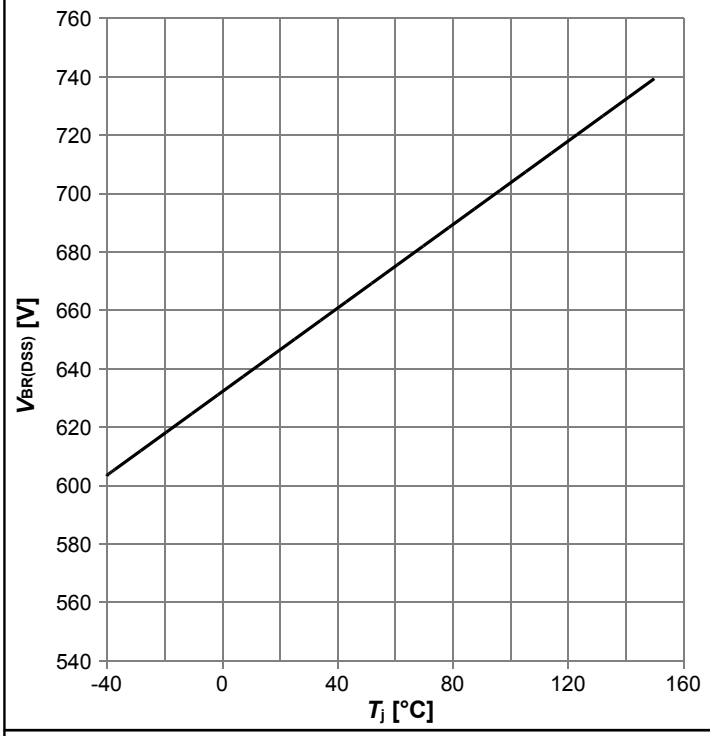
$V_{GS}=f(Q_{gate})$; I_D=19.2 A pulsed; parameter: V_{DD}

Avalanche energy



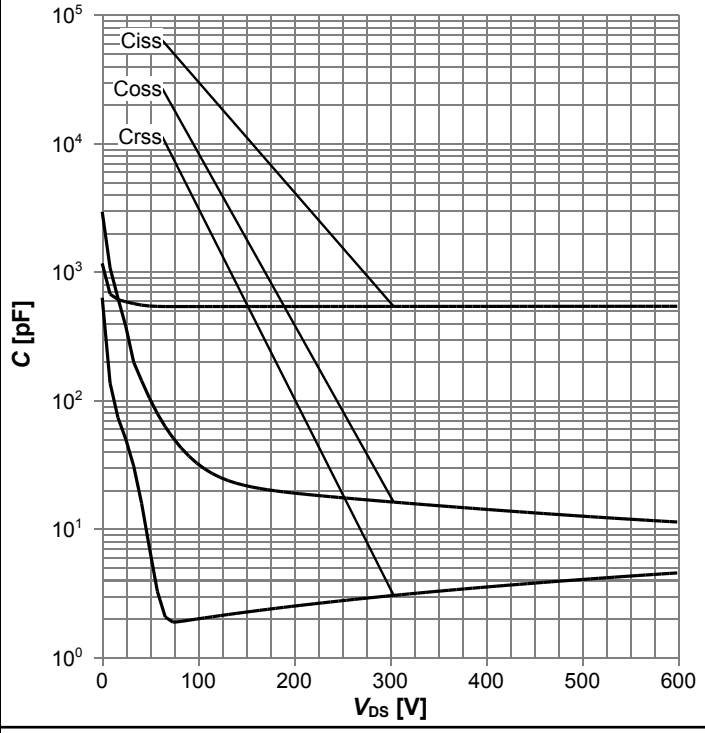
$E_{AS}=f(T_j)$; I_D=6.6 A; V_{DD}=50 V

Drain-source breakdown voltage



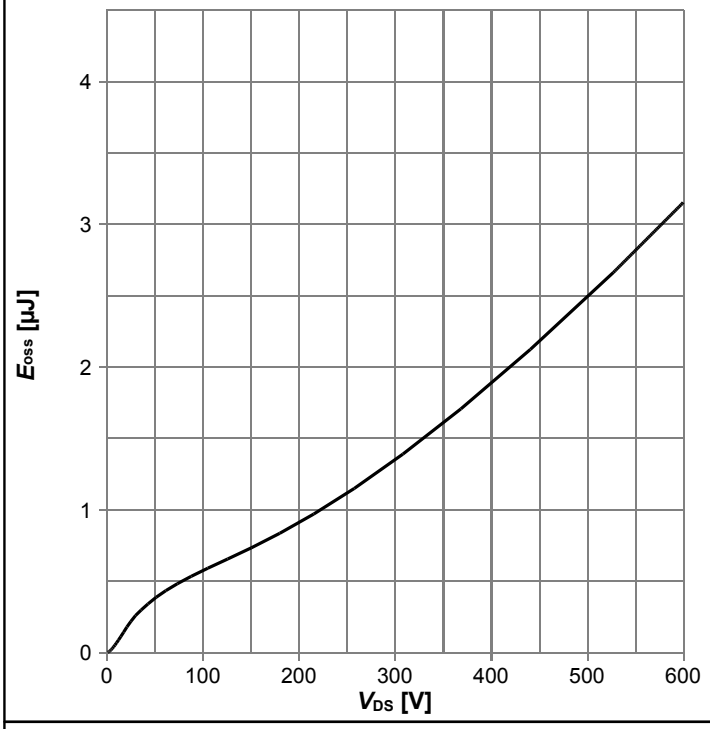
$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA

Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

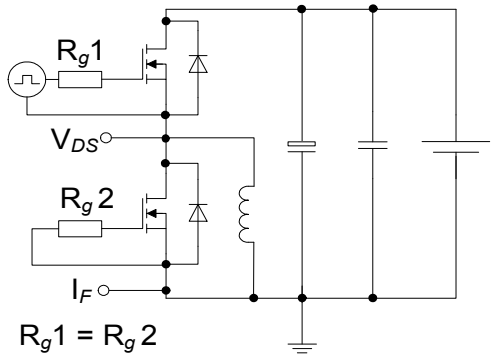
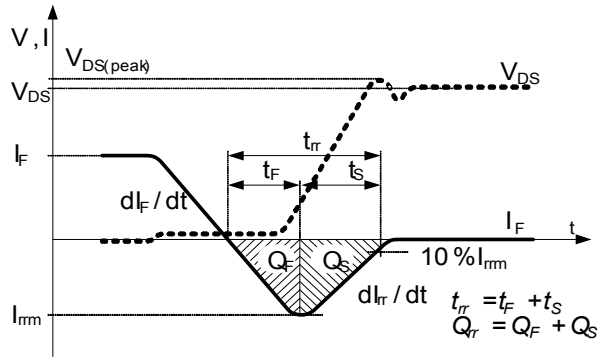
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

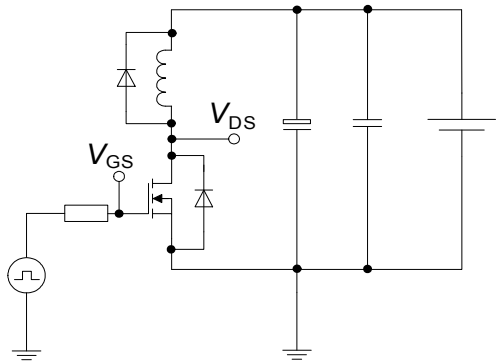
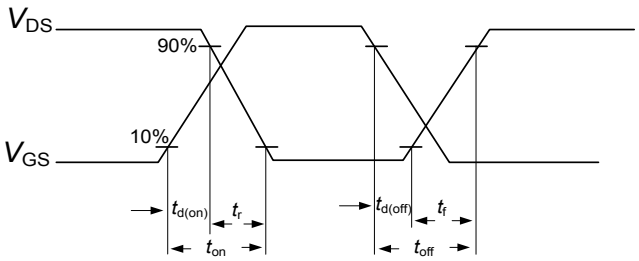
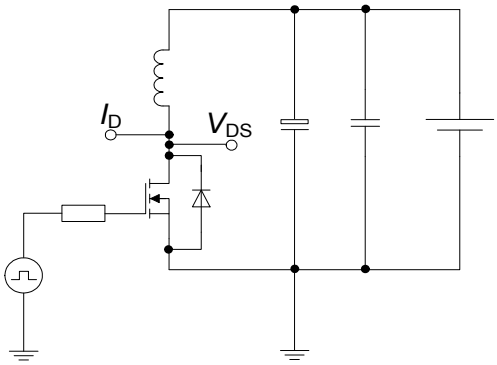
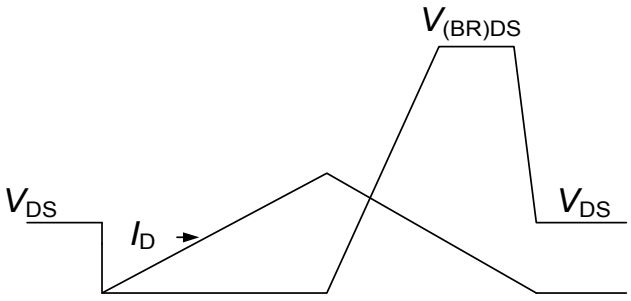
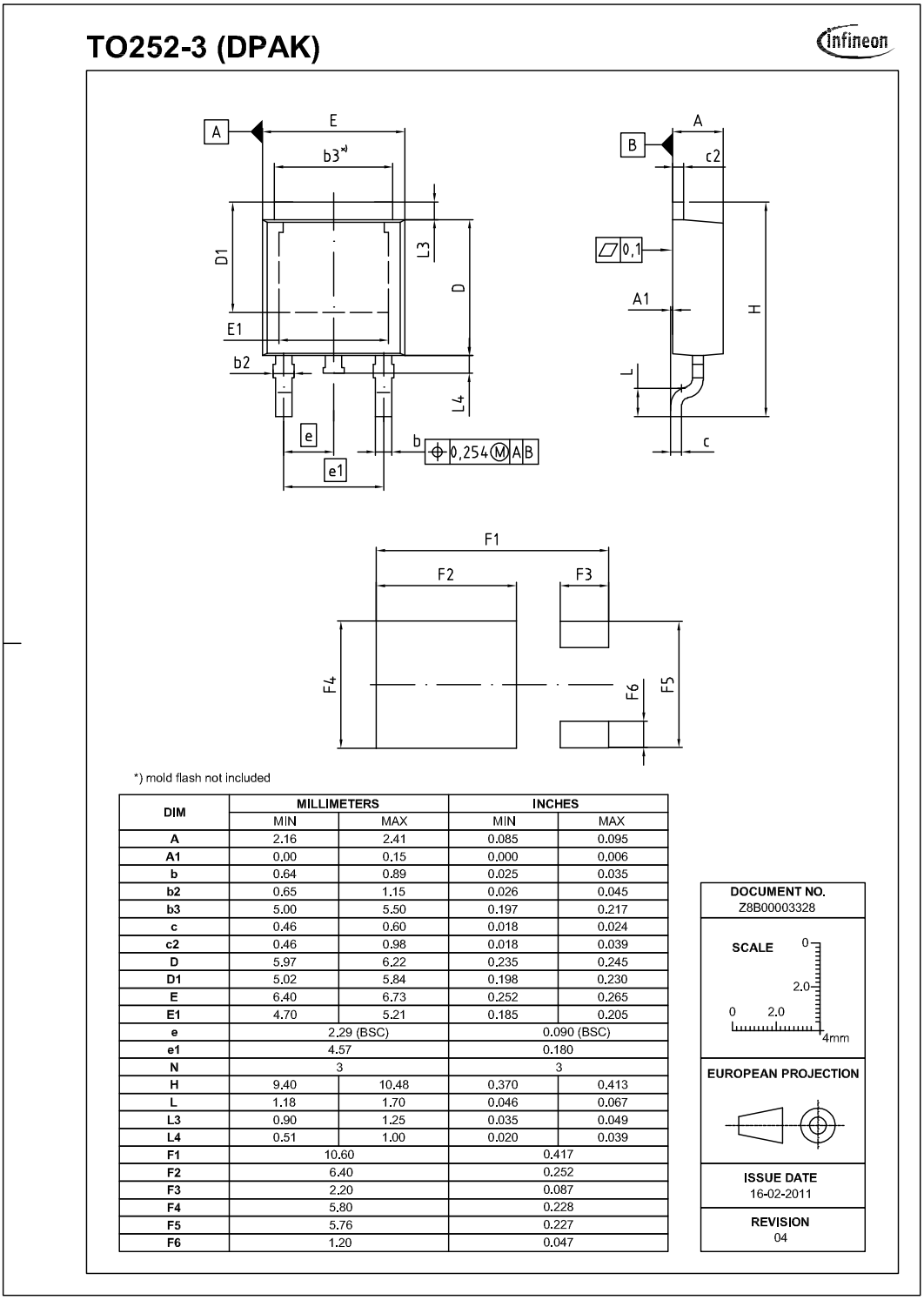
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

Figure 1 Outline PG-TO 252, dimensions in mm/inches

Revision History

IPD65R660CFDA

Revision: 2016-04-18, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-07-12	Preliminary
2.1	2014-11-19	Correction of Marking Code
2.2	2016-04-18	Updated: SOA diagrams, Idss at 150C, Rdson vs. Tj.

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