μA7307

1.6 WATT AUDIO AMPLIFIER

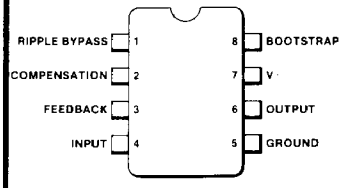
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA7307 is an integrated monolithic audio amplifier in an 8-pin plastic package. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use as a low frequency class B amplifier with wide range of supply voltage (3 to 16 V) and is primarily designed for low voltage portable radios and industrial applications where limited space and power consumption are important.

- **MINIMUM WORKING VOLTAGE OF 3 V**
- **LOW QUIESCENT CURRENT**
- **LOW NUMBER OF EXTERNAL COMPONENTS**
- **GOOD RIPPLE REJECTION**
- **NO CROSS-OVER DISTORTION**
- **TYPICAL OUTPUT POWER:**

1.6 W AT	**9 V - 4 Ω**
1.2 W AT	**9 V - 8 Ω**
0.75 W AT	**6 V - 4 Ω**
0.5 W AT	**6 V - 8 Ω**
0.22 W AT	**3.5 V - 4 Ω**
0.09 W AT	**3 V - 4 Ω**

CONNECTION DIAGRAM
8-PIN MINI-DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
7307C	**μA7307TC**

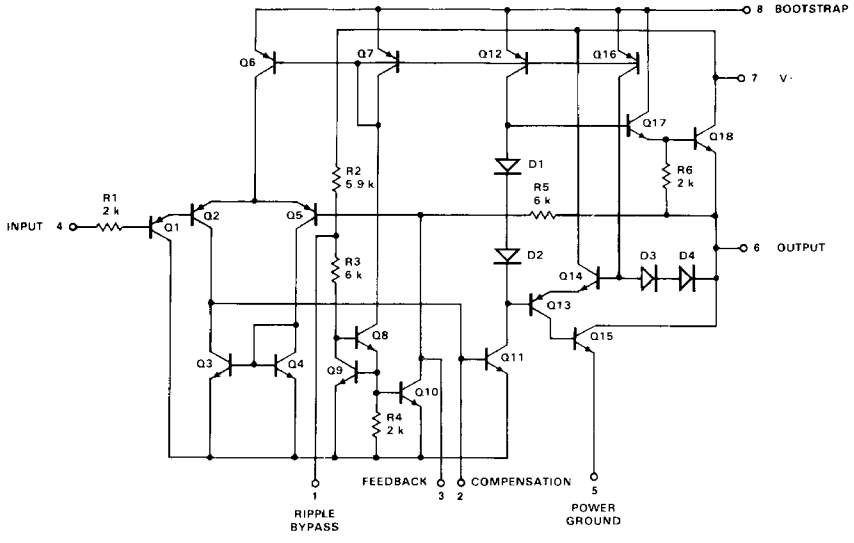
ABSOLUTE MAXIMUM RATINGS

Peak Voltage (Pin 8)	24 V
Supply Voltage	16 V
Output Peak Current	1.0 A
Power Dissipation at $T_{amb} \leq 50°C$	1.05 W
Storage and Junction Temperature	-40°C to 150°C
Lead Temperature (Soldering 10 s)	260°C

THERMAL DATA

θ_{j-amb} Thermal Resistance Junction-Ambient (copper frame) max 95°C/W

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: Power output measured at pin 6, T_A = 25°C unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		3		16	V
Quiescent Output Voltage (Pin 6)	V+ = 9 V	4	4.5	5	V
Quiescent Drain Current	V+ = 9 V		4	9	mA
Bias Current (Pin 4)	V+ = 9 V		0.1	0.7	μA
Power Output, Figure 1	THD = 10%, R_{FB} = 120 Ω, f = 1 kHz,				
	V+ = 12 V, R_L = 8 Ω		2.0		W
	V+ = 9 V, R_L = 4 Ω		1.6		W
	V+ = 9 V, R_L = 8 Ω	0.9	1.2		W
	V+ = 6 V, R_L = 4 Ω		0.75		W
	V+ = 3.5 V, R_L = 4 Ω		0.22		W
	V+ = 3 V, R_L = 4 Ω		0.09		W
Input Sensitivity, Figure 1	P_{OUT} = 1.2 W, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		16	24	mV
	R_{FB} = 120 Ω		60	82	mV
Input Sensitivity, Figure 1	P_{OUT} = 50 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		3.5		mV
	R_{FB} = 120 Ω		12		mV
Input Resistance			5		MΩ
Frequency Response (-3 dB) Figure 1	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω				
	C_{FB} = 680 pF		25-7000		Hz
	C_{FB} = 220 pF		25-20,000		Hz
Total Harmonic Distortion Figure 1	P_{OUT} = 500 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		0.8		%
	R_{FB} = 120 Ω		0.4		%
Voltage Gain (Open Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz		75		dB
Voltage Gain (Closed Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz				
	R_{FB} = 33 Ω		45		dB
	R_{FB} = 120 Ω	31	34	37	dB
Input Noise Voltage	V+ = 9 V, BW (-3.0 dB) = 25-20,000 Hz		3.5		μV
Input Noise Current	V+ = 9 V, BW (-3.0 dB) = 25-20,000 Hz		0.4		nA
Signal Plus Noise to Noise Ratio	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω				
	BW (-3.0 dB) = 25-20,000 Hz				
	R_1 = 100 kΩ, P_{OUT} = 1.2 W		70		dB
Supply Voltage Rejection, Figure 2	V = 9 V, R_L = 8 Ω, f (ripple) = 100 Hz,				
	C6 = 50 μF, R_{FB} = 120 Ω		42		dB

APPLICATIONS INFORMATION

Two typical application circuits are shown in *Figures 1* and *2*. The ripple bypass capacitor C6 may be omitted in most battery operated applications or where high ripple rejection is not required.

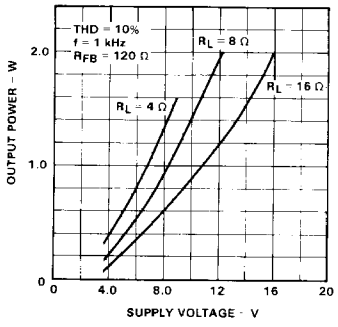
Resistor R2 must be included in series with C3 to assure stable operation of the μA7307.

A PC board layout for the circuit of *Figure 1* is shown to scale in *Figure 3*. A photograph of a finished module is shown in *Figure 4*.

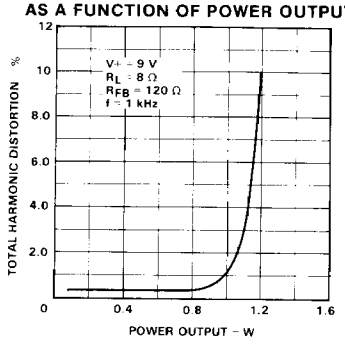
The PC board layout for the circuit of *Figure 2* is shown to scale in *Figure 5*, and a photograph is shown in *Figure 6*.

TYPICAL PERFORMANCE CURVES

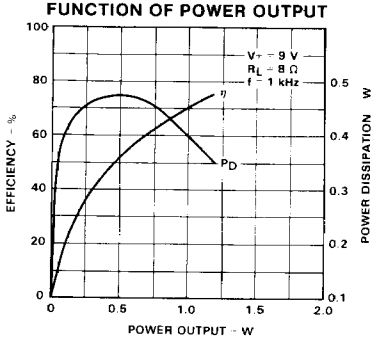
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



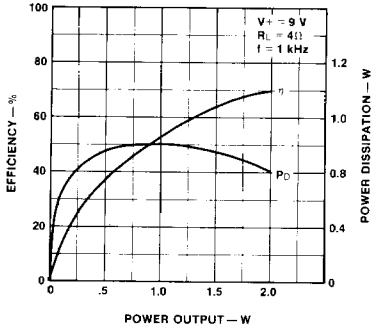
TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT



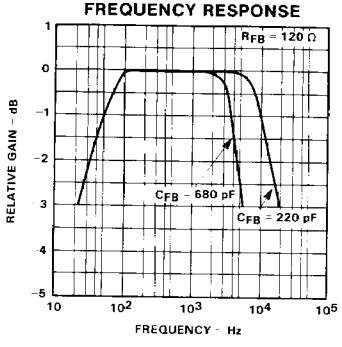
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT



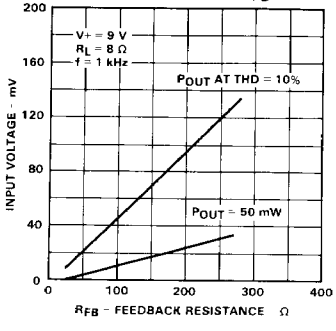
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT



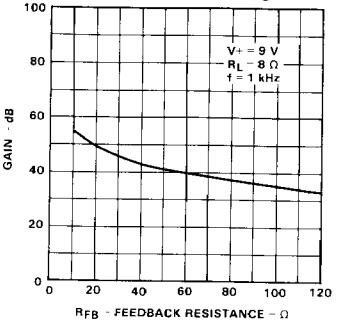
TYPICAL RELATIVE FREQUENCY RESPONSE



INPUT SENSITIVITY AS A FUNCTION OF R_{FB}



TYPICAL VOLTAGE GAIN (CLOSED LOOP) AS A FUNCTION OF R_{FB}



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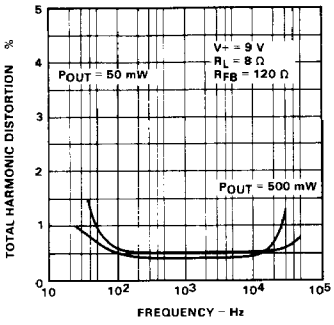
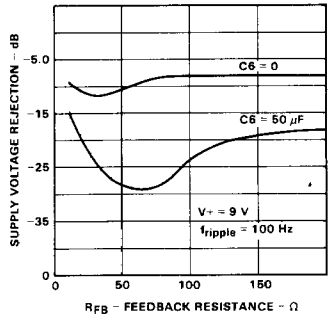
TYPICAL PERFORMANCE CURVES

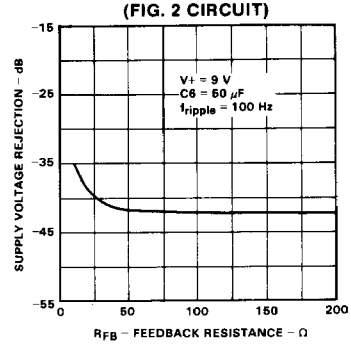
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



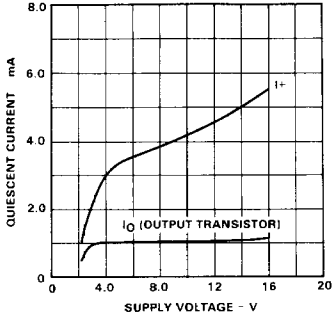
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_{FB} FOR FIG. 1 CIRCUIT



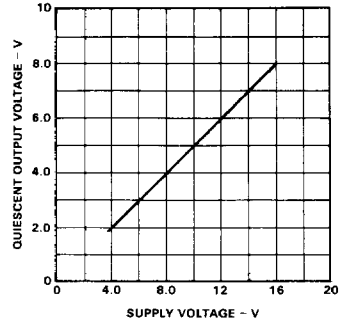
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_{FB} (FIG. 2 CIRCUIT)



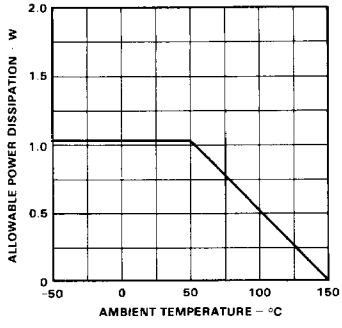
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



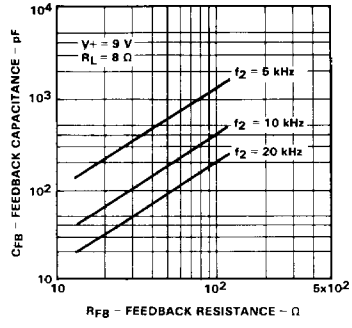
QUIESCENT OUTPUT VOLTAGE AT PIN 12 AS A FUNCTION OF SUPPLY VOLTAGE



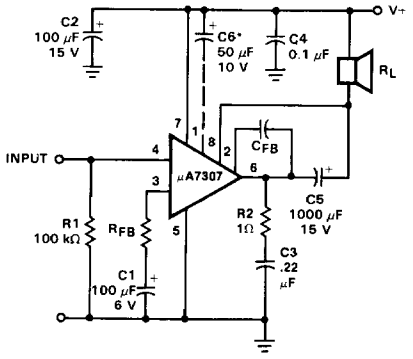
POWER RATING CHART AS A FUNCTION OF AMBIENT TEMPERATURE

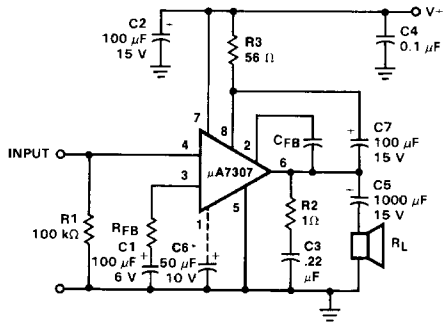


TYPICAL VALUE OF C_{FB} AS A FUNCTION OF R_{FB}



TEST AND APPLICATION CIRCUITS





*Capacitor C6 must be used when high ripple rejection is desired.

Fig. 1 Circuit Diagram with Load Connected to the Supply Voltage

Fig. 2 Circuit Diagram with Load Connected to Ground

Bottom View

Fig. 3 1:1 Scale P.C. Board Layout for Circuit of Figure 1

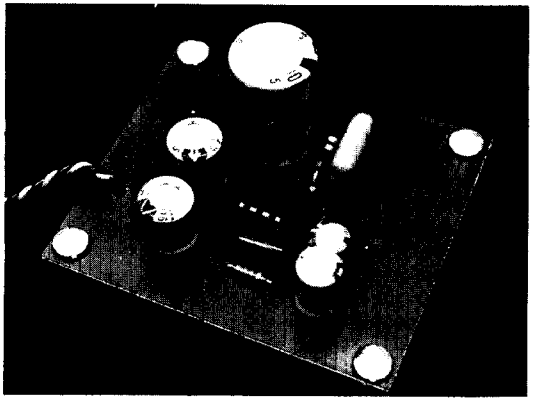
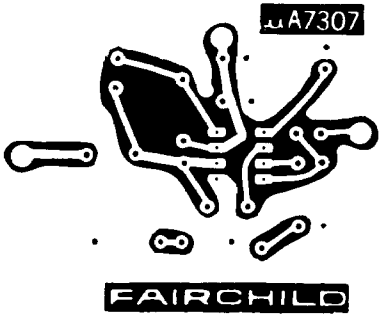


Fig. 4 Photograph of Assembled Board for Figure 1



Bottom View

Fig. 5 1:1 Scale P.C. Board Layout for Circuit of Figure 2

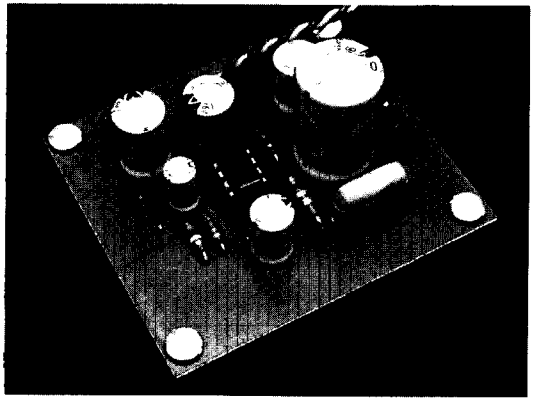


Fig. 6 Photograph of Assembled Board for Figure 2