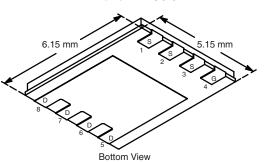


Vishay Siliconix

COMPLIANT

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R _{DS(on)} (Ω)	(Ω) I _D (A) ^{b, c} Q		
60	0.010 at V _{GS} = 10 V	16	45	
	0.0125 at V _{GS} = 6 V	14.4	40	



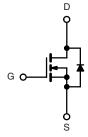
PowerPAK SO-8



- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

- Primary Side Switch for 24 V DC/DC Applications
- Secondary Synchronous Rectifier



Ordering Information: Si7370ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	s otherwise not	ed		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	60	v	
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C		50 ^a		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I _D	50 ^a		
	T _A = 25 °C	U	16 ^{b, c}		
	T _A = 70 °C		12.9 ^{b, c}	А	
Pulsed Drain Current		I _{DM}	50	~	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	50 ^a		
Solution Diale Diale Suller	T _A = 25 °C	'S	4.4 ^{b, c}		
Avalanche Current		I _{AS}	50		
Single Pulse Avalanche Energy	E = 0.1 mm	E _{AS}	125	mJ	
	T _C = 25 °C		69.4		
Maximum Power Dissipation	T _C = 70 °C	PD	44.4	w	
	T _A = 25 °C	• 0	5.2 ^{b, c}	••	
	T _A = 70 °C		3.3 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	℃	
Soldering Recommendations (Peak Temperature) ^{d, e}			260	U	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	19	24	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.5	1.8	- C/W	

Notes:

a. Package Limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (http://www.vishay.com/ppg?73461). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 65 °C/W.





SPECIFICATIONS $T_J = 25 \degree C$, Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static	Symbol	Test conditions	WIII.	тур.	Wax.	Unit	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$			60		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 9.8			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	2.0	0.0	4.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS} -	$V_{DS} = 60 V, V_{GS} = 0 V$			1		
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			5	μA	
On-State Drain Current ^a	I _{D(on)}	$\frac{V_{DS} \ge 5 \text{ V, } V_{GS} = 10 \text{ V}}{V_{DS} \ge 5 \text{ V, } V_{GS} = 10 \text{ V}}$	50			A	
Drain-Source On-State Resistance ^a	D(on)	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 12 \text{ A}$		0.008	0.010	- Ω	
	R _{DS(on)}	$V_{GS} = 6 \text{ V}, \text{ I}_{D} = 10 \text{ A}$		0.010	0.0125		
Forward Transconductance ^a	9 _{fs}	$V_{\rm DS} = 15 \text{ V}, \text{ I}_{\rm D} = 10 \text{ A}$		50		S	
Dynamic ^b			1	I	I		
Input Capacitance	C _{iss}			2850		pF	
Output Capacitance	C _{oss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		375			
Reverse Transfer Capacitance	C _{rss}			150			
Total Gate Charge	Q _g			45	70		
Gate-Source Charge	Q _{gs}	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_{D} = 12$ A		12.2		nC	
Gate-Drain Charge	Q _{gd}			10			
Gate Resistance	Rg	f = 1 MHz	0.2	0.75	1.5	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	V_{DD} = 30 V, R_{L} = 30 Ω		9	18	- ns -	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		40	60		
Fall Time	t _f			20	30		
Turn-On Delay Time	t _{d(on)}			25	40		
Rise Time	t _r	V_{DD} = 30 V, R_L = 30 Ω		14	25		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong \text{1}$ A, V_GEN = 10 V, R_g = 1 Ω		35	55		
Fall Time	t _f			20	30		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	۱ _S	$T_{C} = 25 \ ^{\circ}C$			50	А	
Pulse Diode Forward Current ^a	I _{SM}				50	А	
Body Diode Voltage	V_{SD}	I _S = 3 A		0.75	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			35	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 3 A, dl/dt = 100 A/μs, T _J = 25 °C		45	70	nC	
Reverse Recovery Fall Time	t _a	F = 0 A, u/ul = 100 A/µs, $1 = 25$ C		22		20	
Reverse Recovery Rise Time	t _b	7		13		ns	

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

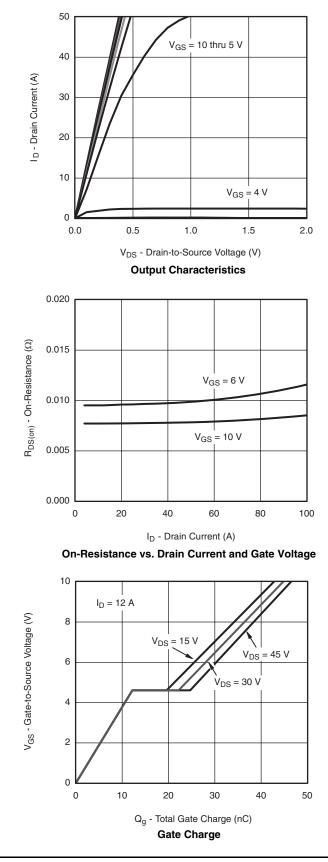
b. Guaranteed by design, not subject to production testing.

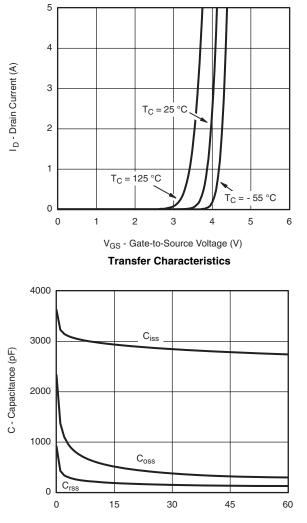
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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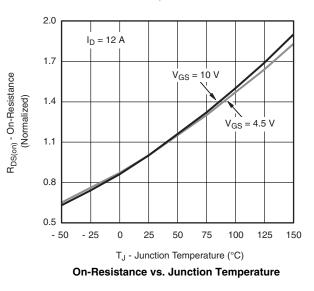
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





 V_{DS} - Drain-to-Source Voltage (V)

Capacitance



Document Number: 68746 S-81472-Rev. A, 23-Jun-08

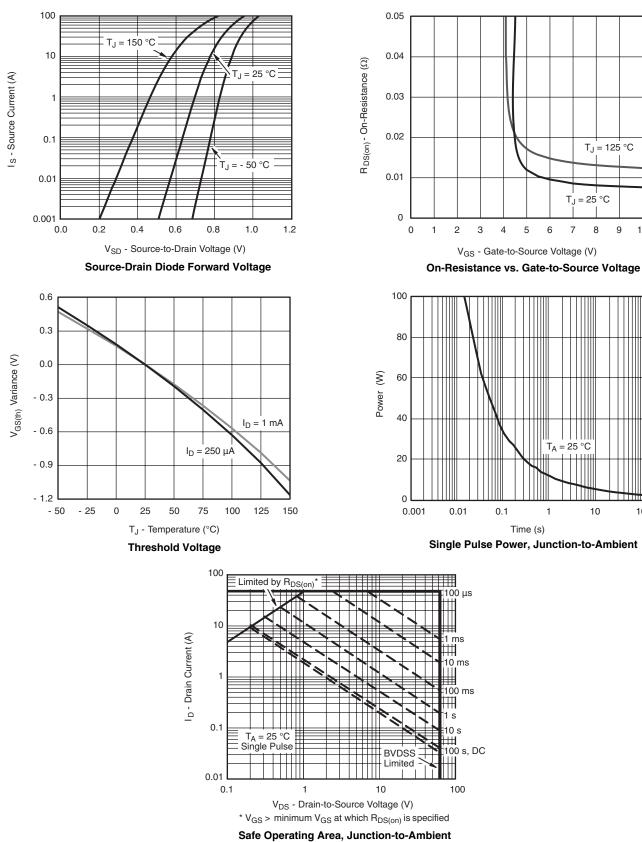
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10

100

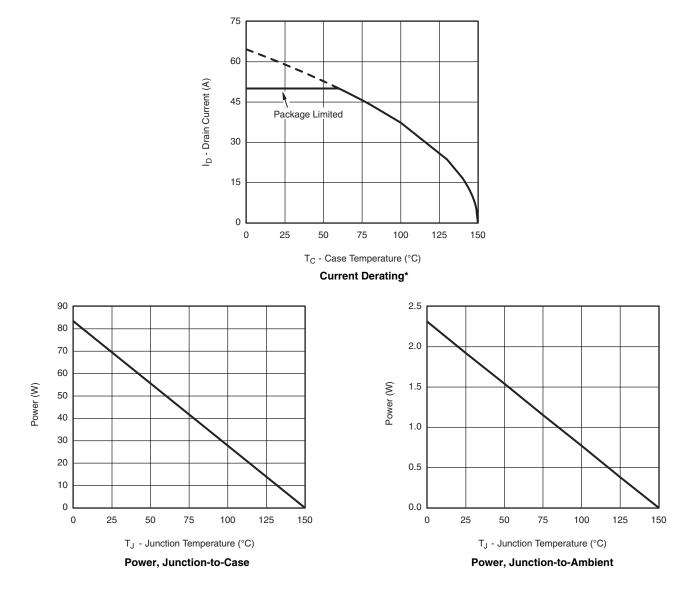
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





Si7370ADP Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

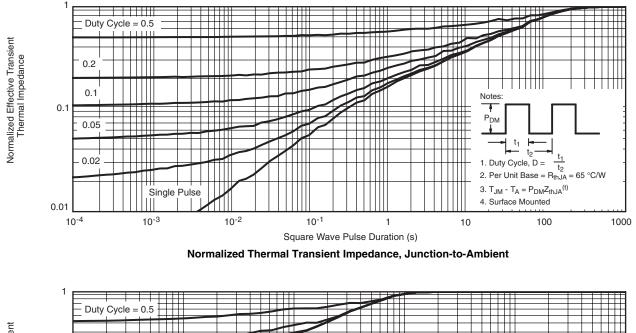


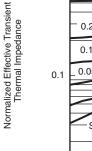
* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

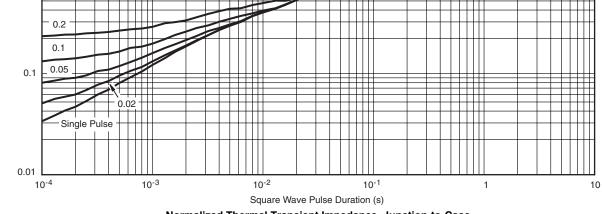
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?68746.



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