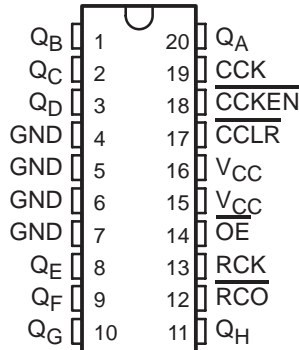


74ACT11590 8-BIT BINARY COUNTER WITH REGISTERED 3-STATE OUTPUTS

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Parallel Registered Outputs
- Internal Counters Have Direct Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE
(TOP VIEW)



description

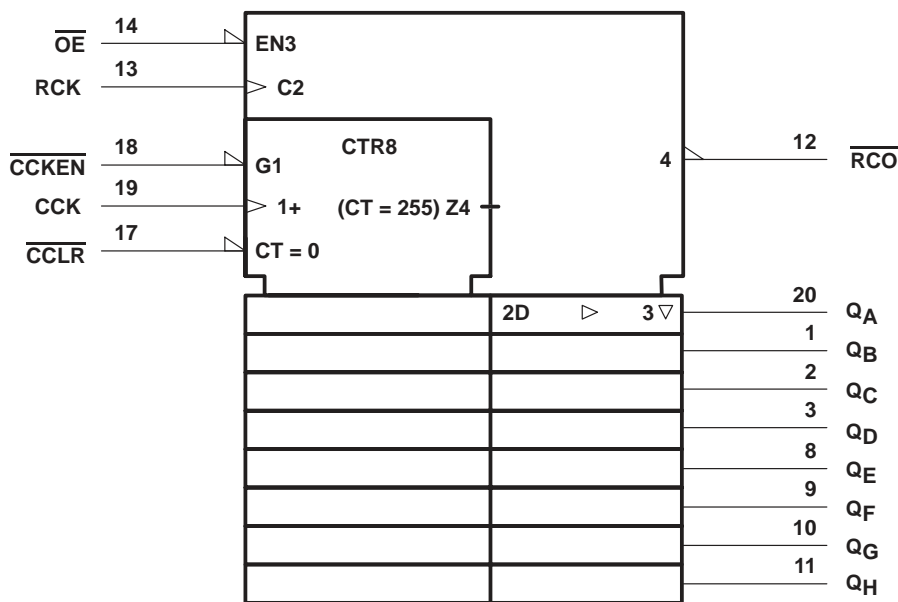
The 74ACT11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear (\overline{CCLR}) input and a count-enable (\overline{CCKEN}) input. For cascading, a ripple-carry (\overline{RCO}) output is provided. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to CCK of the following stage.

Both the register and the counter have individual positive-edge-triggered clocks. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The 74ACT11590 is characterized for operation from -40°C to 85°C .

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

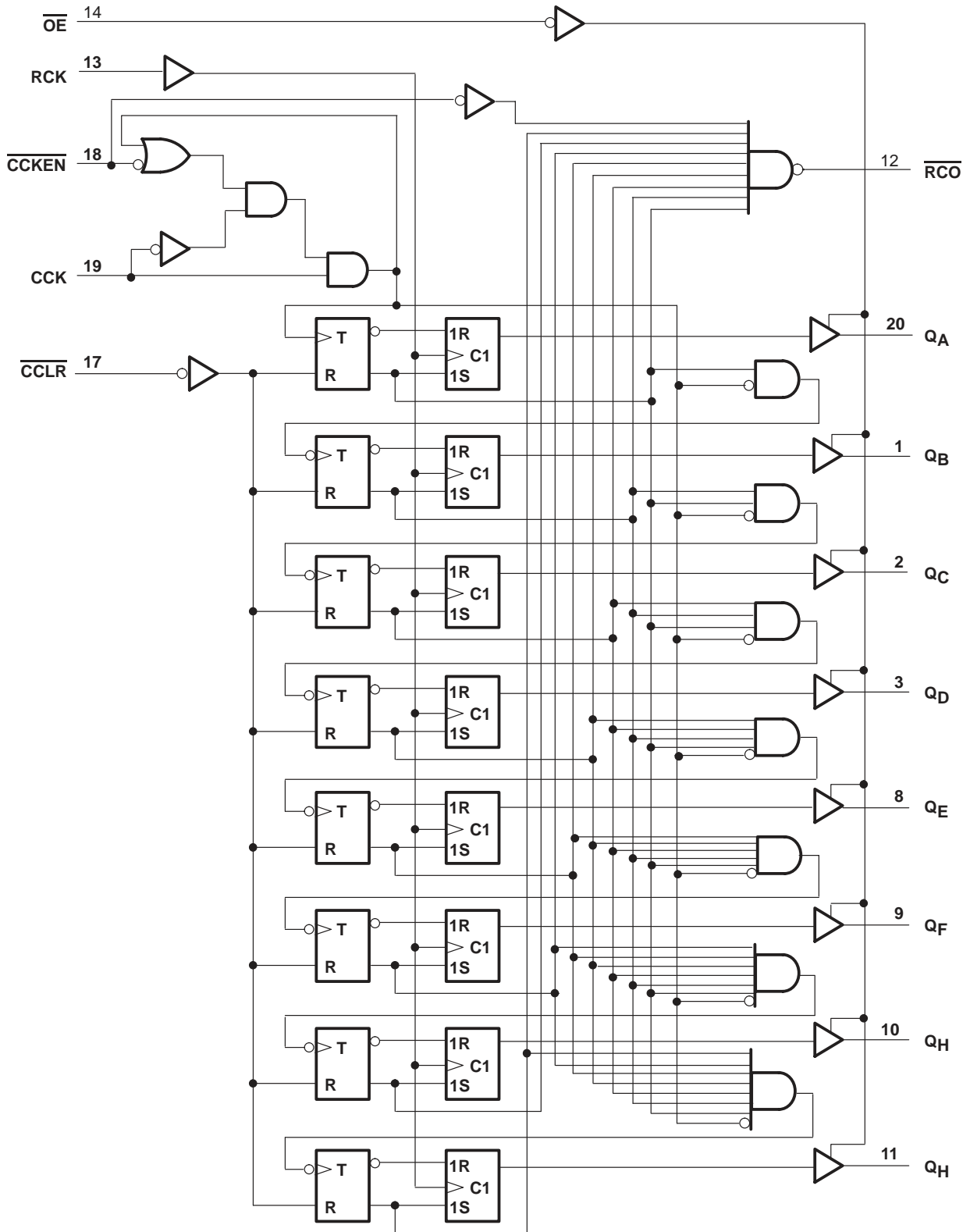
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74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

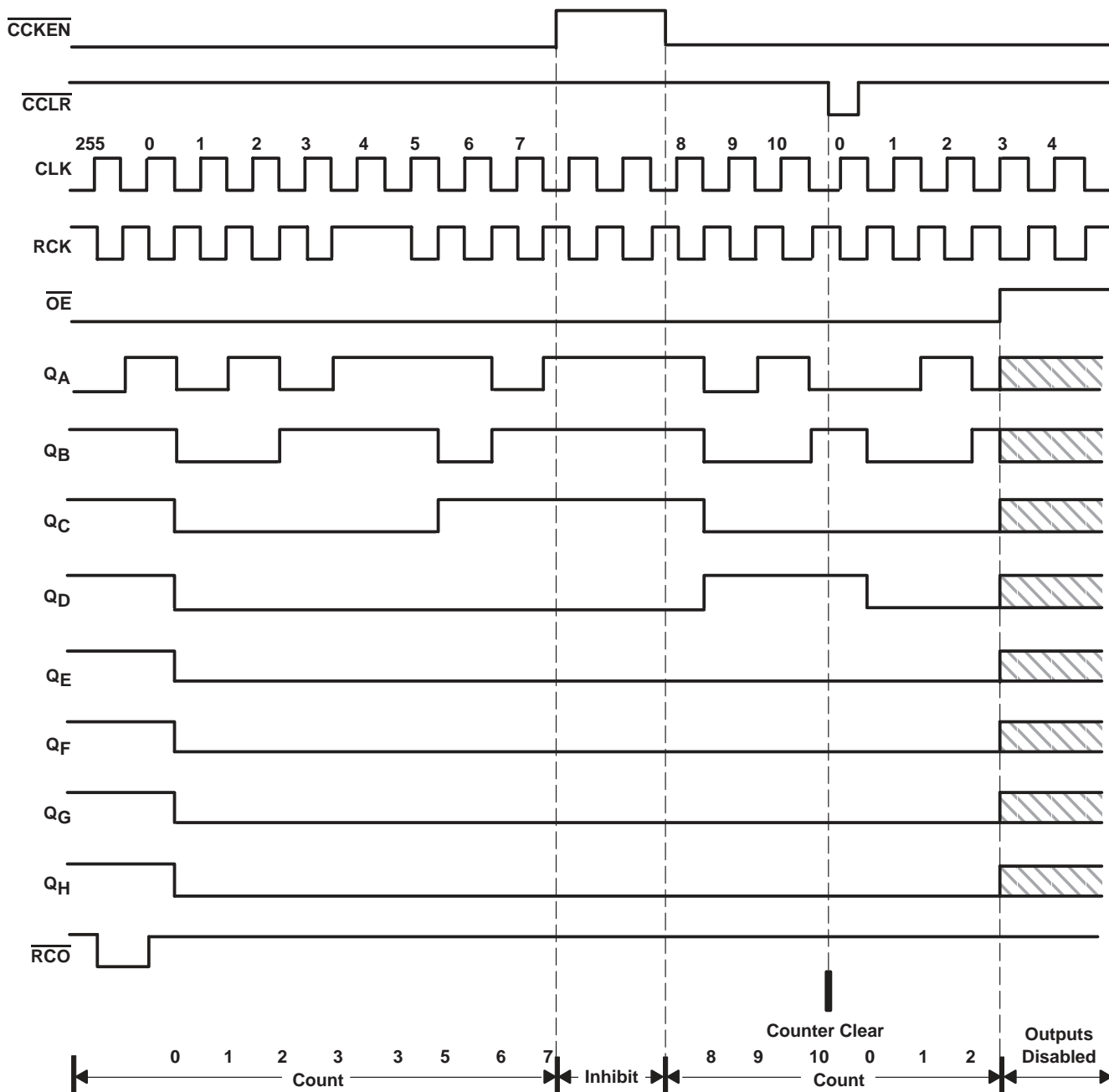
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logic diagram (positive logic)



74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS
SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

typical operating sequence



74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 225 mA
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_I Input voltage	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	V
I_{OH} High-level output current			-24	mA
I_{OL} Low-level output current			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	ns/V
T_A Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS
 SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4		4.4		V	
		5.5 V	5.4		5.4			
	I _{OH} = -24 mA	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	I _{OH} = -75 mA†	5.5 V			3.85			
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1	V	
		5.5 V			0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
	I _{OL} = 75 mA†	5.5 V				1.65		
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5	±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	80	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9	1	mA	
C _i	V _I = V _{CC} or GND	5 V			3		pF	
C _o	V _O = V _{CC} or GND	5 V			11		pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f _{clock}	Clock frequency, CCK or RCK	0	80	0	80	MHz
t _w	Pulse duration	CCK or RCK high or low		6.3	6.3	ns
		CCLR low		8.4	8.4	
t _{su}	Setup time	CCKEN low before CCK↑		5.1	5.1	ns
		CCLR high before CCK↑		1.6	1.6	
		CCK↑ before RCK↑§		5.5	5.5	
t _h	Hold time	CCKEN low after CCK↑		0.6	0.6	ns

§ This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.



74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

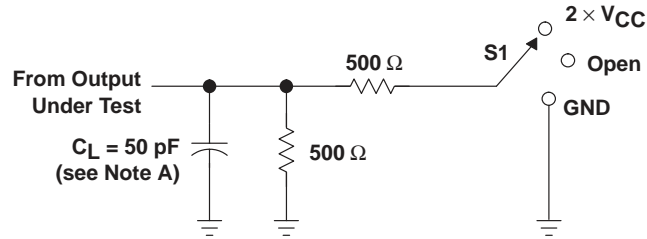
switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80			80		MHz
t_{PLH}	CCK	$\overline{\text{RCO}}$	4.5	8	11	4.5	13	ns
t_{PHL}			5.1	9	13.8	5.1	16.4	
t_{PLH}	$\overline{\text{CCLR}}$	$\overline{\text{RCO}}$	3.5	7	11	3.5	13.1	ns
t_{PLH}	RCK	Q	4.6	8	11.1	4.6	13	ns
t_{PHL}			3.9	7.6	11.8	3.9	13.9	
t_{PZH}	$\overline{\text{OE}}$	Q	4	8.3	13.2	4	15.6	ns
t_{PZL}			3.8	8.2	13.9	3.8	16.2	
t_{PHZ}	$\overline{\text{OE}}$	Q	5.3	8	10.3	5.3	11.5	ns
t_{PLZ}			6.1	9.1	11.5	6.1	13	
t_{PLH}	$\overline{\text{CCKEN}}$	$\overline{\text{RCO}}$	3.8	6.8	9.7	3.8	11.2	ns
t_{PHL}			2.8	7.6	11	2.8	12.8	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	66	pF
			42	

PARAMETER MEASUREMENT INFORMATION

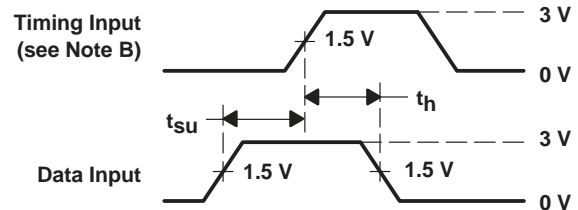


LOAD CIRCUIT

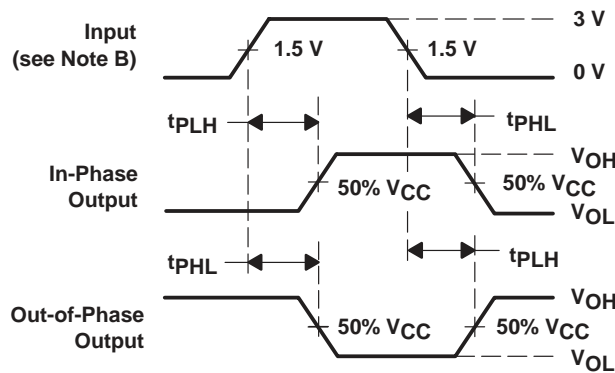
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



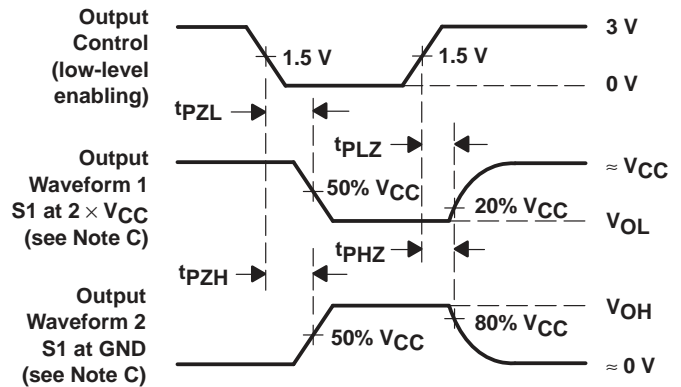
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT11590DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
74ACT11590DWR	OBSOLETE	SOIC	DW	0		TBD	Call TI	Call TI
74ACT11590N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

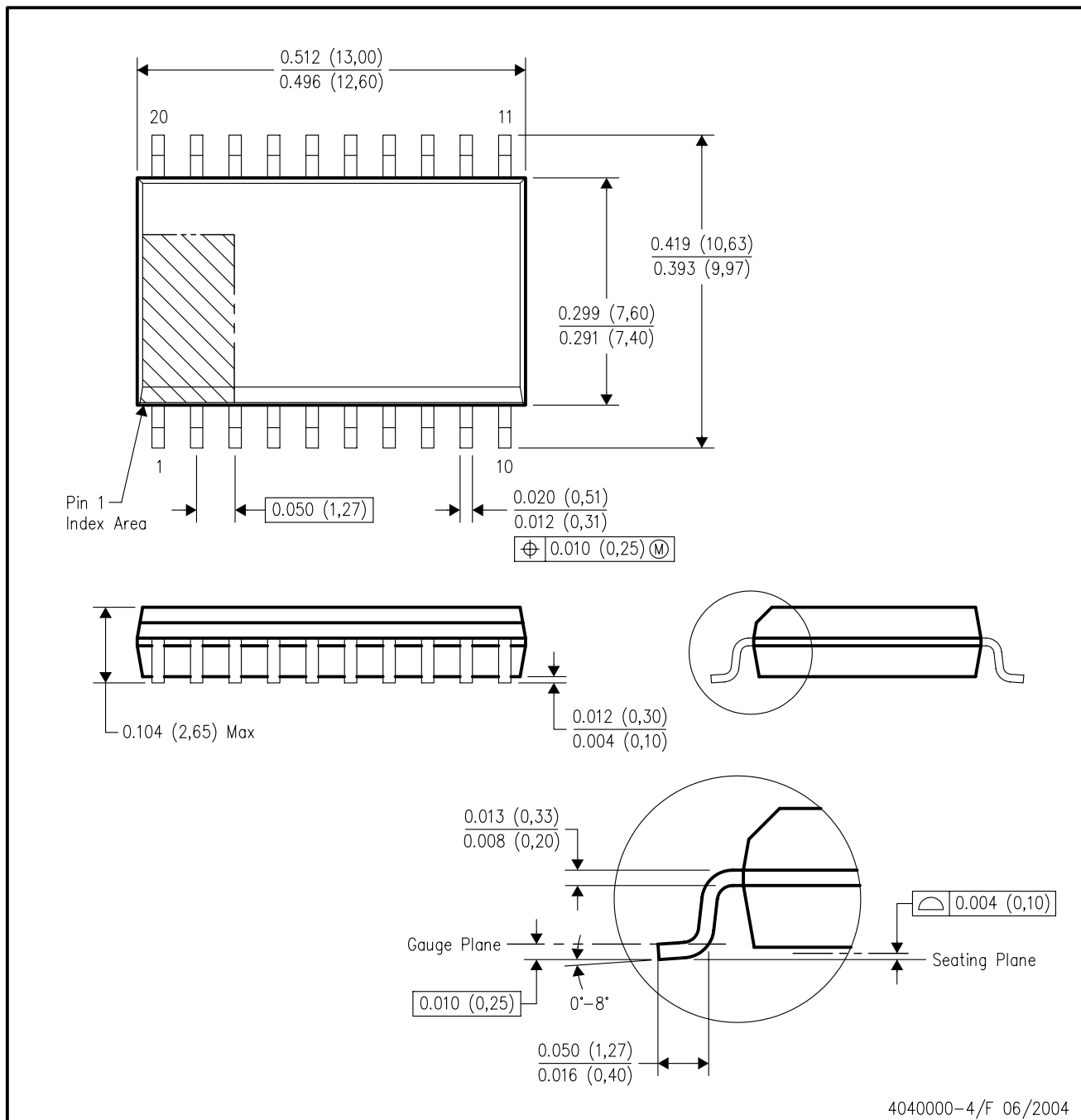
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

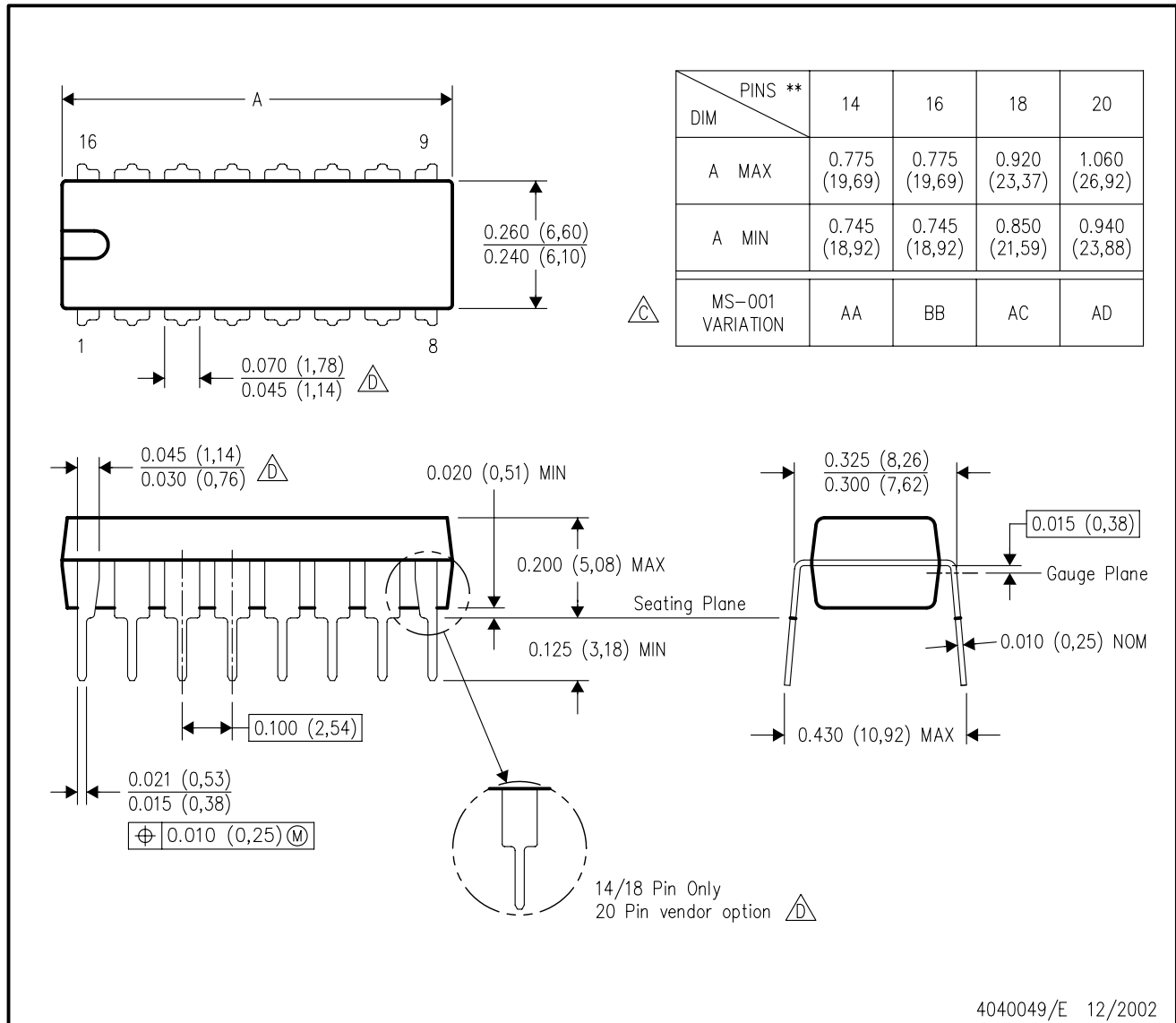


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ACT11590DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
74ACT11590DWR	OBSOLETE	SOIC	DW	0		TBD	Call TI	Call TI	-40 to 85		
74ACT11590N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

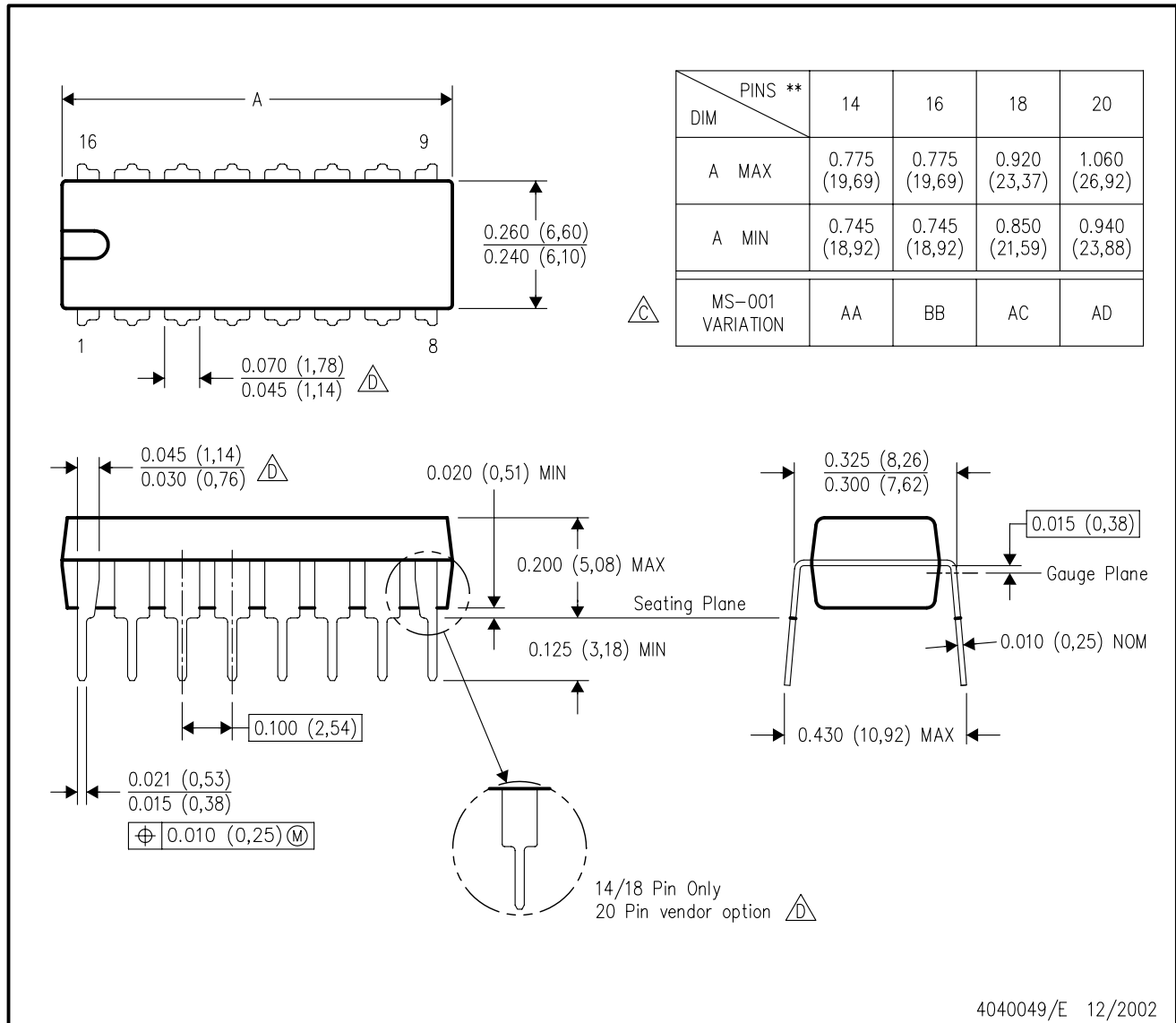
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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

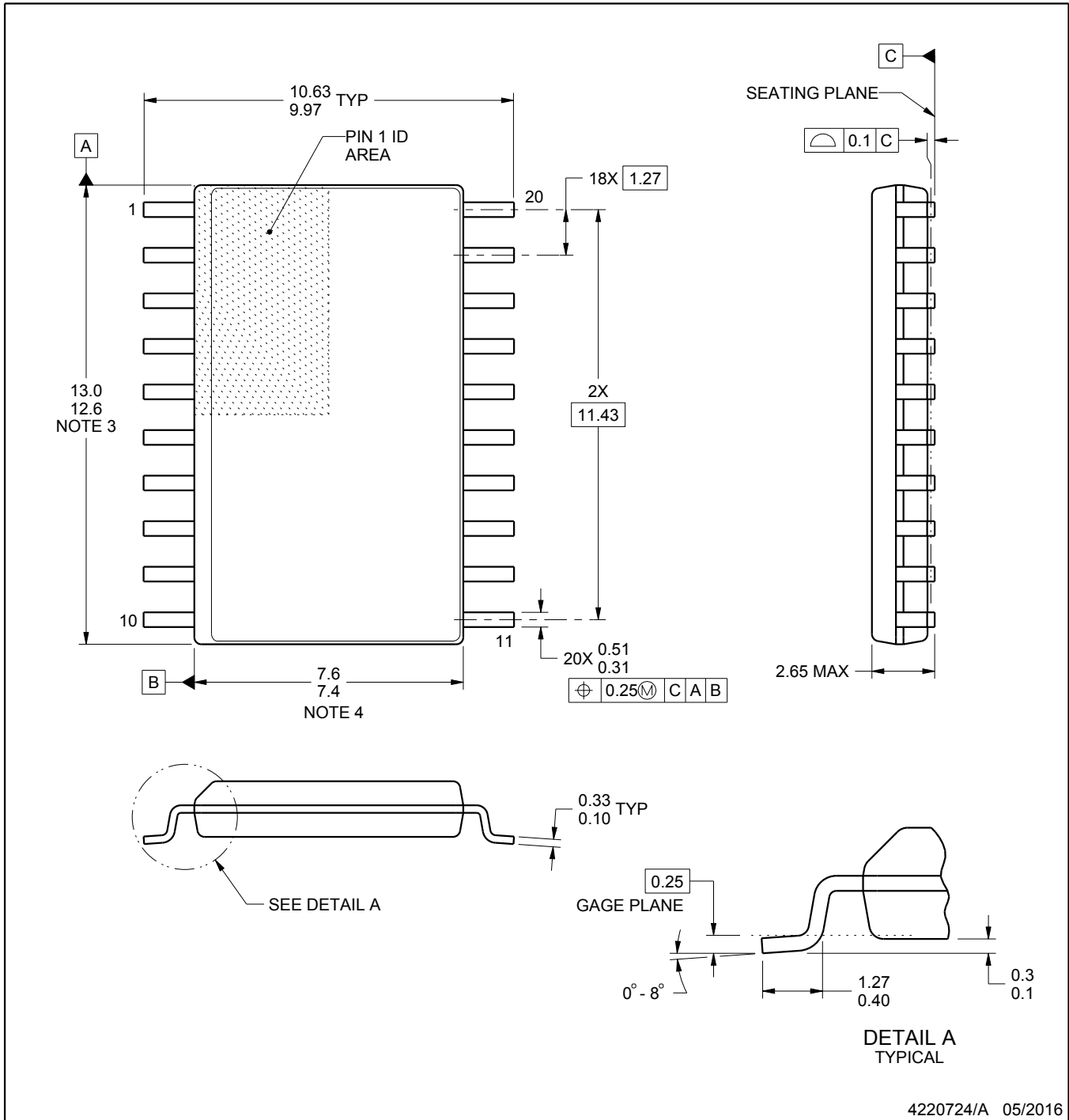
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

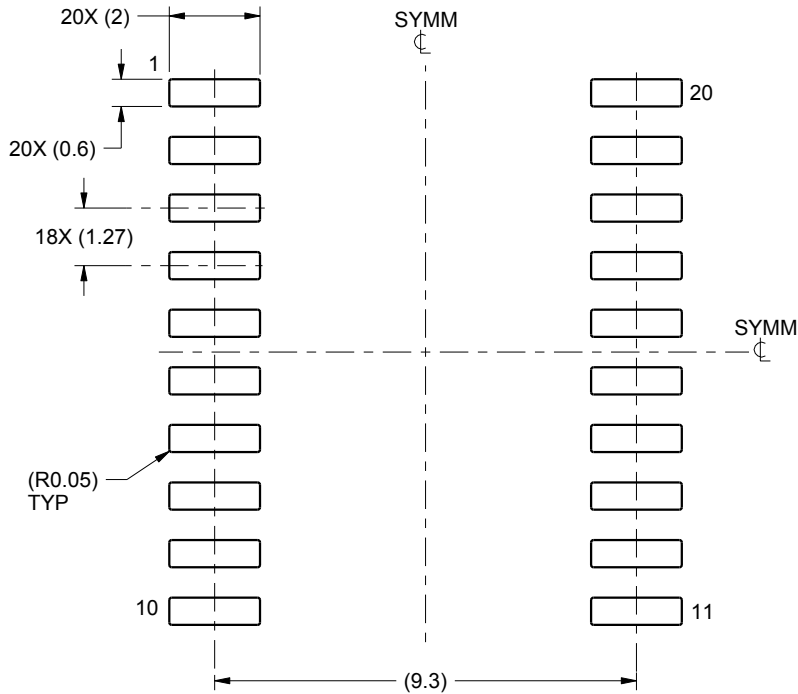
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

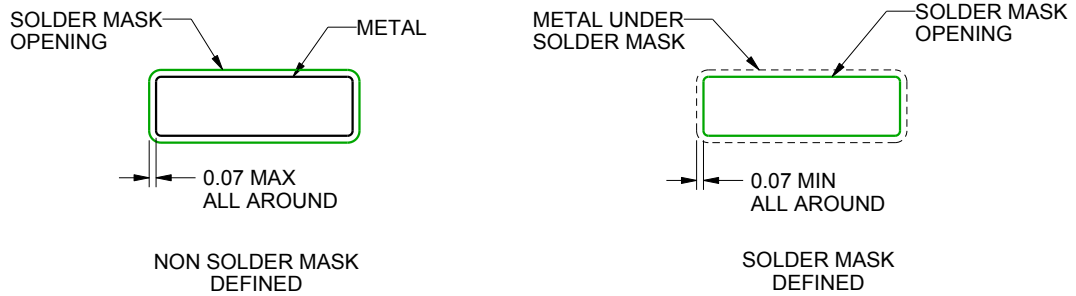
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

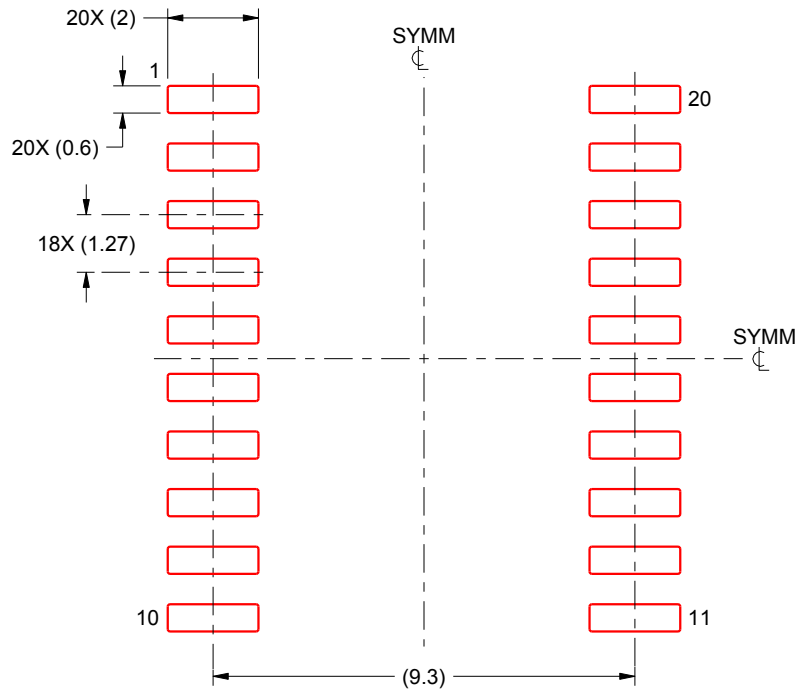
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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