National Semiconductor

PRELIMINARY

MM74C945, MM74C947 4-Digit Up/Down Counter/Latch/Decoder Driver

General Description

The MM74C945, MM74C947 are 4-digit counters for directly driving LCD displays. The MM74C945 contains a 4-decade up/down counter, output latches, counter/latch select multiplexer and 7-segment decoders. Also included are the backplane oscillator/driver, segment drivers and display blanking circuitry.

The MM74C947 differs from the MM74C945 in that it has no counter/latch multiplexer, but provides true leading zero blanking. All leading zeroes are automatically blanked except the least significant digit, which can be optionally blanked.

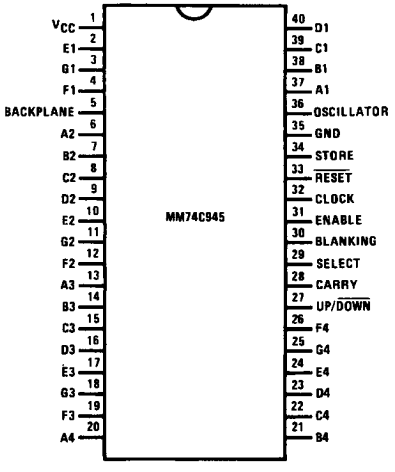
Both devices provide 28-segment outputs to drive a 4-digit display. Segment and backplane waveforms are generated internally, but can also be slaved to an external signal. This facilitates cascading of multiple displays.

Features

- 4-decade up/down count
- Direct 4-digit drive for high contrast and long display life
- Carry/borrow out for cascading counters
- Schmitt trigger clock input
- MM74C945 has display select to allow viewing of counter or latch
- Store and reset inputs allow operation as frequency or period counter
- MM74C947 has true ripple blanking; least significant digit may be optionally blanked

Connection Diagrams

Dual-In-Line Package



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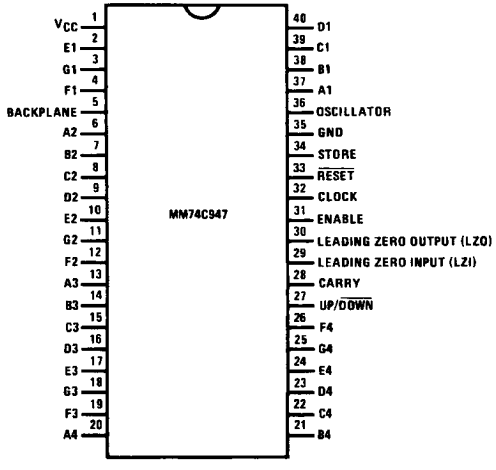
Top View

Order Number MM74C945*

Dual-In-Line Package



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Top View

Order Number MM74C947*

*Please look into Section 8, Appendix D for availability of various package types.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A) MM74C945/MM74C947	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	500 mW
Operating V_{CC} Range	3.0V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	$V_{CC} = 5V$, V_{IN} (0 ⟶ 5) V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Only)	$V_{CC} = 5V$, V_{IN} (0 ⟶ 5) V	1.5	2.2	2.4	V
Hysteresis ($V_{T+} - V_{T-}$) (Clock Only)	$V_{CC} = 5V$	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 5V$, $I_O = +10\ \mu A$			0.5	V
Clock Input Current $\lvert I_{IN} \rvert$	$V_{CC} = 5V$, $V_{IN} = 5V/0V$		0.005	1.0	μA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC} = 5V$, $V_{IN} = 0V$	-2.0	-12	-25	μA
Oscillator Input Current (I_{OSL})	$V_{CC} = 5V$, $V_{IN} = 0V/5V$		± 1	± 10.0	μA
Supply Current (I_{CC}) (Note 3)	$V_{CC} = 5V$, $V_{IN} = 0V/5V$		10	60	μA
Oscillator Input Voltage $V_{IH\ (OSC)}$ $V_{IL\ (OSC)}$	When Driving Oscillator Pin with External Signal	 0.2 V_{CC}		 $V_{CC} - 0.2$	 V V
DC Offset Voltage (Note 4)	$V_{CC} = 5V$			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 4.75V$	$V_{CC} - 1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (Short Circuit Current)					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	1.75	2.7		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	1.75	3.2		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	1.4	2.0		mA
Output Sink Current (I_{SINK}) (Segment Output)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	1.4	2.2		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	12.6	15.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	12.6	20.0		mA

AC Electrical Characteristics* T_J = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	V_{CC} = 5.0V		375	600	ns
f_{CLK}	Maximum Clock Frequency	V_{CC} = 5.0V	2	3		MHz
t_r, t_f	Clock Input Rise or Fall Time	V_{CC} = 5.0V			No Limit	MHz
t_{WR}	Reset Pulse Width	V_{CC} = 5.0V	180	120		ns
t_{WS}	Store Pulse Width	V_{CC} = 5.0V	150	80		ns
$t_{SU\ (CK,\ S)}$	Clock to Store Set-Up Time	V_{CC} = 5.0V	500	270		ns
t_{SR}	Store to Reset Wait Time	V_{CC} = 5.0V	280	170		ns
$t_{SU\ (E,\ CK)}$	Enable to Clock Set-Up Time	V_{CC} = 5.0V	140	80		ns
t_{RR}	Reset Removal	V_{CC} = 5.0V	50	0		ns
$t_{SU\ (U/D,\ CK)}$	Up/Down to Clock Set-Up Time	V_{CC} = 5.0V	300	190		ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating, V_{CC} = 5.0V		85		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 2)		5		pF
t_{rfs}	Segment Rise/Fall Time	C_{load} = 200 pF		0.5		μs
t_{rfb}	Backplane Rise/Fall time	C_{load} = 5000 pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating, V_{CC} = 5.0V		11		kHz

*AC Parameters are guaranteed by DC correlated testing.

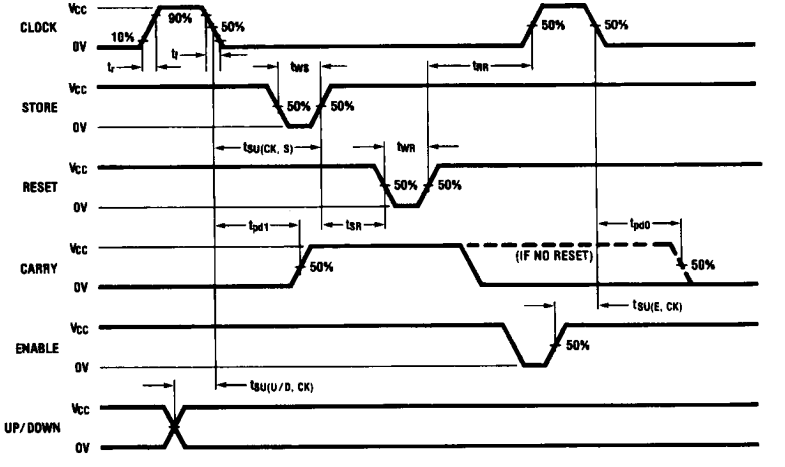
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Does not apply to backplane and oscillator pins.

Note 3: Display blanked. See Test Circuit.

Note 4: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

AC Waveforms



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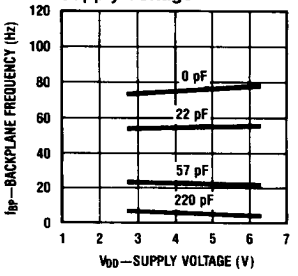
Typical Characteristics

Backplane Frequency as a Function of Supply Voltage



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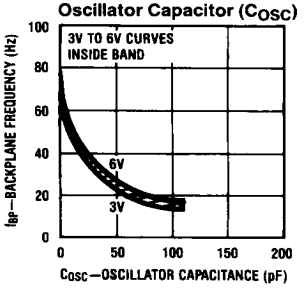
Backplane Frequency as a Function of Oscillator Capacitor (C_{OSC})



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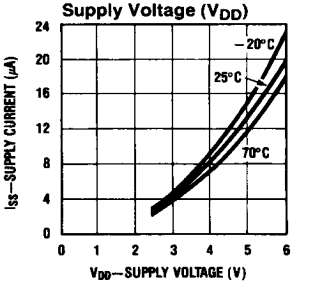
Operating Supply Current (I_{SS}) as a Function of Supply Voltage (V_{DD})



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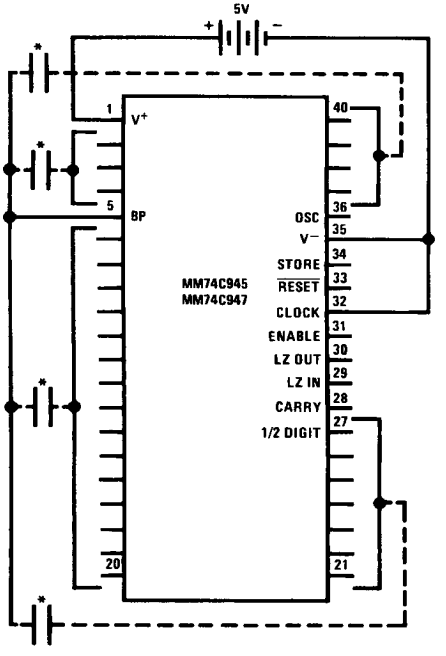
Test Circuit



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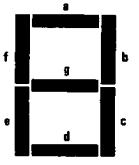
*Each segment to backlane with 200 pF capacitor.

Segment Identification



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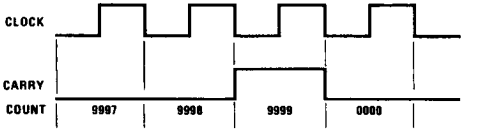
Timing Diagrams

Carry Out Timing (Up Mode)



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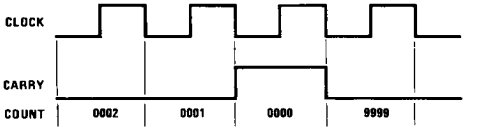
Carry Out Timing (Down Mode)



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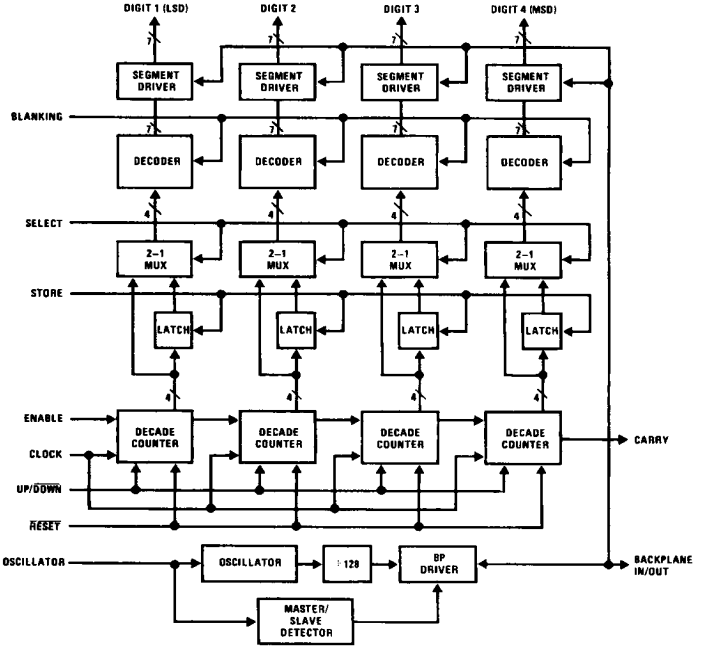
Block Diagrams

MM74C945



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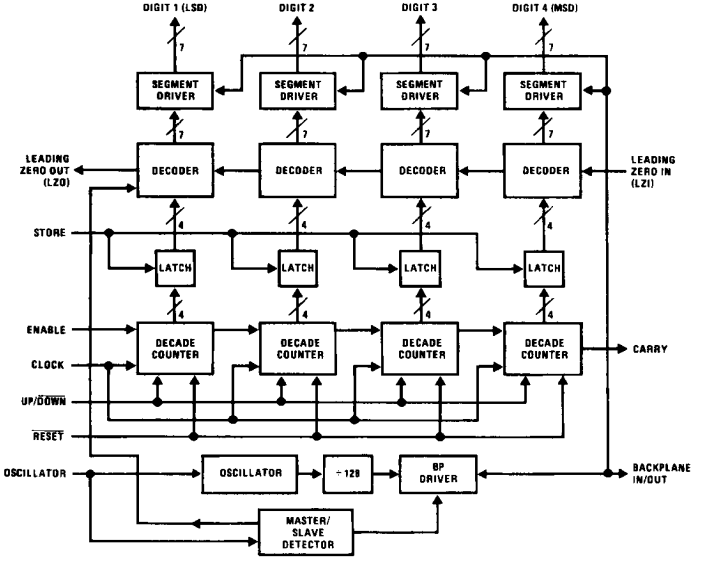
MM74C947



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Pin Description

Backplane In/Out—When the oscillator input is grounded this pin is an input allowing an external device to generate a backplane waveform. When the oscillator input is left open this pin is an output supplying backplane drive for the display.

Oscillator—The oscillator frequency may be lowered by tying a capacitor (C_{OSC}) to this pin. On the MM74C947, when the oscillator pin is open, the LSD is inhibited from blanking when leading zero blanking is enabled. If this pin is grounded, the backplanes on both parts become inputs, slaving the device to an external backplane.

Store—This input controls the on-chip latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high, the data on the counter outputs are stored in the latches.

$\overline{\text{Reset}}$—When low, counters are reset to zero.

Clock—Advances counters on negative edge.

Enable—When low, halts counter operation.

Leading Zero Input (LZI)—(MM74C947) When high, enables leading zero blanking.

Leading Zero Output (LZO)—(MM74C947) This output goes high when the latch contents equal zero, LZI is high and the oscillator pin is open.

Blanking—(MM74C945) When high, blanks display.

Select—(MM74C945) When high, the contents of the counter are displayed. When low, the contents of the latch are displayed.

Carry—This outputs goes high when 9999 is reached (up) or 0000 is reached (down).

Up/$\overline{\text{Down}}$—When high, the counter counts up. When low, the counter counts down.

A1–G1—Digit 1 segment outputs.

A2–G2—Digit 2 segment outputs.

A3–G3—Digit 3 segment outputs.

A4–G4—Digit 4 segment outputs.

Application Hints

DISPLAY CIRCUITRY DESCRIPTION

The MM74C945 and MM74C947 have 28 segment outputs capable of directly driving 4 digits of 7 segments. Both the segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life (i.e., DC offset voltage).

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. Several devices can then be driven by a single master backplane waveform which can be generated by another MM74C945, MM74C947 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven with several counters. The maximum fanout of a master backplane driver is limited by its total capacitive load, which is the sum of the slaved backplane input capacitances and the display backplane capacitance. (The MM74C947 oscillator pin controls the least significant digit blanking as well.)

An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency is typically 85 Hz, but may be lowered by connecting an external capacitor (C_{OSC}) between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane pin will be put in the slave (input) mode (see $V_{IH(OSC)}$ and $V_{IL(OSC)}$ specifications).

COUNTER CIRCUITRY DESCRIPTION

The MM74C945, MM74C947 are 4-decade up/down counters. The direction of the count is controlled by the up/$\overline{\text{down}}$ input. A high level on this pin causes the counter to count up. The counter advances on the negative clock edge. The carry output is high for one clock period during a count of 9999 in up mode, or during a count of 0000 in down mode. The carry is designed to allow cascading of several circuits in either ripple carry or synchronous modes.

Reset and Enable controls are provided to allow period and frequency measurements. The Reset control clears the counter when low and the Enable control disables counting when taken low.

The counter chain feeds a series of 4-bit flow-through latches. These latches enable the display to follow the counter when the Store input is low. When the Store pin is taken high the data on the counter outputs at this time become latched and the display will remain unchanged. (Assuming the latch display is selected on MM74C945.)

On the MM74C945 the latch outputs feed a multiplexer which selects either the latch outputs or counter outputs for display. This allows an intermediate count to be stored in the latches while the counter continues to be displayed. This is equivalent to a stopwatch lap feature.

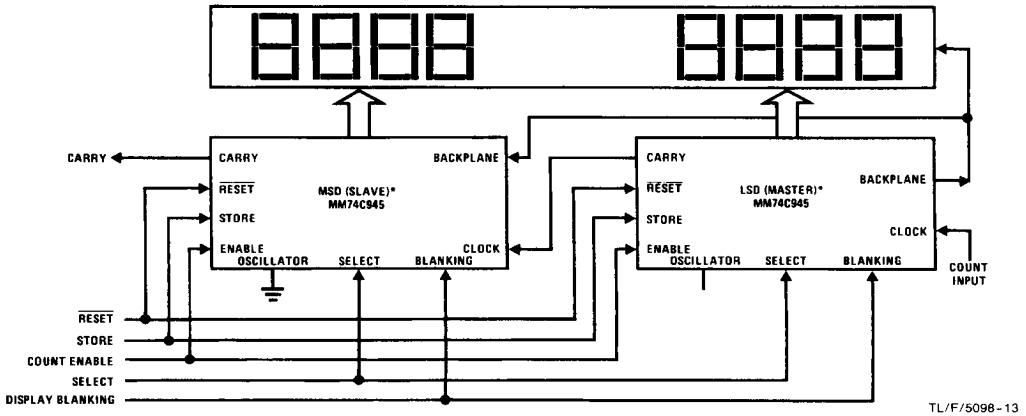
The output of the MM74C945's multiplexer feeds a decoder which converts 4-bit input to 7-segment outputs. A blanking control into these decoders blanks the display.

On the MM74C947 the latch outputs feed the decoders directly, but these decoders have a special ripple blanking capability that enables all leading zeroes except the least significant digit (LSD) to be blanked, even when counters are cascaded. Thus when the entire counter reads zero, instead of blanking all digits, the LSD will remain on. (When multiple counters are cascaded, all except the least significant counter will blank entirely on zeroes.) This feature is properly implemented by configuring the least significant device as the master (oscillator pin ungrounded) thereby inhibiting LSD blanking.

The outputs of the decoders for both devices control the segment drivers, which in turn enable display operation.

Typical Applications

Ripple Carry Cascading—MM74C945



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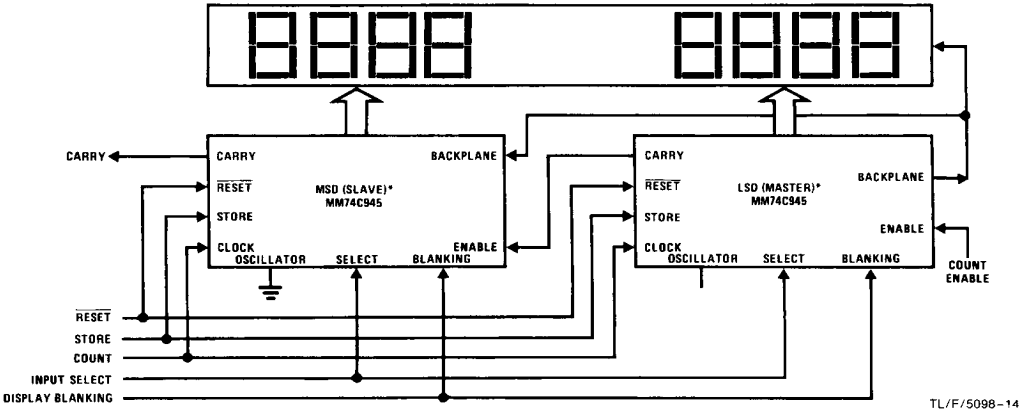
Synchronous Cascading—MM74C945



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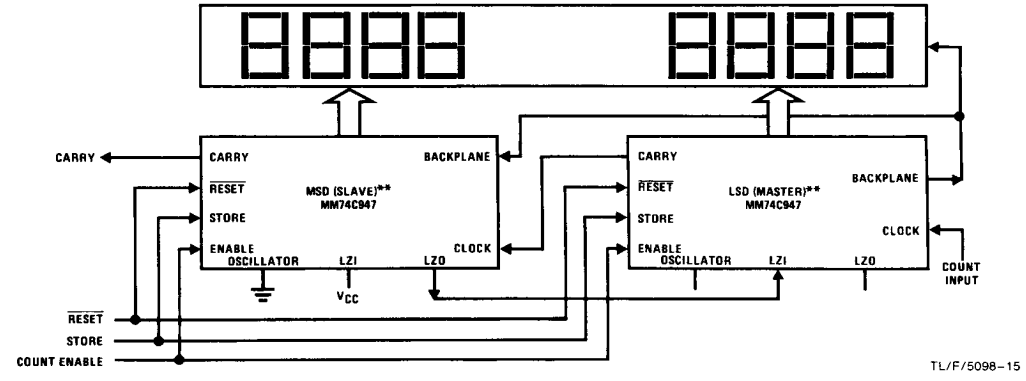
Ripple Cascading—MM74C947



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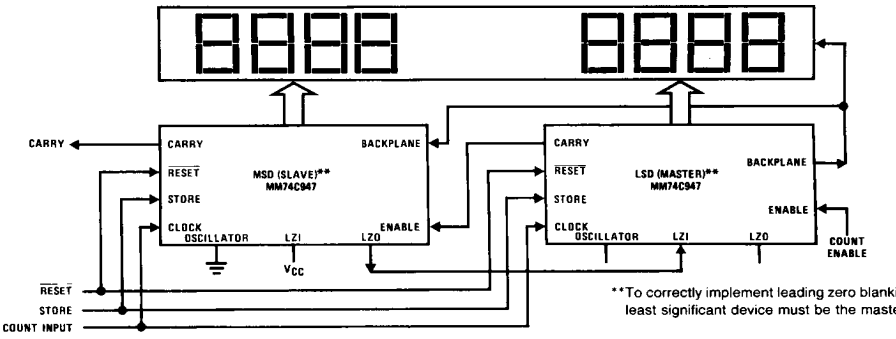
Typical Applications (Continued)

Synchronous Cascading—MM74C947



**To correctly implement leading zero blanking, the least significant device must be the master.

*Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

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