

# FSAV450

## 800MHz 4 Channel 2:1 Video Switch

### General Description

The FSAV450 is a high performance Quad SPDT (2-to-1 multiplexer/demultiplexer) video switch designed specifically for switching high definition YPbPr and computer RGB (up to UXGA) signals. The bandwidth of this device is 800MHz (Typ) which allows signals to pass with minimal edge and phase distortion. Image integrity is maintained with low crosstalk, high OFF-Isolation and low differential gain and phase. The low On Resistance ( $4\Omega$  typical) minimizes signal insertion loss. Low voltage operation (3V), low power consumption (1uA maximum) and small scale packaging (including leadless DQFN) make this device ideal for a broad range of applications.

### Features

- -50dB OFF Isolation at 30MHz
- -80dB non-adjacent channel crosstalk at 30MHz
- $4\Omega$  typical On Resistance ( $R_{ON}$ )
- -3dB bandwidth: 800MHz
- Low power consumption (1uA max)
- Control input: TTL compatible

### Applications

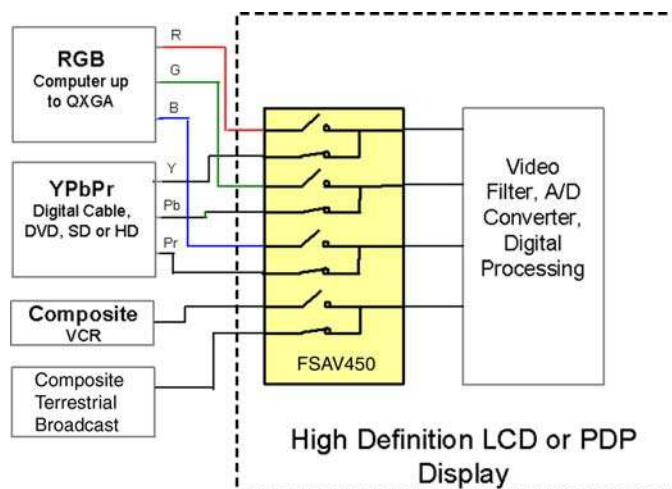
- RGB Video Switch in LCD, plasma and projector displays

### Ordering Code:

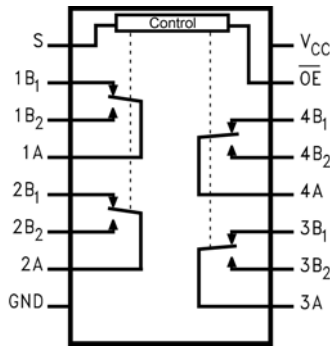
Order Number	Package Number	Package Description
FSAV450BQX (Note 1)	MLP016E	Pb-Free 16-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.5mm
FSAV450QSC	MQA16A	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FSAV450MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** DQFN package available in Tape and Reel only.

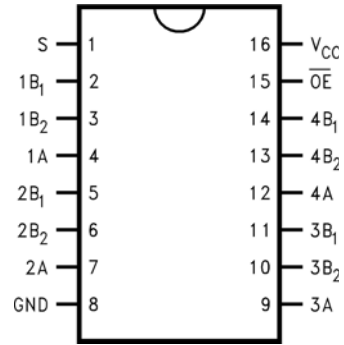


### Analog Symbol

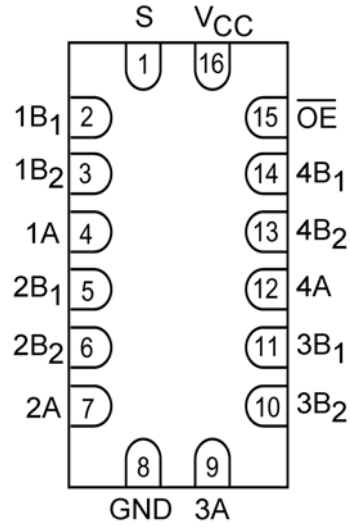


### Connection Diagrams

Pin Assignments for QSOP and TSSOP



Pad Assignments for DQFN (Preliminary)



### Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B <sub>1</sub> -B <sub>2</sub>	Bus B

### Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	A = B <sub>1</sub>
H	L	A = B <sub>2</sub>

## Absolute Maximum Ratings (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +6.0V
DC Switch Voltage ( $V_S$ )	-0.5V to +6.0V
DC Input Voltage ( $V_{IN}$ ) (Note 3)	-0.5V to +6.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output ( $I_{OUT}$ ) Sink Current	128 mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150 °C
ESD	
Human Body Model	2kV

## Recommended Operating Conditions

(Note 4)

Power Supply Operating ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Input Rise and Fall Time ( $t_r, t_f$ )	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature ( $T_A$ )	-40 °C to +85 °C

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

**Note 3:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 4:** Unused control inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$			Units	Conditions
			Min	Typ (Note 5)	Max		
	Analog Signal Range		0		2.0	V	
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18\text{ mA}$
$V_{IH}$	HIGH Level Input Voltage	4.5 to 5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.5 to 5.5			0.8	V	
$I_I$	Input Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq V_{IN} \leq 5.5V$
$I_{OFF}$	OFF-STATE Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 6)	4.5		4.0	6.0	$\Omega$	$V_{IN} = 1.0V$ $R_I = 75\ \Omega, I_{ON} = 13\text{ mA}$
		4.5		5.0	7.0	$\Omega$	$V_{IN} = 2.0V$ $R_I = 75\ \Omega, I_{ON} = 26\text{ mA}$
$I_{CC}$	Quiescent Supply Current	5.5			1.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	5.5			1.5	mA	One Input at 3.4V Other Inputs at $V_{CC}$ or GND

**Note 5:** Typical values are at  $T_A = +25^\circ\text{C}$

**Note 6:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Units	Conditions	Figure Number
			Min	Typ (Note 7)	Max			
t <sub>ON</sub>	Turn ON Time S-to-Bus B	4.5 to 5.5		4.0	6.0	ns	V <sub>B</sub> = 2.0V	Figures 8, 9
	Output Enable Time OE-to-A or B	4.5 to 5.5		3.5	5.5			
t <sub>OFF</sub>	Turn OFF Time S-to-Bus B	4.5 to 5.5		1.5	3.5	ns	V <sub>B</sub> = 2.0V	Figures 8, 9
	Output Disable Time OE-to-A or B	4.5 to 5.5		1.5	3.5			
DG	Differential Gain	4.5 to 5.5		0.2		%	R <sub>L</sub> = 75Ω, f = 3.58MHz	Figure 2
DP	Differential Phase	4.5 to 5.5		0.1		Degree	R <sub>L</sub> = 75Ω, f = 3.58MHz	Figure 3
O <sub>IRR</sub>	Non-Adjacent OFF-Isolation	4.5 to 5.5		-50.0		dB	f = 30MHz, R <sub>L</sub> = 75Ω	Figures 4, 10
X <sub>TALK</sub>	Non-Adjacent Channel Crosstalk	4.5 to 5.5		-80.0		dB	R <sub>L</sub> = 75Ω, f = 30MHz	Figures 5, 11
BW	-3dB Bandwidth	4.5 to 5.5		800		MHz	R <sub>L</sub> = 50Ω (DQFN)	Figures 1, 12
		4.5 to 5.5		700			R <sub>L</sub> = 50Ω (QSOP and TSSOP)	
		4.5 to 5.5		650			R <sub>L</sub> = 75Ω (DQFN)	
		4.5 to 5.5		600			R <sub>L</sub> = 75Ω (QSOP and TSSOP)	

Note 7: Typical values are at V<sub>CC</sub> = 5.0V and T<sub>A</sub> = +25°C

## Capacitance

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C		Units	Conditions
		Min	Typ		
C <sub>IN</sub>	Control Pin Input Capacitance		3.0	pF	V <sub>CC</sub> = 0V
C <sub>ON</sub>	A/B ON Capacitance		8.5	pF	V <sub>CC</sub> = 5.0V, $\overline{OE}$ = 0V
C <sub>OFF</sub>	Port B OFF Capacitance		3.0	pF	V <sub>CC</sub> and $\overline{OE}$ = 5.0V

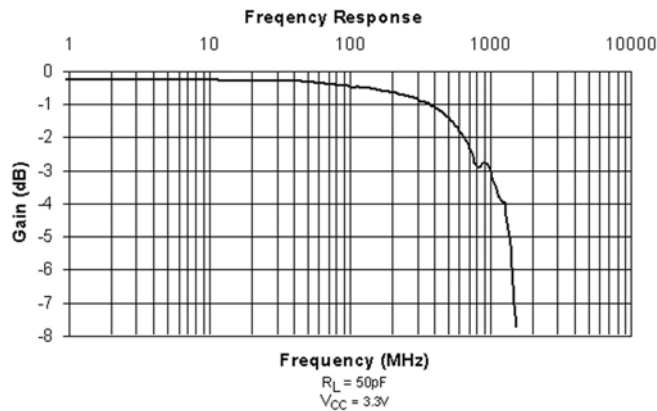


FIGURE 1. Gain vs. Frequency

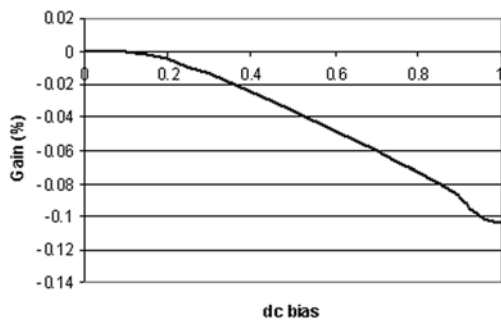


FIGURE 2. Differential Gain vs. dc bias

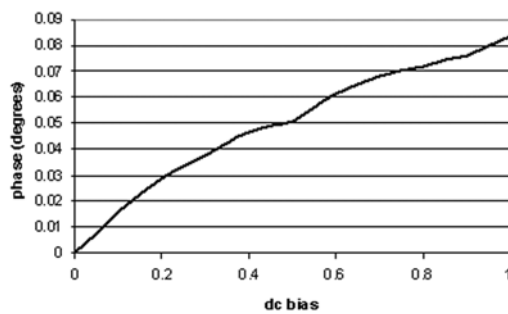


FIGURE 3. Differential Phase vs. dc bias

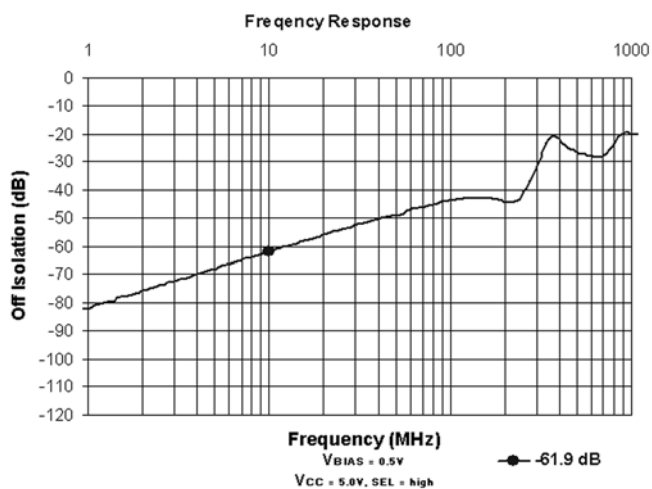


FIGURE 4. OFF Isolation

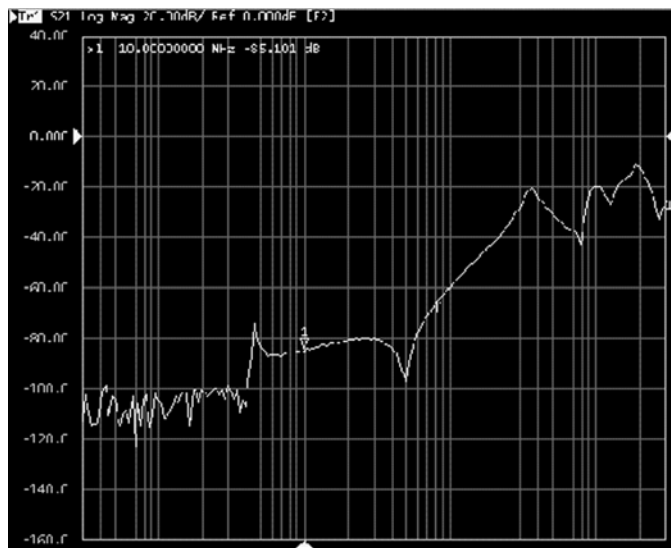


FIGURE 5. OFF Crosstalk vs. Frequency

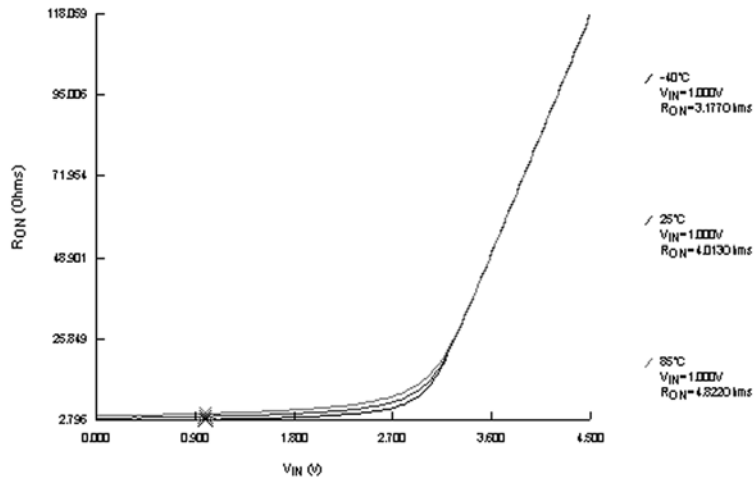


FIGURE 6.  $R_{ON}$  Switch On Resistance,  $I_{ON} = 13mA$

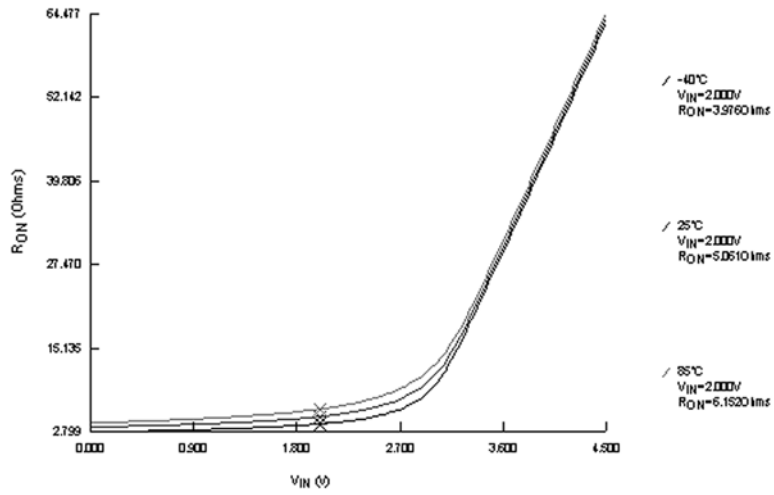
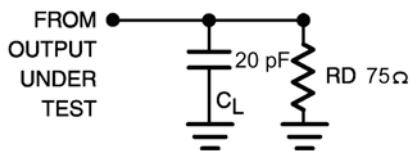


FIGURE 7.  $R_{ON}$  Switch On Resistance,  $I_{ON} = 26mA$

## AC Loading and Waveforms



Note: Input driven by 50  $\Omega$  source terminated in 50  $\Omega$

Note:  $C_L$  includes load and stray capacitance

Note: Input PRR = 1.0 MHz,  $t_{IV} = 500$  ns

FIGURE 8. AC Test Circuit

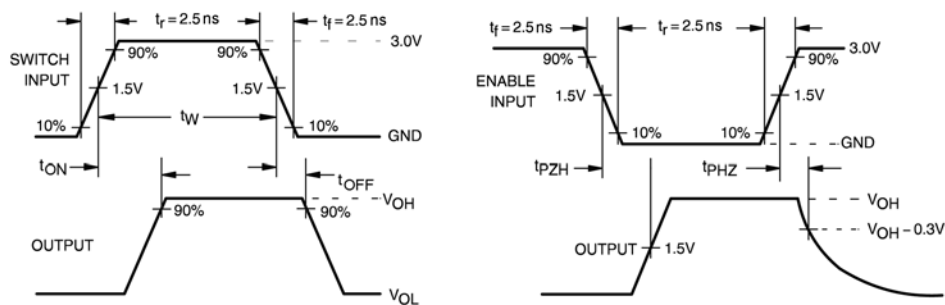


FIGURE 9. AC Waveforms

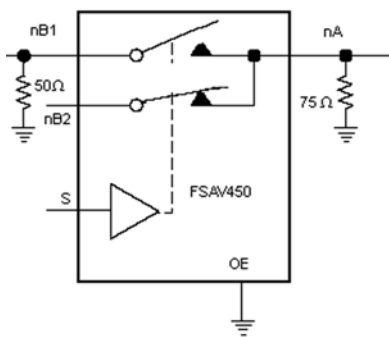


FIGURE 10. OFF Isolation Test

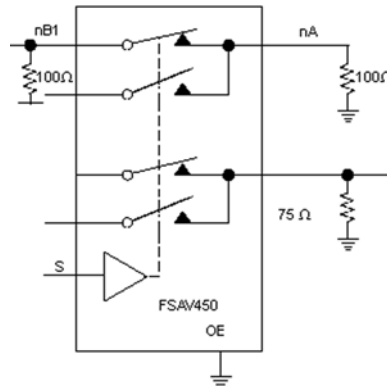


FIGURE 11. Crosstalk Test

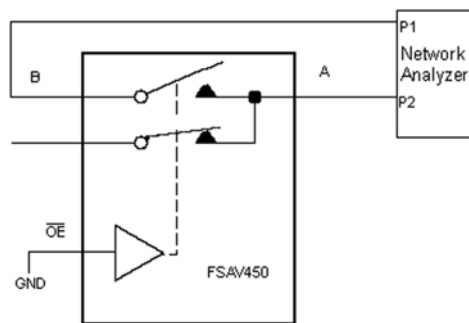


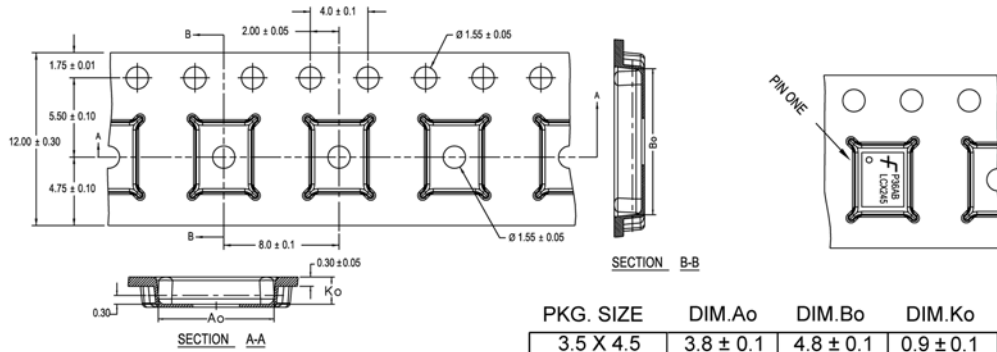
FIGURE 12. Bandwidth Test

## Tape and Reel Specification

TAPE FORMAT for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



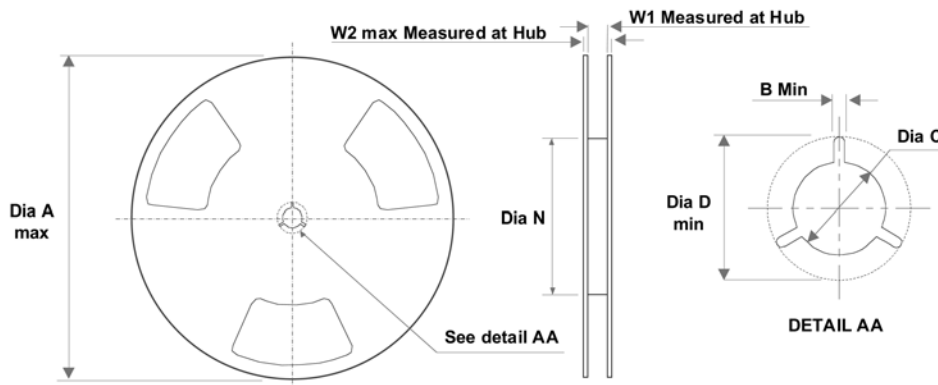
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

REEL DIMENSIONS inches (millimeters)

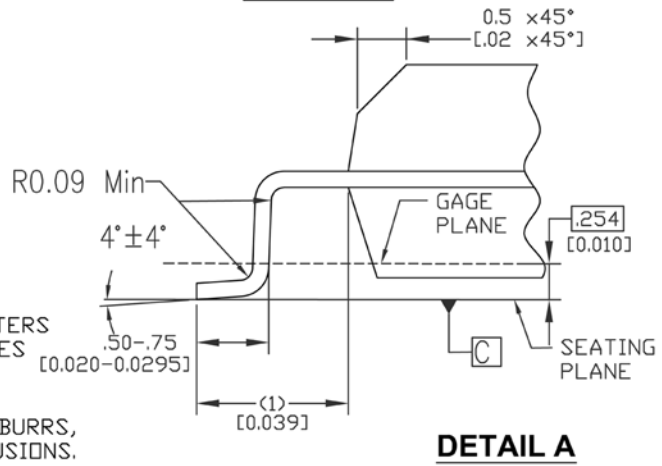
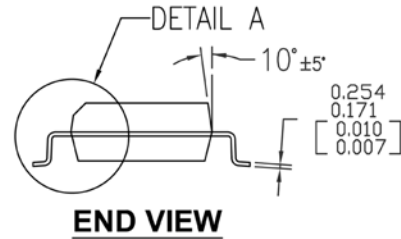
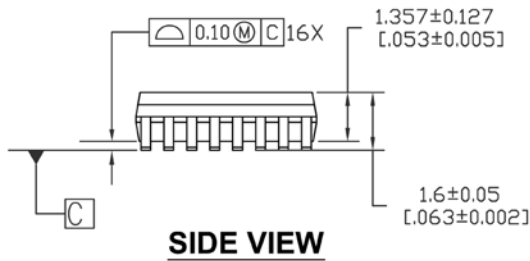
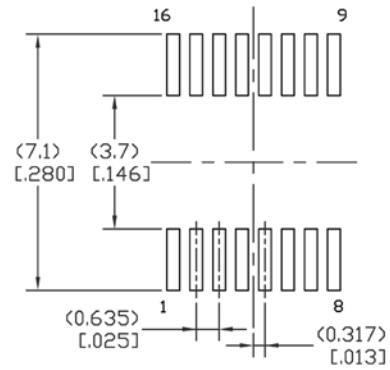
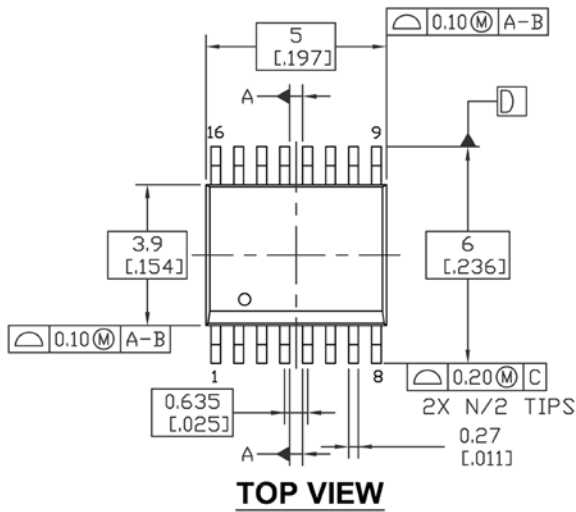


Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)





**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



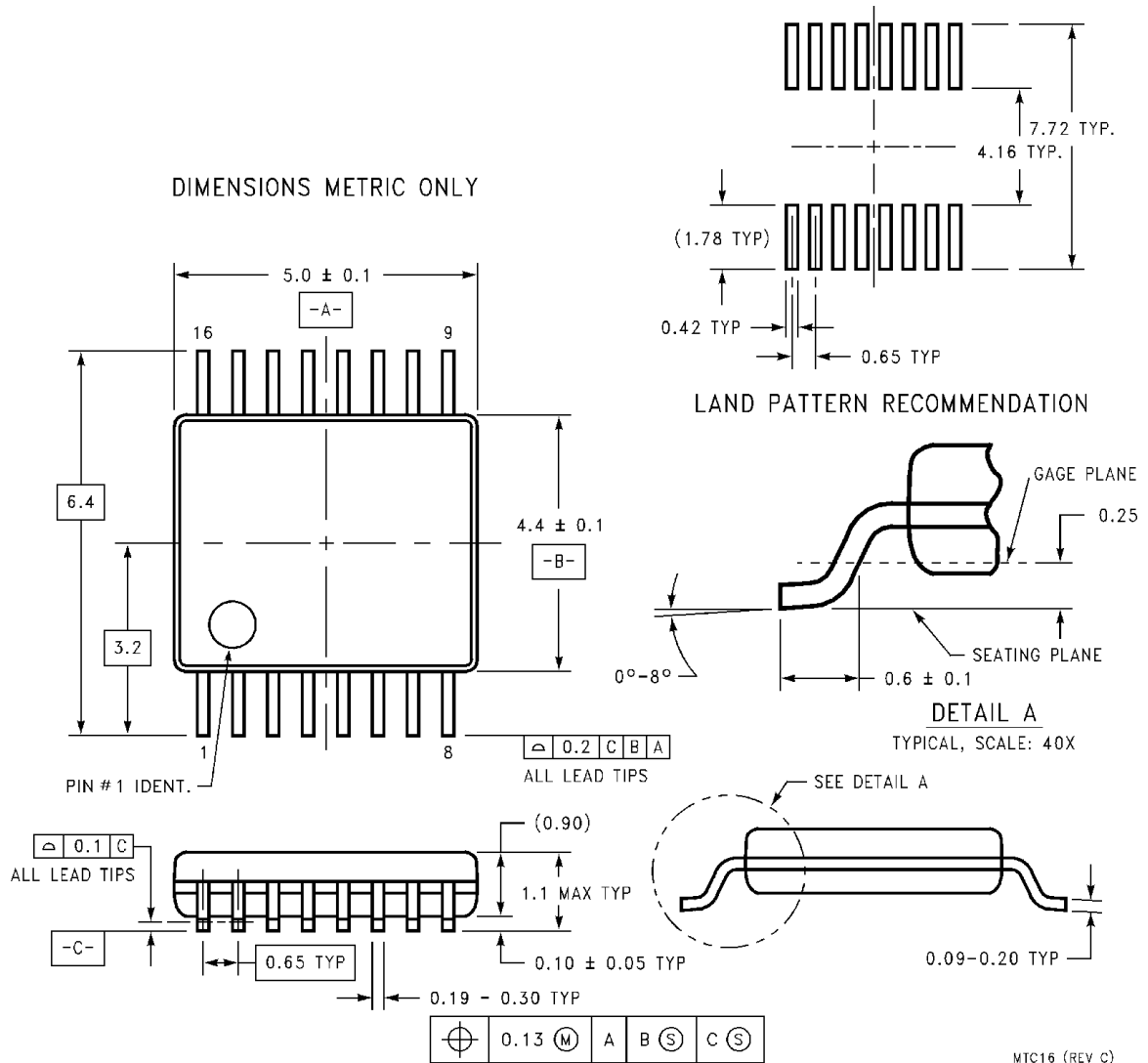
NOTES :

- A. THIS PACKAGE CONFORMS TO JEDEC MO-137 VARIATION AB
- B. PRIMARY DIMENSIONS IN MILLIMETERS  
REFERENCE DIMENSIONS IN INCHES
- C. DRAWING CONFORMS TO ASME Y14.5M-1994
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MQA16AREVB

**16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide  
Package Number MQA16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

Definition of terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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