

## MAT-04

### FEATURES

- Low Offset Voltage ..... 200 $\mu$ V Max
- High Current Gain ..... 400 Min
- Excellent Current Gain Match ..... 2% Max
- Low Noise Voltage at 100Hz, 1mA ..... 2.5nV/  $\sqrt{\text{Hz}}$  Max
- Excellent Log Conformance .....  $r_{BE} = 0.6\Omega$  Max
- Matching Guaranteed for All Transistors
- Available in Die Form

### ORDERING INFORMATION <sup>†</sup>

$T_A = +25^\circ\text{C}$ $V_{OS}$ MAX ( $\mu\text{V}$ )	PACKAGE		OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC 14-PIN	
200	MAT04AY*	—	MIL
200	MAT04EY	—	IND
400	MAT04BY*	—	MIL
400	MAT04FY	MAT04FP	XIND
400	—	MAT04FS <sup>††</sup>	XIND

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

<sup>†</sup> Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

<sup>††</sup> For availability and burn-in information on SO and PLCC packages, contact your local sales office.

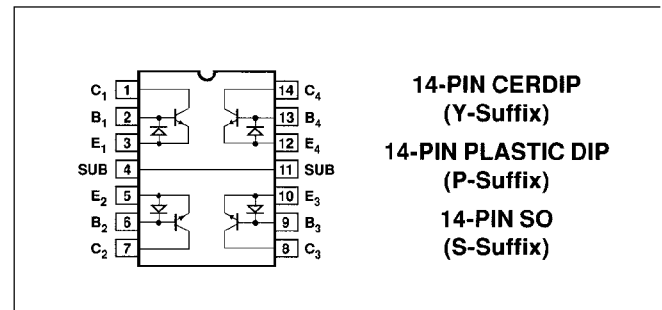
### GENERAL DESCRIPTION

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and non-linear circuit applications. Performance characteristics of the MAT-04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5nV/ $\sqrt{\text{Hz}}$  maximum at 100Hz,  $I_C = 1 \text{ mA}$ ) and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 200 $\mu\text{V}$  and tight current gain matching, to within 2%. Each transistor of the MAT-04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT-04 makes it an excellent choice for use in log and antilog circuits. The MAT-04 is an ideal choice in applications where low noise and high gain are required.

### PIN CONNECTIONS



14-PIN CERDIP  
(Y-Suffix)

14-PIN PLASTIC DIP  
(P-Suffix)

14-PIN SO  
(S-Suffix)

### ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage ( $BV_{CBO}$ )	40V
Collector-Emitter Voltage ( $BV_{CEO}$ )	40V
Collector-Collector Voltage ( $BV_{CC}$ )	40V
Emitter-Emitter Voltage ( $BV_{EE}$ )	40V
Collector Current	30mA
Emitter Current	30mA
Substrate (Pin-4 to Pin-11) Current	30mA
Operating Temperature Range	
MAT-04AY, BY	-55°C TO +125°C
MAT-04EY	-25°C TO +85°C
MAT-04FY,FP,FS	-40°C to +85°C
Storage Temperature	
Y Package	-65°C to +150°C
P Package	-65°C to +125°C
Lead Temperature (Soldering, 60 sec)	+300°C

PACKAGE TYPE	$\theta_{JA}$ (Note 2)	$\theta_{JC}$	UNITS
14-Pin CERDIP (Y)	108	16	$^\circ\text{C/W}$
14-Pin Plastic DIP (P)	83	39	$^\circ\text{C/W}$
14-Pin SO (S)	120	36	$^\circ\text{C/W}$

### NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for CerDIP and P-DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

# MAT-04

**ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$  unless otherwise noted. Each transistor is individually tested. For matching parameters ( $V_{OS}$ ,  $I_{OS}$ ,  $\Delta h_{FE}$ ) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04A/E			MAT-04B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	$h_{FE}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	400	800	—	300	600	—	
Current Gain Match	$\Delta h_{FE}$	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 2)	—	0.5	2	—	1	4	%
Offset Voltage	$V_{OS}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 4)	—	50	200	—	100	400	$\mu\text{V}$
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0\text{V}$ (Note 4)	—	5	25	—	10	50	$\mu\text{V}$
Offset Voltage Change vs $V_{CB}$	$\Delta V_{OS}/\Delta V_{CB}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 4)	—	50	100	—	100	200	$\mu\text{V}$
Bulk Emitter Resistance	$r_{BE}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0\text{V}$ (Note 5)	—	0.4	0.6	—	0.4	0.6	$\Omega$
Input Bias Current	$I_B$	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	125	250	—	165	330	nA
Input Offset Current	$I_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	0.6	5	—	2	13	nA
Breakdown Voltage	$BV_{CEO}$	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\mu\text{A}$ $I_C = 1\text{mA}$	—	0.03	0.06	—	0.03	0.06	V
Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = 40\text{V}$	—	5	—	—	5	—	pA
Noise Voltage Density	$e_n$	$V_{CB} = 0\text{V}$ $f_O = 10\text{Hz}$ $I_C = 1\text{mA}$ $f_O = 100\text{Hz}$ (Note 3) $f_O = 1\text{kHz}$	—	2	3	—	2	4	$\text{nV}/\sqrt{\text{Hz}}$
Gain Bandwidth Product	$f_T$	$I_C = 1\text{mA}$ $V_{CE} = 10\text{V}$	—	300	—	—	300	—	MHz
Output Capacitance	$C_{OBO}$	$V_{CB} = 15\text{V}$ $I_E = 0$ $f = 1\text{MHz}$	—	10	—	—	10	—	pF
Input Capacitance	$C_{EBO}$	$V_{BE} = 0\text{V}$ $I_C = 0$ $f = 1\text{MHz}$	—	40	—	—	40	—	pF

## NOTES:

- Current gain measured at  $I_C = 10\mu\text{A}$ ,  $100\mu\text{A}$  and  $1\text{mA}$ .
- Current gain match is defined as:  $\Delta h_{FE} = \frac{100 (\Delta I_B) (h_{FE} \text{ min})}{I_C}$
- Sample tested.
- Measured at  $I_C = 10\mu\text{A}$  and guaranteed by design over the specified range of  $I_C$ .
- Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at  $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  for MAT-04E,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  for MAT-04F, unless otherwise noted. Each transistor is individually tested. For matching parameters ( $V_{OS}$ ,  $I_{OS}$ ) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04E			MAT-04F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	$h_{FE}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	225	625	—	200	500	—	
Offset Voltage	$V_{OS}$	$10\mu\text{A} \leq I_C < 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 3)	—	60	260	—	120	520	$\mu\text{V}$
Average Offset Voltage Drift	$TCV_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$ (Note 2)	—	0.2	1	—	0.4	2	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	$I_B$	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	160	445	—	200	500	nA
Input Offset Current	$I_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	4	20	—	8	40	nA
Average Offset Current Drift	$TCI_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	50	—	—	100	—	$\text{pA}/^{\circ}\text{C}$
Breakdown Voltage	$BV_{CEO}$	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = 40\text{V}$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	$I_{CES}$	$V_{CE} = 40\text{V}$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	$I_{CS}$	$V_{CS} = 40\text{V}$	—	0.7	—	—	0.7	—	nA

**ELECTRICAL CHARACTERISTICS** at  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise noted. Each transistor is individually tested. For matching parameters ( $V_{OS}$ ,  $I_{OS}$ ) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

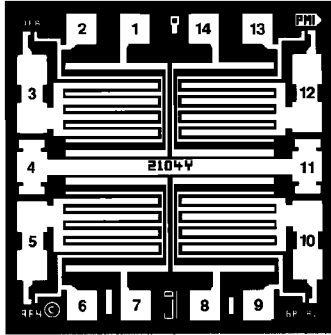
PARAMETER	SYMBOL	CONDITIONS	MAT-04A			MAT-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	$h_{FE}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	175	475	—	125	425	—	
Offset Voltage	$V_{OS}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 3)	—	70	300	—	140	600	$\mu\text{V}$
Average Offset Voltage Drift	$TCV_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$ (Note 2)	—	0.2	1	—	0.4	2	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	$I_B$	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	210	570	—	235	800	nA
Input Offset Current	$I_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	6	30	—	12	60	nA
Average Offset Current Drift	$TCI_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	50	—	—	100	—	$\text{pA}/^{\circ}\text{C}$
Breakdown Voltage	$BV_{CEO}$	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = 40\text{V}$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	$I_{CES}$	$V_{CE} = 40\text{V}$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	$I_{CS}$	$V_{CS} = 40\text{V}$	—	7	—	—	7	—	nA

**NOTES:**

- Current gain measured at  $I_C = 10\mu\text{A}$ ,  $100\mu\text{A}$  and  $1\text{mA}$ .
- Guaranteed by  $V_{OS}$  test ( $TCV_{OS} \leq V_{OS}/T$  for  $V_{OS} \ll V_{BE}$ )  $T = 298^{\circ}\text{K}$  for  $T_A = 25^{\circ}\text{C}$ .
- Measured at  $I_C = 10\mu\text{A}$  and guaranteed by design over the specified range of  $I_C$ .

# MAT-04

## DICE CHARACTERISTICS



1. Q<sub>1</sub> COLLECTOR
2. Q<sub>1</sub> BASE
3. Q<sub>1</sub> EMITTER
4. SUBSTRATE
5. Q<sub>2</sub> EMITTER
6. Q<sub>2</sub> BASE
7. Q<sub>2</sub> COLLECTOR
8. Q<sub>3</sub> COLLECTOR
9. Q<sub>3</sub> BASE
10. Q<sub>3</sub> EMITTER
11. SUBSTRATE
12. Q<sub>4</sub> EMITTER
13. Q<sub>4</sub> BASE
14. Q<sub>4</sub> COLLECTOR

DIE SIZE 0.060 x 0.060 inch, 3600 sq. mils  
(1.52 x 1.52 mm, 2.31 sq. mm)

**WAFER TEST LIMITS** at  $T_A = +25^\circ\text{C}$  unless otherwise noted. Each transistor is individually tested. For matching parameters ( $V_{OS}$ ,  $I_{OS}$ ,  $\Delta h_{FE}$ ) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

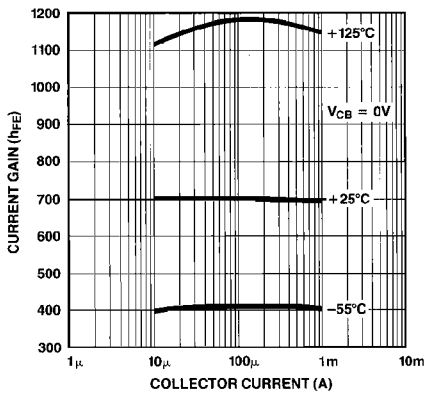
PARAMETER	SYMBOL	CONDITIONS	MAT-04N LIMITS	UNITS
Current Gain	$h_{FE}$	$I_C = 100\mu\text{A}$ $0V \leq V_{CB} \leq 30V$	300	MIN
Current Gain Match	$\Delta h_{FE}$	$I_C = 100\mu\text{A}$ , $V_{CB} = 0V$	4	% MAX
Offset Voltage	$V_{OS}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0V \leq V_{CB} \leq 30V$ (Note 1)	400	$\mu\text{V}$ MAX
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0V$ (Note 1)	50	$\mu\text{V}$ MAX
Offset Voltage Change us VCB	$\Delta V_{OS}/\Delta V_{CB}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0V \leq V_{CB} \leq 30V$ (Note 1)	200	$\mu\text{V}$ MAX
Bulk Emitter Resistance	$r_{BE}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0V$ (Note 2)	0.6	$\Omega$ MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\mu\text{A}$ $I_C = 1\text{mA}$	0.06	V MAX
Input Bias Current	$I_B$	$I_C = 100\mu\text{A}$ $0V \leq V_{CB} \leq 30V$	330	nA MAX
Input Offset Current	$I_{OS}$	$I_C = 100\mu\text{A}$ $V_{CB} = 0V$	13	nA MAX
Breakdown Voltage	$BV_{CEO}$	$I_C = 10\mu\text{A}$	40	V MIN

**NOTE:**

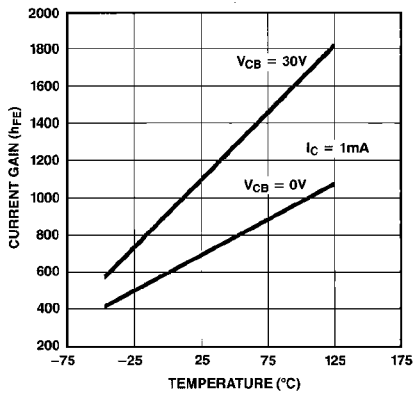
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

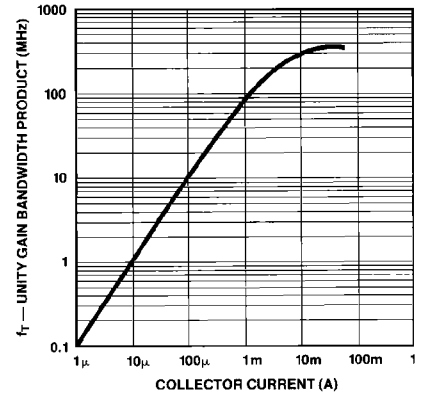
**CURRENT GAIN vs COLLECTOR CURRENT**



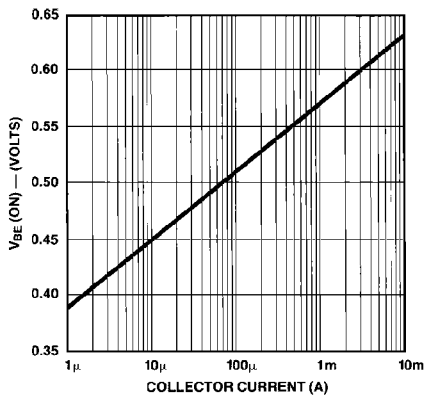
**CURRENT GAIN vs TEMPERATURE**



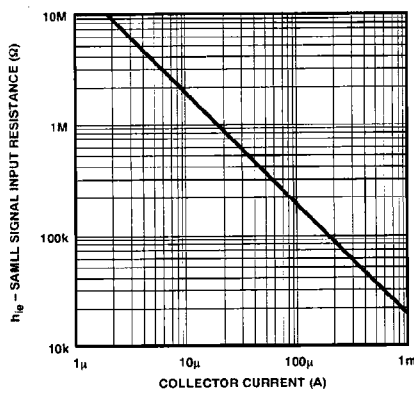
**GAIN BANDWIDTH vs COLLECTOR CURRENT**



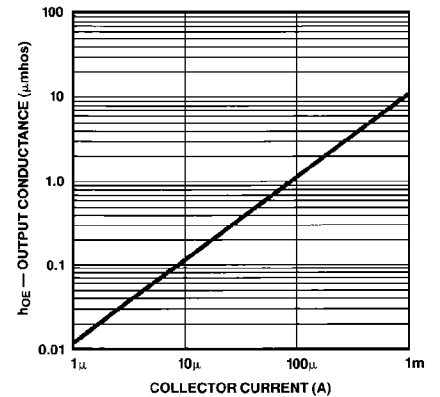
**BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT**



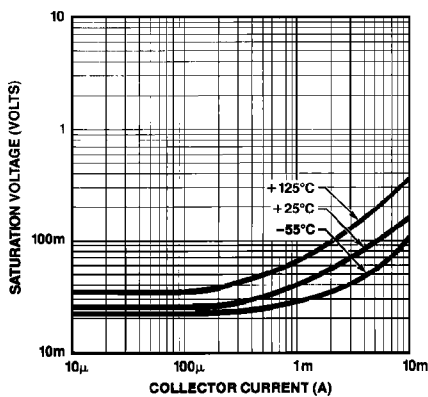
**SMALL SIGNAL INPUT RESISTANCE ( $h_{ie}$ ) vs COLLECTOR CURRENT**



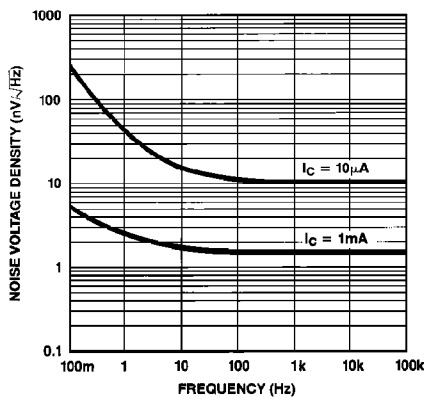
**SMALL SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT**



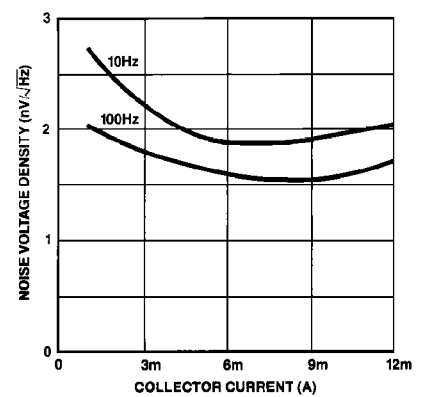
**SATURATION VOLTAGE vs COLLECTOR CURRENT**



**NOISE VOLTAGE DENSITY vs FREQUENCY**

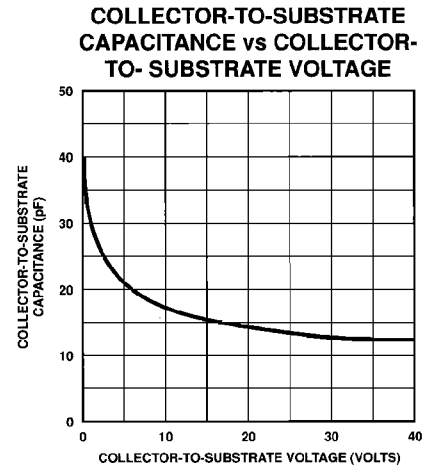
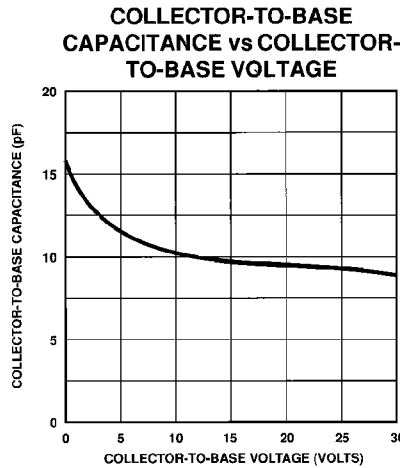
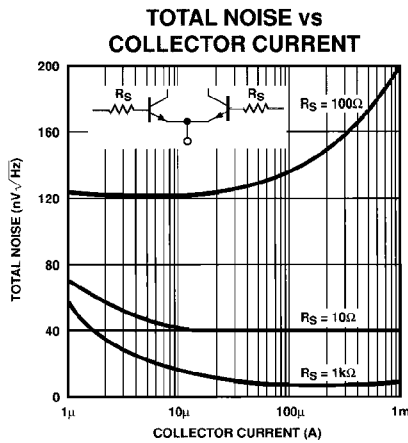


**NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT**



# MAT-04

## TYPICAL PERFORMANCE CHARACTERISTICS *Continued*



### APPLICATION NOTES

It is recommended that one of the substrate pins (Pins 4 and 11) be tied to the most negative circuit potential to minimize coupling between devices. Pins 4 and 11 are internally connected.

### APPLICATIONS

#### CURRENT SOURCES

The MAT-04 can be used to implement a variety of high impedance current mirrors as shown in Figures 1, 2, and 3. These current mirrors can be used as biasing elements and load devices for amplifier stages.

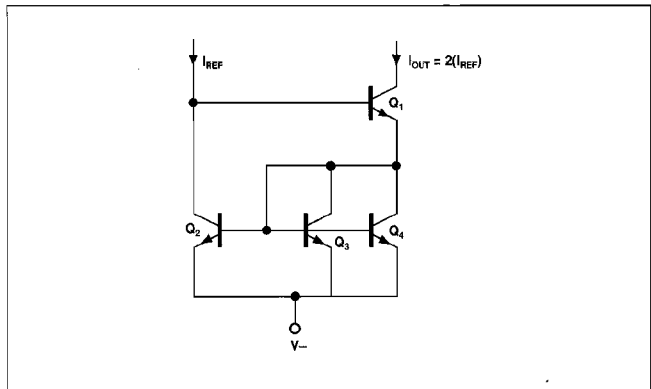


FIGURE 2: Current Mirror,  $I_{OUT} = 2(I_{REF})$

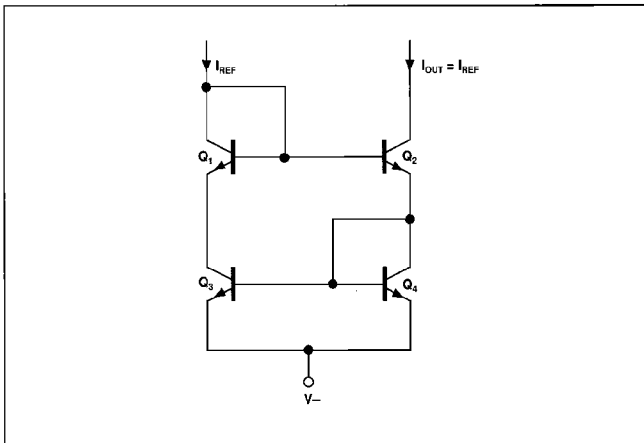


FIGURE 1: Unity Gain Current Mirror,  $I_{OUT} = I_{REF}$

The unity-gain current mirror of Figure 1, using a MAT-04AY, has an accuracy of better than 1% and an output impedance of over  $100M\Omega$  at  $100\mu A$ . Figures 2 and 3 show modified current mirrors designed for a current gain of two, and one-half respectively. The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but is still better than 2%.

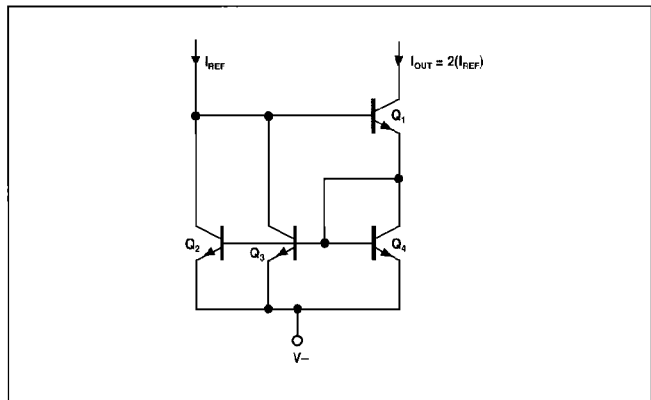
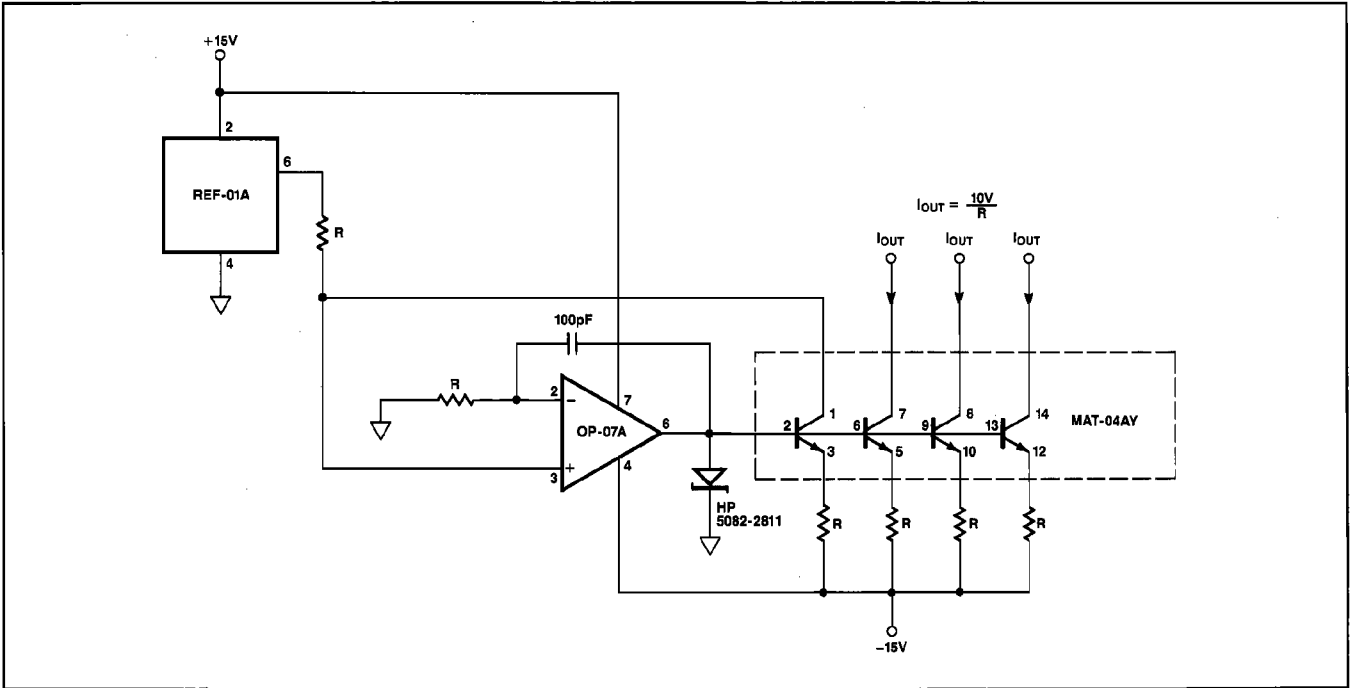


FIGURE 2: Current Mirror,  $I_{OUT} = 2(I_{REF})$

Figure 4 is a temperature independent current sink that has an accuracy of better than 1% over the military temperature range at an output current of  $100\mu A$  to 1 mA. The Schottky diode acts as a clamp to insure correct circuit start-up at power on. The resistors used in this circuit should be 1% metal-film type.

FIGURE 4: Temperature Independent Current Sink,  $I_{OUT} = 10V/R\Omega$



**NONLINEAR FUNCTIONS**

An application where precision matched-transistors are a powerful tool is in the generation of nonlinear functions. These circuits are based on the transistor's logarithmic property which takes the following idealized form:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$$

The MAT-04, with its excellent logarithmic conformance, maintains this idealized function over many decades of collector current. This, in addition to the stringent parametric matching of the MAT-04, enables the implementation of extremely accurate log/antilog circuits.

The circuit of Figure 5 is a vector summer that adds and subtracts logged inputs to generate the following transfer function:

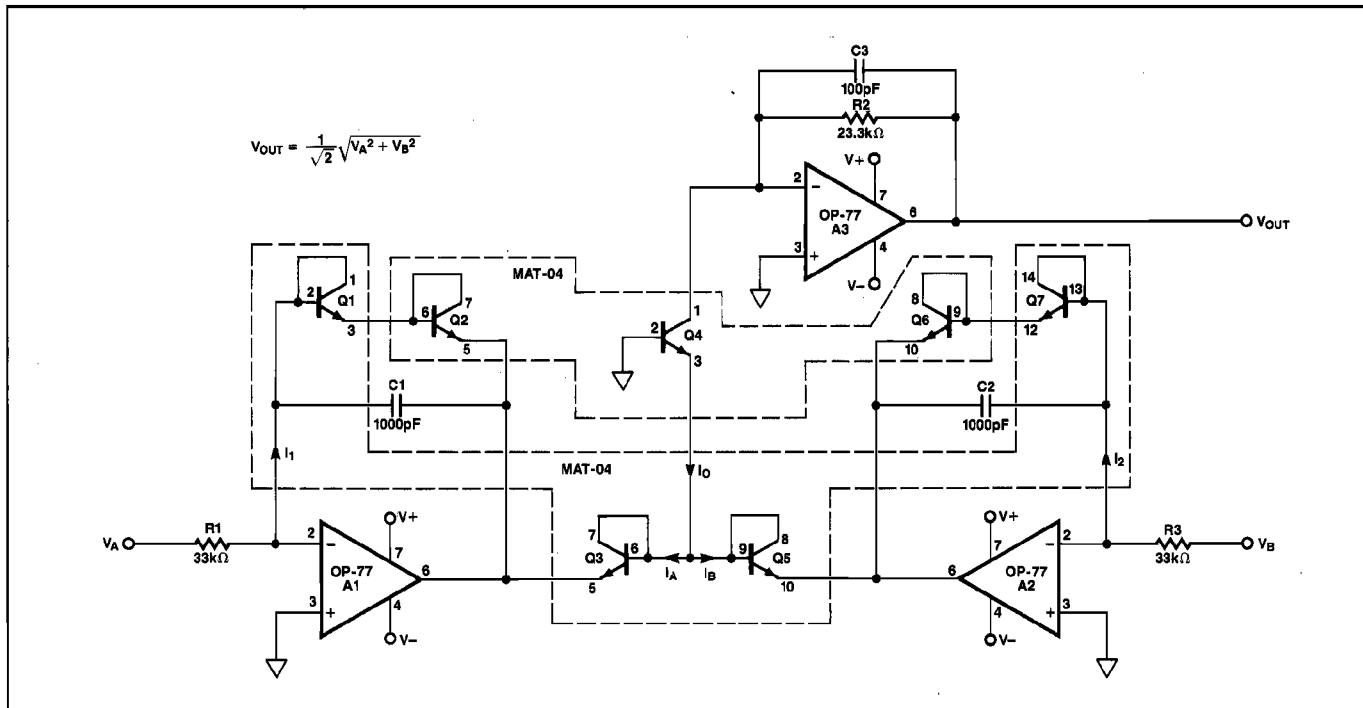
$$V_{OUT} = \frac{1}{\sqrt{2}} \sqrt{V_A^2 + V_B^2}$$

This circuit uses two MAT-04AYs and maintains an accuracy of better than 0.5% over an input range of 10mV to 10V. The layout of the MAT-04s reduces errors due to matching and temperature differences between the two precision quad matched-transistors.

Op amps A1 and A2 translate the input voltages into logarithmic valued currents ( $I_A$  and  $I_B$  in Figure 5) that flow through transistor  $Q_3$  and  $Q_5$ . These currents are summed by transistor  $Q_4$  ( $I_O = I_A + I_B = \sqrt{I_1^2 + I_2^2}$ ) which feeds the current-to-voltage converter consisting of op amp A3. To maintain accuracy, 1% metal-film resistors should be used.

# MAT-04

FIGURE 5: Vector Summer



## LOW NOISE, HIGH SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 is a very low noise, high speed amplifier, ideal for use in precision transducer and professional audio applications. The performance of the amplifier is summarized in Table I. Figure 7 shows the input referred spot noise over the 0-25kHz bandwidth to be flat at 1.2nV/√Hz. Figure 8 highlights the low 1/f noise corner at 2Hz.

The circuit uses a high speed op amp, the OP-17, preceded by an input amplifier. This consists of a precision dual matched-transistor, the MAT-02, and a feedback V-to-I converter, the MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" which performs the voltage-to-current conversion. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistors R1, R2, and R3, R4 form voltage dividers that attenuate the output voltage swing since the "cross quad" arrangement has a limited input range. Biasing for the input stage is set by zener diode Z1. At low currents the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of 530μA per side for the input stage. The gain of this amplifier with the values shown in Figure 6 is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{33000}{R_G}$$

TABLE I: Instrumentation Amplifier Characteristics

Input Noise Voltage Density	G = 1000	1.2nV/√Hz
	G = 100	3.6nV/√Hz
	G = 10	30nV/√Hz
Bandwidth	G = 500	400kHz
	G = 100	1MHz
	G = 10	1.2MHz
Slew Rate		40V/μs
Common-Mode Rejection	G = 1000	130dB
	G = 100	
Distortion	G = 100	0.03%
	f = 20Hz to 20kHz	
Settling Time	G = 1000	10μs
Power Consumption		350mW



FIGURE 6: Low Noise, High Speed Instrumentation Amplifier

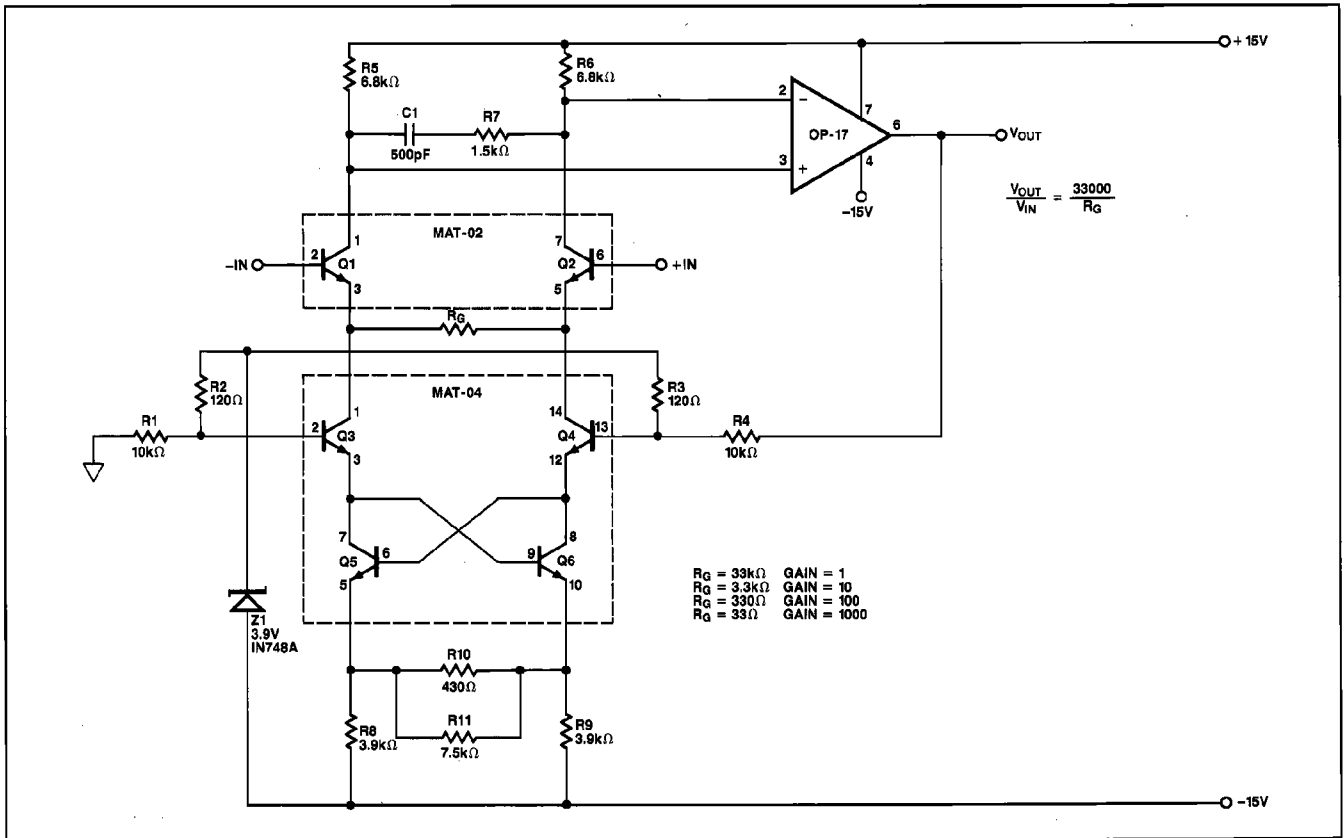


FIGURE 7: Spot Noise of the Instrumentation Amplifier from 0-25kHz at a Gain of 1000

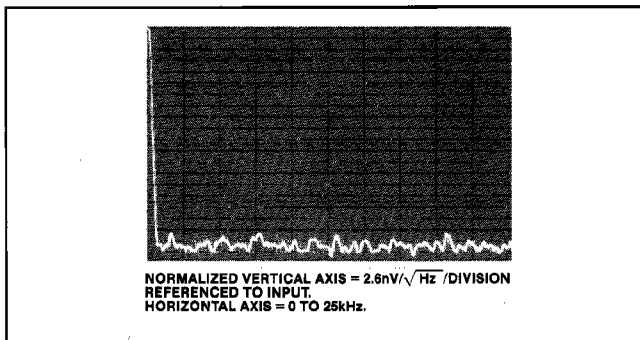
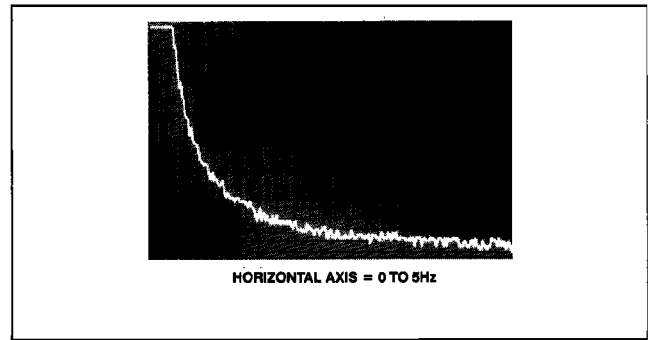
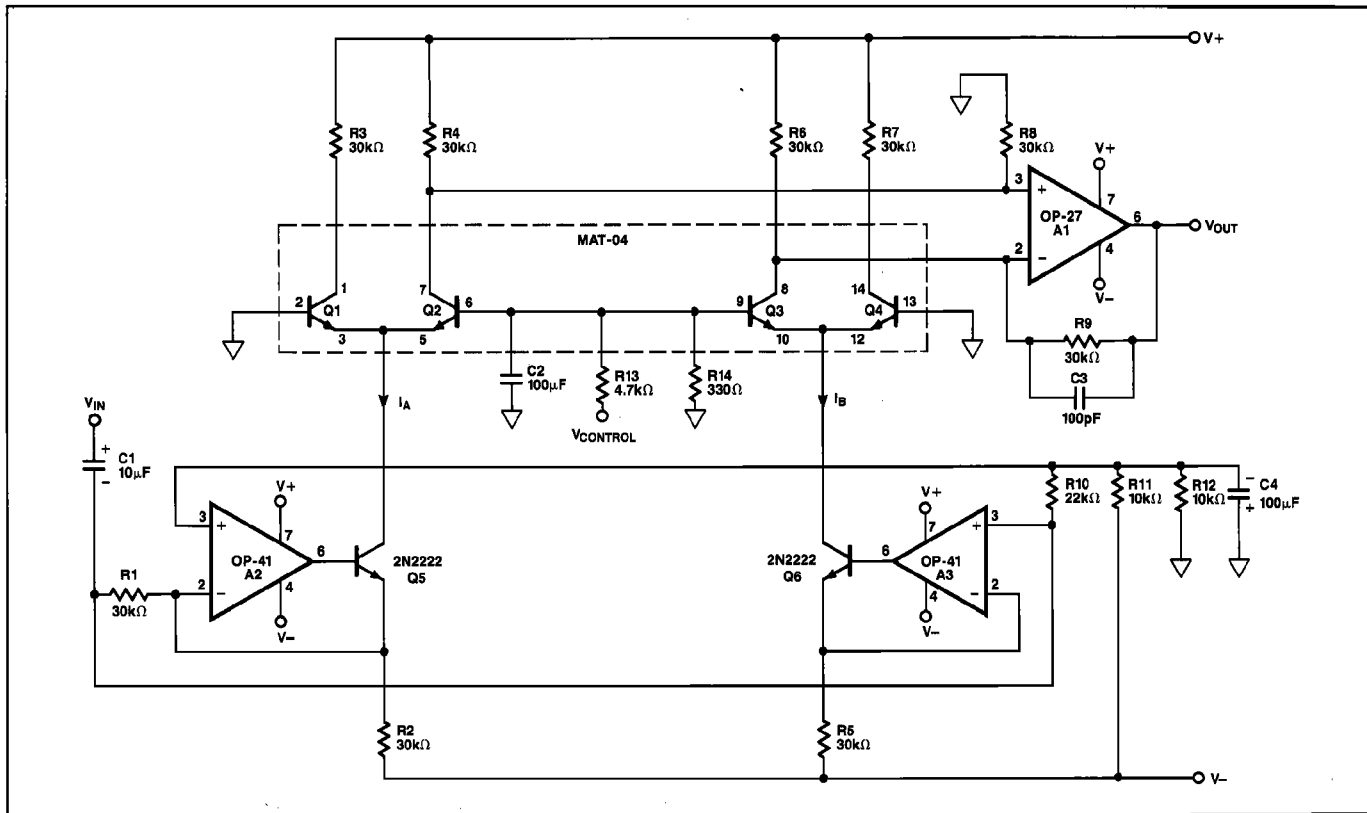


FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner. Gain = 1000.



# MAT-04

FIGURE 9: Voltage-Controlled Attenuator



## VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator (VCA) of Figure 9, widely used in professional audio circles, can easily be implemented using a MAT-04. The excellent matching characteristics of the MAT-04 enables the VCA to have a distortion level of under 0.03% over a wide range of control voltages. The VCA accepts a 3V RMS input and easily handles the full 20Hz-20kHz audio bandwidth as shown in Figure 10. Noise level for the VCA is more than 110dB below maximum output.

In the voltage-controlled attenuator, the input signal modulates the stage current of each differential pair. Op amps A2 and A3 in conjunction with transistors Q5 and Q6 form voltage-to-current converters that transform a single input voltage into differential currents which form the stage currents of each differential pair. The control voltage shifts the current between each side of the two differential pairs, regulating the signal level reaching the output stage which consists of op amp A1. Figure 11 shows the increase in signal attenuation as the control voltage becomes more negative.

The ideal transfer function for the voltage-controlled attenuator is:

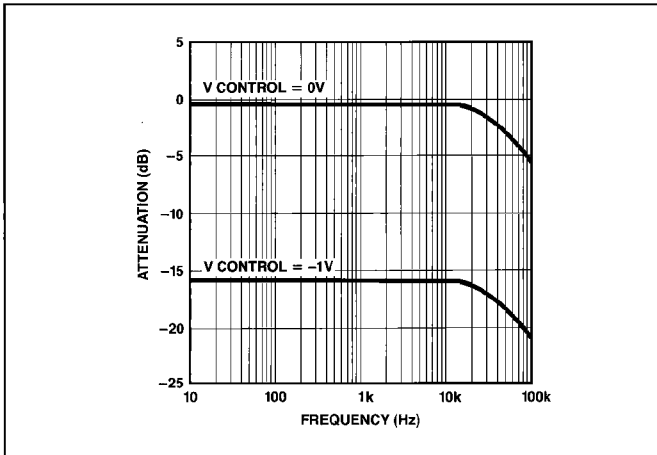
$$V_{OUT}/V_{IN} = \frac{2}{1 + \exp\left(\frac{-V_{CONTROL}}{R_{13} + R_{14}} \left(\frac{R_{14}}{R_{13} + R_{14}}\right) \left(\frac{kT}{q}\right)\right)}$$

Where  $k$  = Boltzmann constant  $1.38 \times 10^{-23}$  J/°K  
 $T$  = temperature in °K  
 $q$  = electronic charge =  $1.602 \times 10^{-19}$  C

From the transfer function it can be seen that the maximum gain of the circuit is 2 (6dB).

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see small amounts of reverse bias when the control voltage is positive, it may be prudent to use a nonpolarized tantalum capacitor.

**FIGURE 10:** Voltage-Controlled Attenuator,  
Attenuation vs Frequency



**FIGURE 11:** Voltage-Controlled Attenuator,  
Attenuation vs Control Voltage

