MPM3860

1.2MHz, Synchronous 2.75V to 7V, 6A Ultra-Thin Power Module

DESCRIPTION

The MPM3860 is a fully integrated, high-frequency, synchronous, rectified, step-down, power module with internal inductor. It offers a very compact solution to achieve 6A of continuous output current over a wide input range, with excellent load and line regulation. The MPM3860 has synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response and easy loop design, as well as very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MPM3860 requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-24 (4mmx6mm) package.

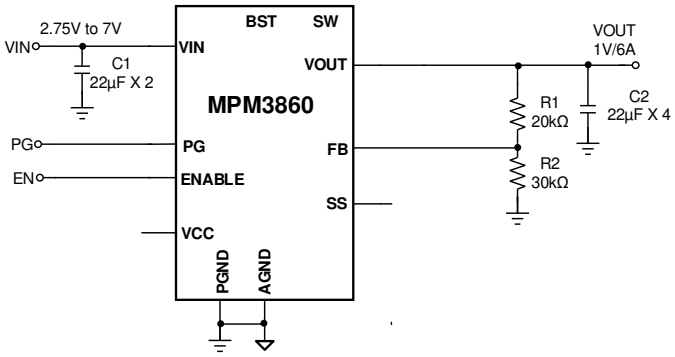
FEATURES

- Wide 2.75V to 7V Operating Input Range
- 6A Output Current
- Internal Power MOSFETs
- Output Adjustable from 0.6V
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Forced CCM Mode for Low V_{OUT} Ripple
- Fixed 1200kHz Switching Frequency
- External Programmable Soft-Start Time
- EN and Power Good for Power Sequencing
- Over-Current Protection and Hiccup Mode
- Thermal Shutdown
- Available in a QFN-24 (4mmx6mmx1.6mm) Package

APPLICATIONS

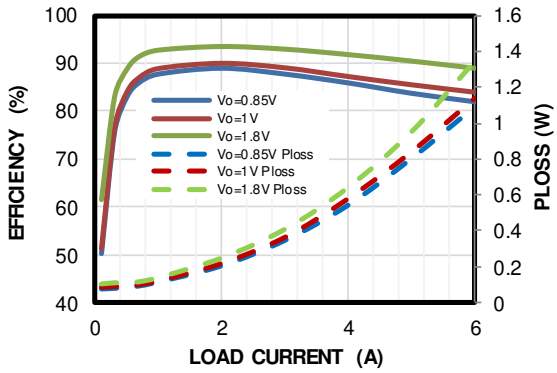
- FPGA Power Systems
- Optical Modules
- Telecom
- Networking
- Industrial Equipment

TYPICAL APPLICATION



Efficiency vs. Power Loss vs. Load Current

V_{IN} = 3.3V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3860GQW	QFN-24 (4mmx6mmx1.6mm)	*See Below*	3

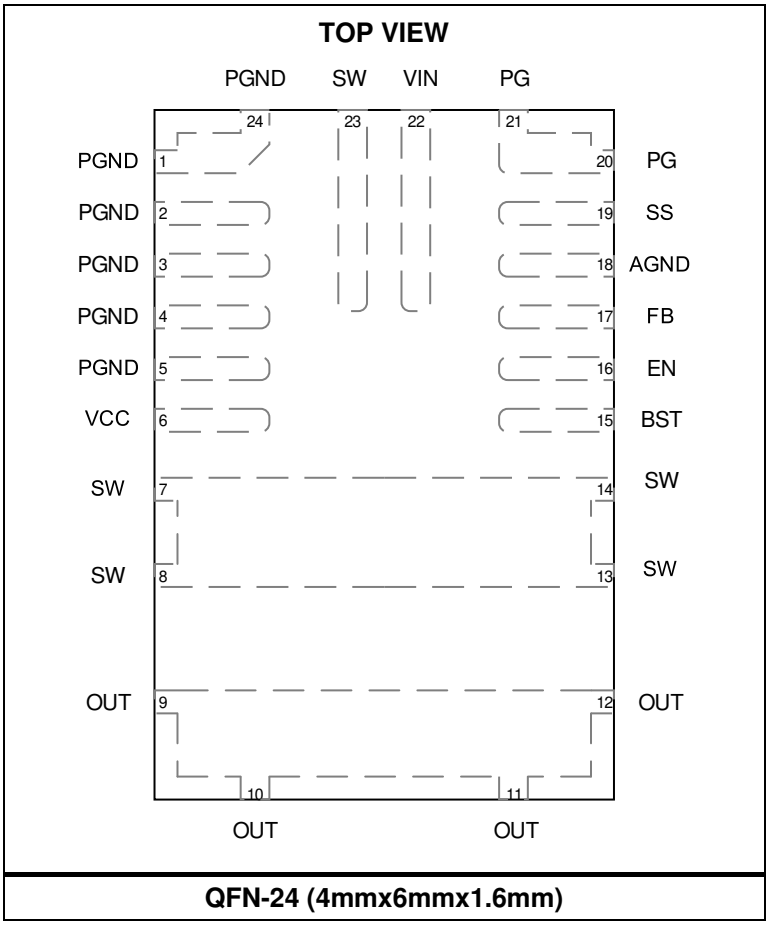
* For Tape & Reel, add suffix –Z (e.g. MPM3860GQW–Z).

TOP MARKING

MPSYWW
MP3860
LLLLLL
M

MPS: MPS prefix
Y: Year code
W: Week code
MP3860: Part number
LLLLLL: Lot number
M: Module

PACKAGE REFERENCE



QFN-24 (4mmx6mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 4, 5, 24	PGND	**System ground.** This pin is the reference ground of the regulated output voltage. Because of this, extra care must be taken when laying out the PCB. It is recommended to connect this pin to GND with copper and vias.
6	VCC	**Internal bias supply output.**
7, 8, 13, 14, 23	SW	**Switch output.** This pin can be left floating.
9, 10, 11, 12	OUT	**Output pin.** Connect this pin to COUT.
15	BST	**Bootstrap.** Internal capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
16	EN	**Enable.** Pull EN high to enable the part. When floating, EN is pulled down to GND by internal 3.3MΩ resistor and is disabled.
17	FB	**Feedback.** Sets the output voltage when connected to the tap of an external resistor divider that is connected between output and GND.
18	AGND	**Signal ground.** AGND is not internally connected to PGND, so ensure that AGND is connected to PGND in the PCB layout.
19	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time and avoid start-up inrush current. This pin includes an internal 22nF SS capacitor.
20, 21	PG	**Power good output.** The output of this pin is an open-drain output. Its state changes if UVP, OCP, OTP, or OV occurs.
22	VIN	**Supply voltage.** The part operates from a 2.75V to 7V input rail. C1 is necessary to decouple the input rail. Use a wide PCB trace to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +8V
V_{SW} .....
-0.3V (-5V < 10ns) to + V_{IN} + 0.7V (10V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2).....
.....4.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +125°C

ESD Rating

Human body model (HBM) 2kV
Charged device model (CDM) 2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.75V to 7V
Output voltage (V_{OUT})..... 0.6V to V_{IN} x D_{MAX}
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

EVM3860-QW-00A.....25.99 ..7.18 . °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation on the EVM3860-QW-00A board at any ambient temperature is calculated with P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.75		7	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2	5	µA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		105	150	µA
MOSFET						
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 7V			5	µA
Current Limit						
Valley current limit	I_{LIMIT_VY}		6	7		A
Short hiccup duty cycle (6)	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		0.9	1.2	1.6	MHz
Minimum on time (6)	t_{ON_MIN}			50		ns
Minimum off time (6)	t_{OFF_MIN}			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	µA
Enable and UVLO						
EN rising threshold	V_{EN_RISING}		1.19	1.23	1.27	V
EN falling threshold	$V_{EN\_FALLING}$		0.96	1	1.04	V
EN pin pull-down resistor	R_{EN_PD}			3.3		MΩ
VCC						
VCC under-voltage lockout rising threshold	VCC_{VTH}		2.4	2.5	2.6	V
VCC under-voltage lockout threshold	VCC_{HYS}			200		mV
VCC regulator	V_{CC}	V_{IN} = 5V		3.5		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%
Power Good						
Power good UV rising threshold	$PGUV_{VTH\_HI}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{VTH\_LO}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{VTH\_HI}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{VTH\_LO}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{TD}	Both edges		50		µs

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	T_{SD-HYS}			20		°C

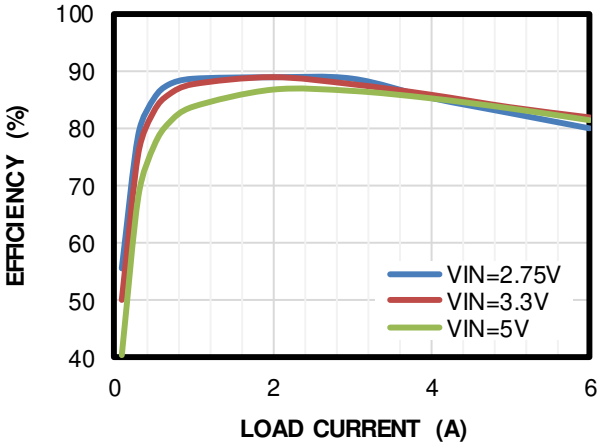
Notes:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization test.

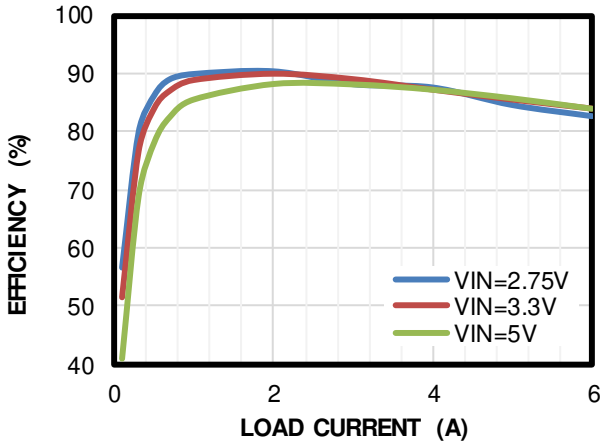
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

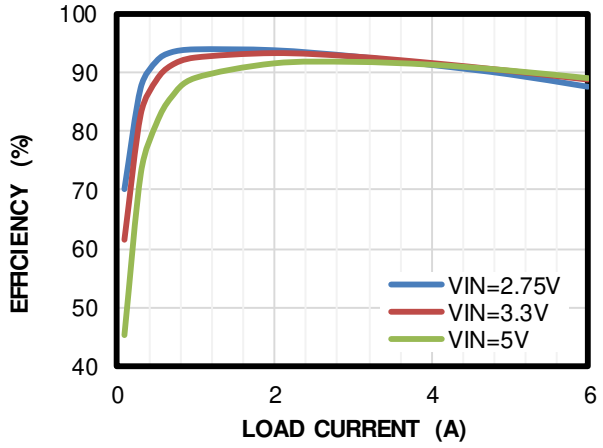
Efficiency vs. Load Current
V_{OUT} = 0.85V



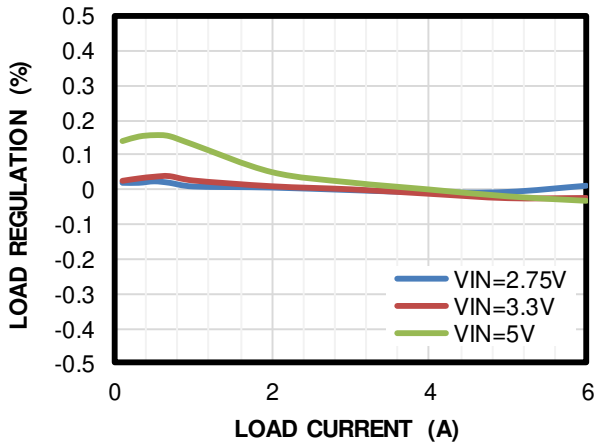
Efficiency vs. Load Current
V_{OUT} = 1V



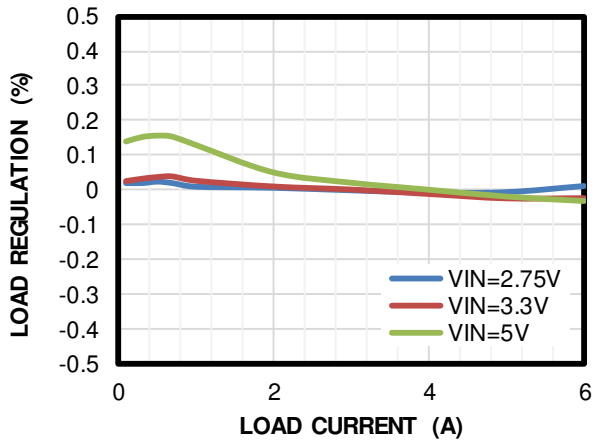
Efficiency vs. Load Current
V_{OUT} = 1.8V



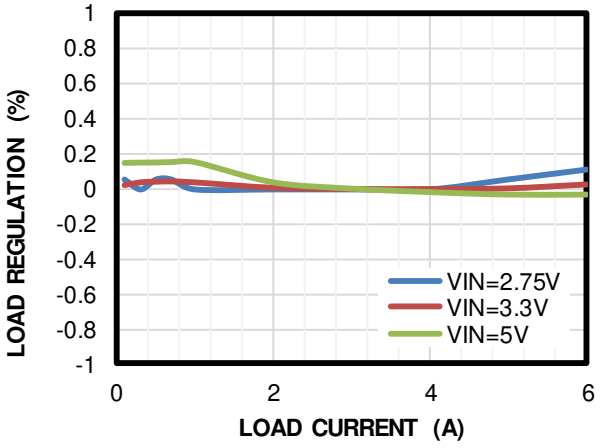
Load Regulation vs. Load Current
V_{OUT} = 0.85V



Load Regulation vs. Load Current
V_{OUT} = 1V



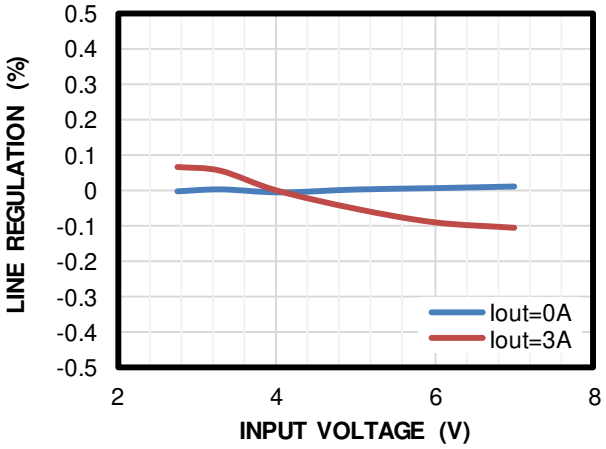
Load Regulation vs. Load Current
V_{OUT} = 1.8V



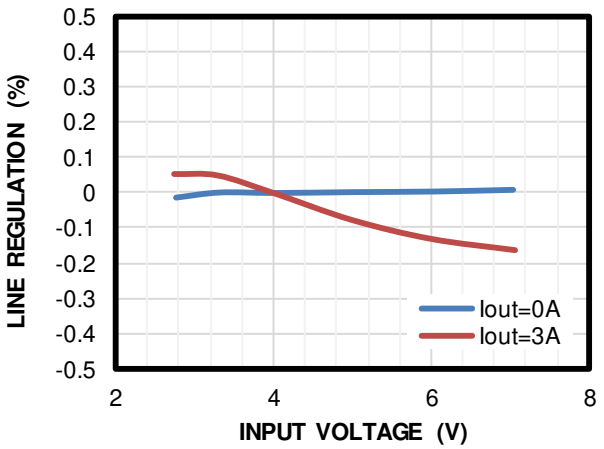
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

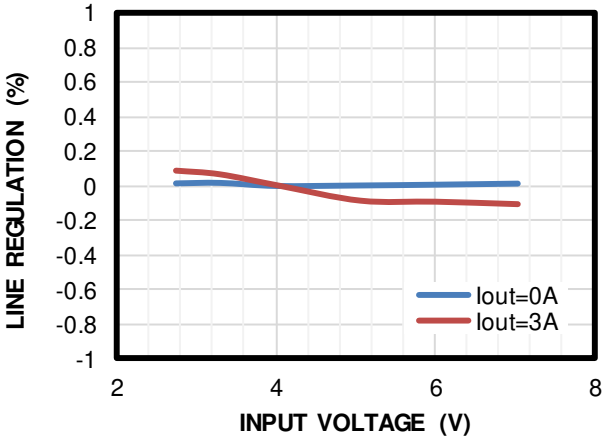
Line Regulation vs. Input Voltage
V_{OUT} = 0.85V



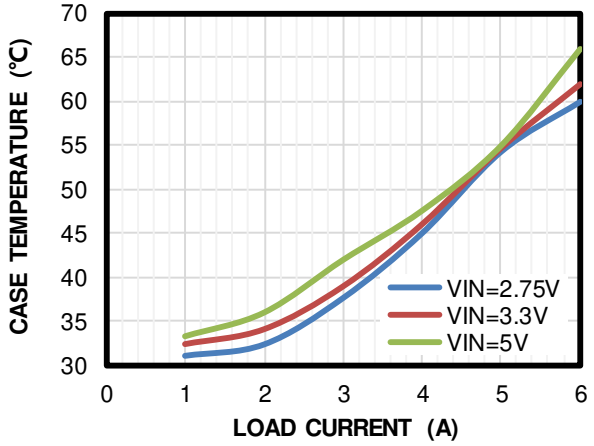
Line Regulation vs. Input Voltage
V_{OUT} = 1V



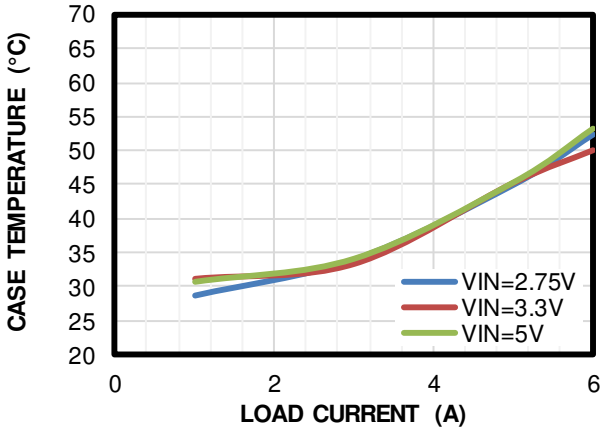
Line Regulation vs. Input Voltage
V_{OUT} = 1.8V



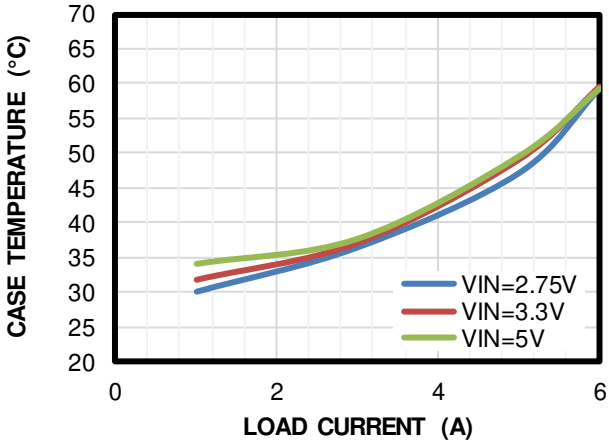
Thermal Rise
V_{OUT} = 0.85V



Thermal Rise
V_{OUT} = 1V



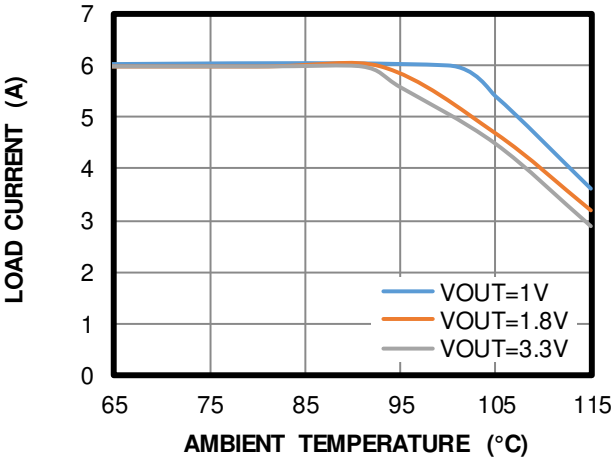
Thermal Rise
V_{OUT} = 1.8V



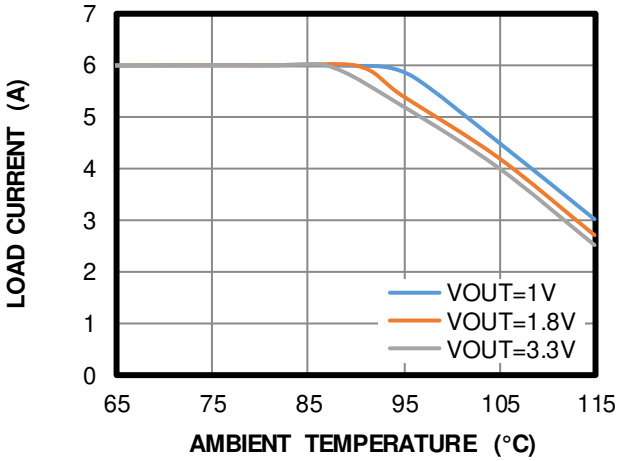
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

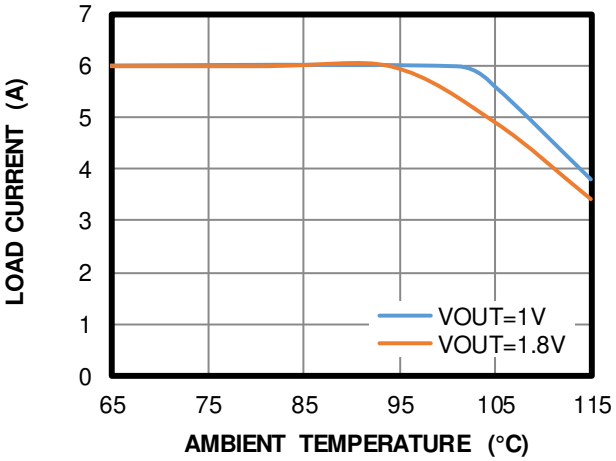
Thermal Derating
V_{IN} = 5V airflow



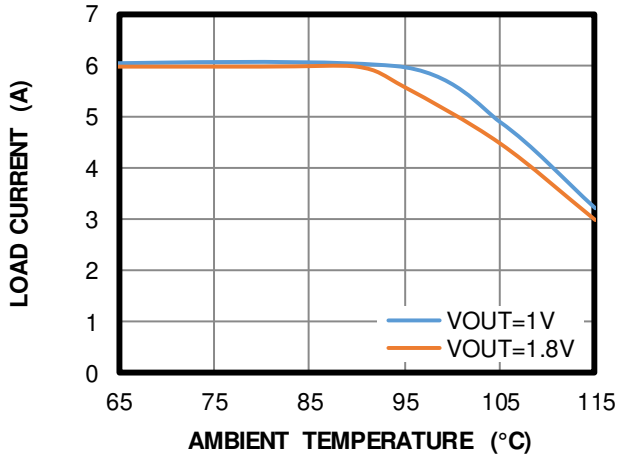
Thermal Derating
V_{IN} = 5V no airflow



Thermal Derating
V_{IN} = 3.3V airflow



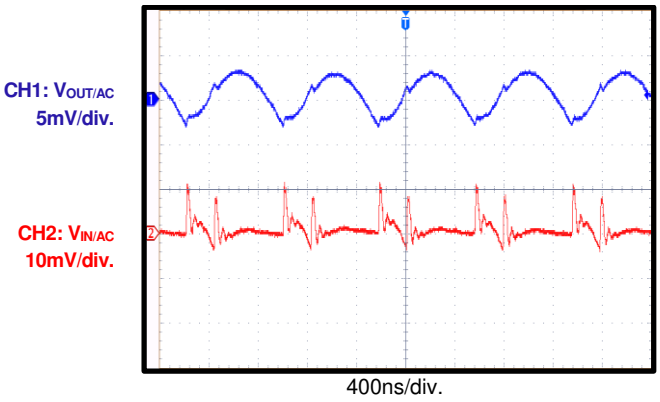
Thermal Derating
V_{IN} = 3.3V no airflow



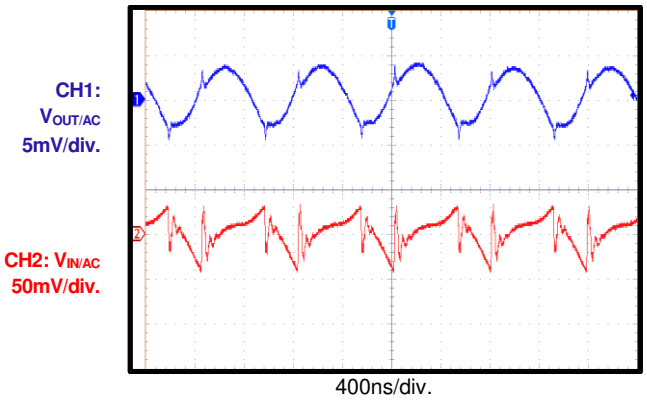
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

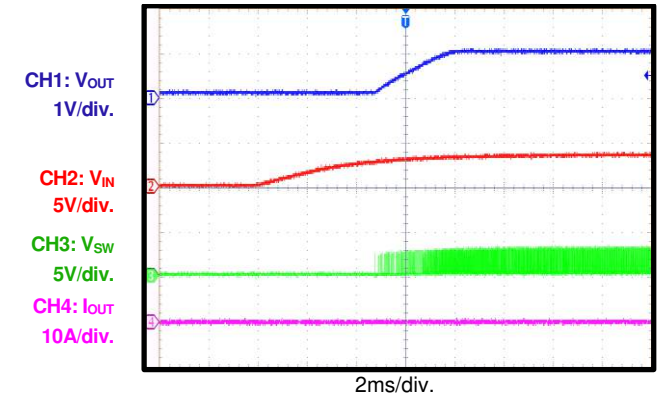
V_{OUT} Ripple
I_{OUT} = 0A



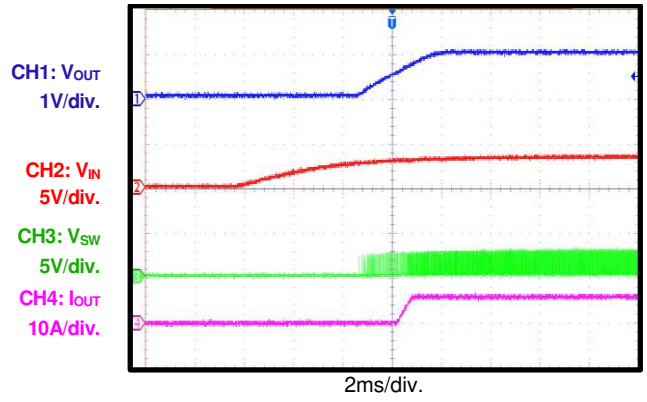
V_{OUT} Ripple
I_{OUT} = 6A



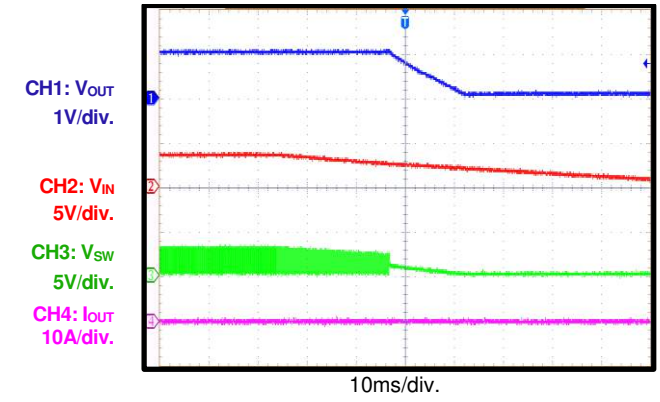
VIN Start-Up
I_{OUT} = 0A



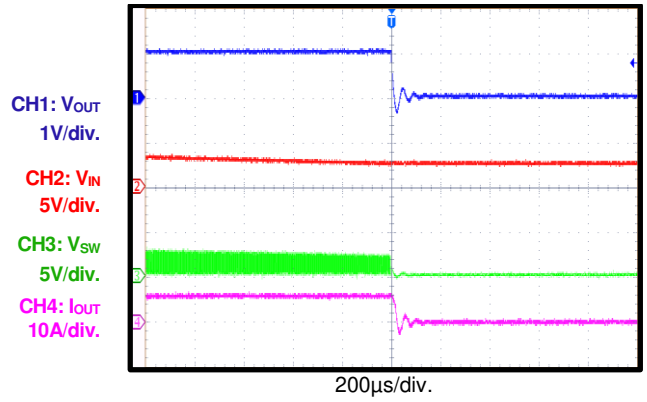
VIN Start-Up
I_{OUT} = 6A



VIN Shutdown
I_{OUT} = 0A



VIN Shutdown
I_{OUT} = 6A

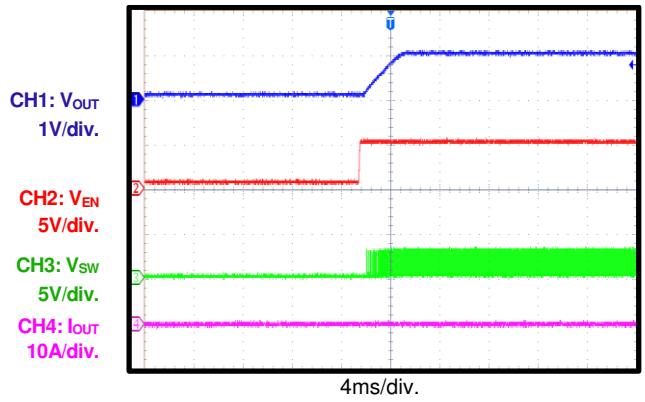


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

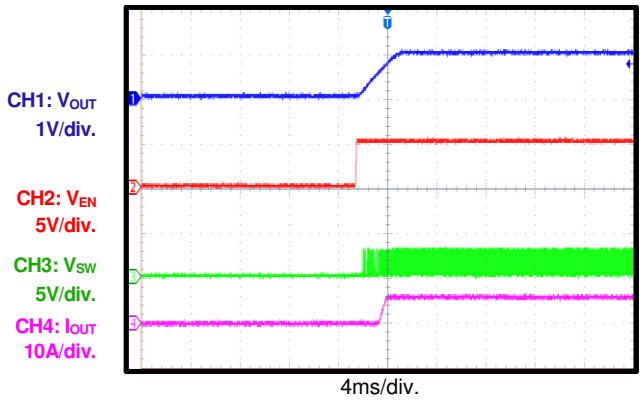
EN Start-Up

I_{OUT} = 0A



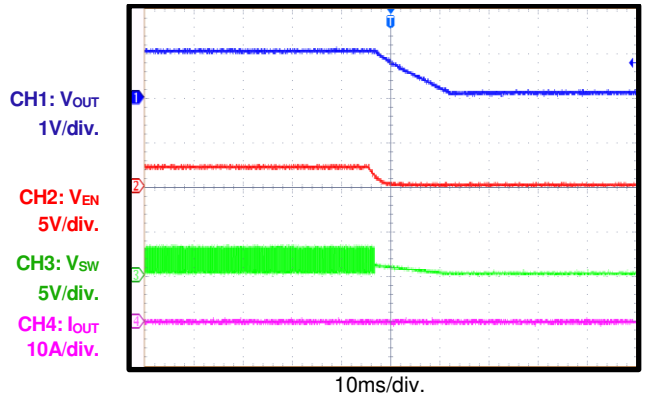
EN Start-Up

I_{OUT} = 6A



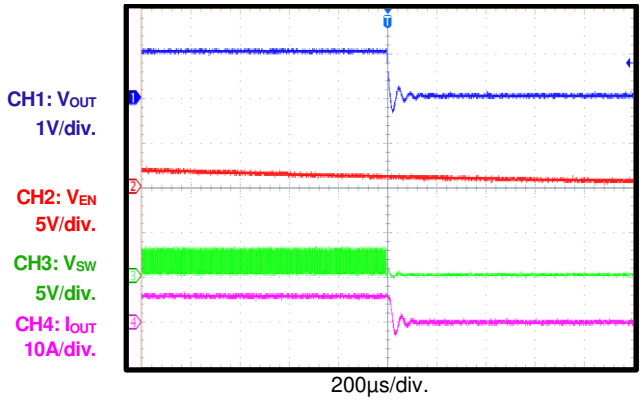
EN Shutdown

I_{OUT} = 0A

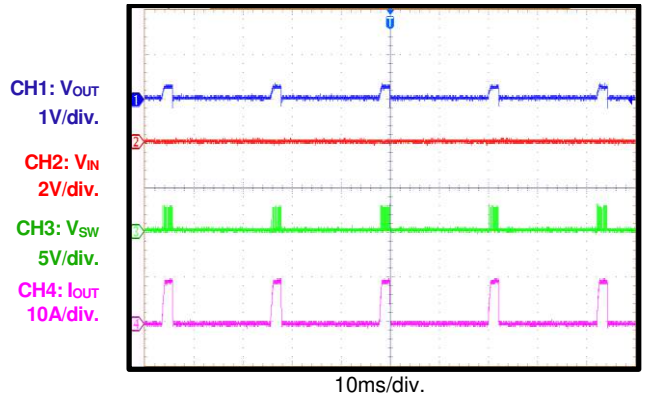


EN Shutdown

I_{OUT} = 6A

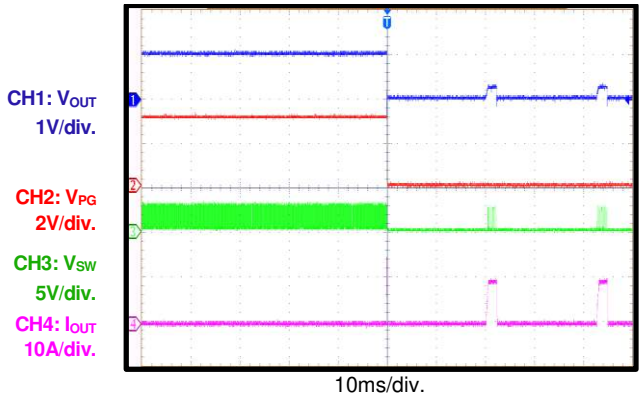


SCP Steady State



SCP Entry

I_{OUT} = 0A

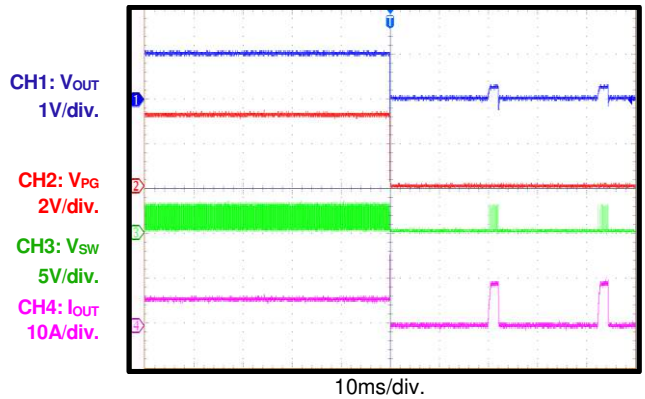


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

SCP Entry

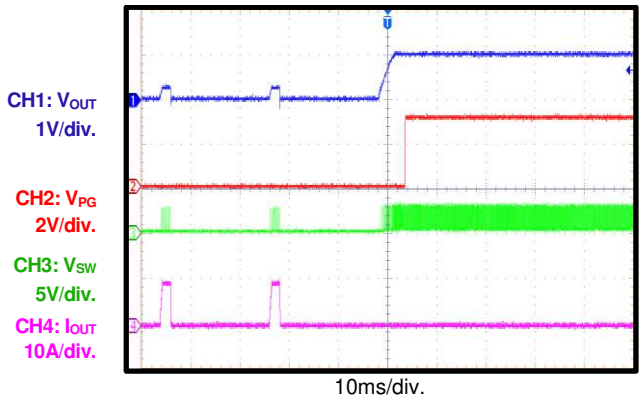
I_{OUT} = 6A



10ms/div.

SCP Recovery

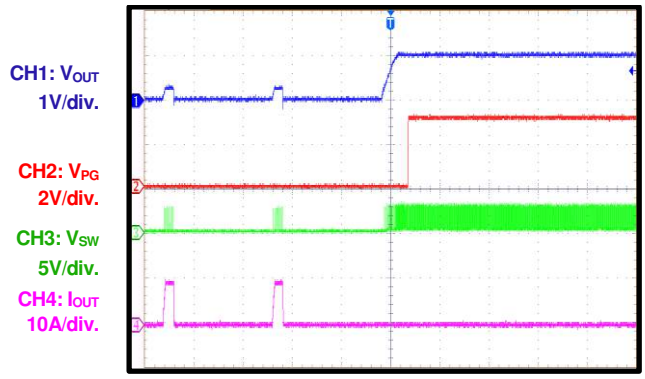
I_{OUT} = 0A



10ms/div.

SCP Recovery

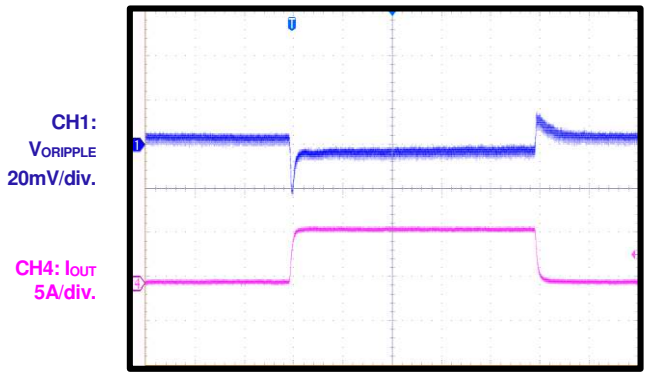
I_{OUT} = 6A



10ms/div.

Load Transient

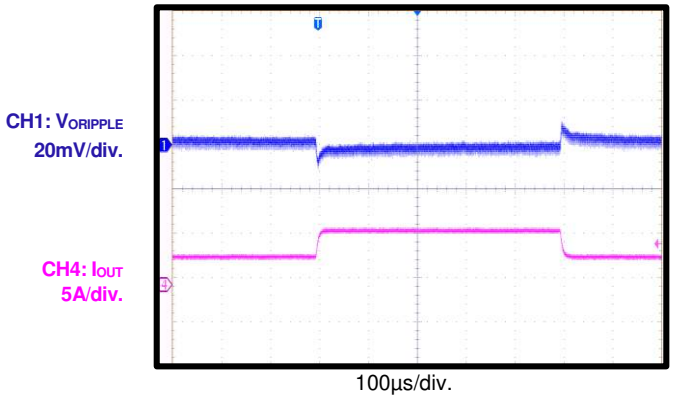
I_{OUT} = 0A to 6A



100µs/div.

Load Transient

I_{OUT} = 3A to 6A



100µs/div.

FUNCTIONAL BLOCK DIAGRAM

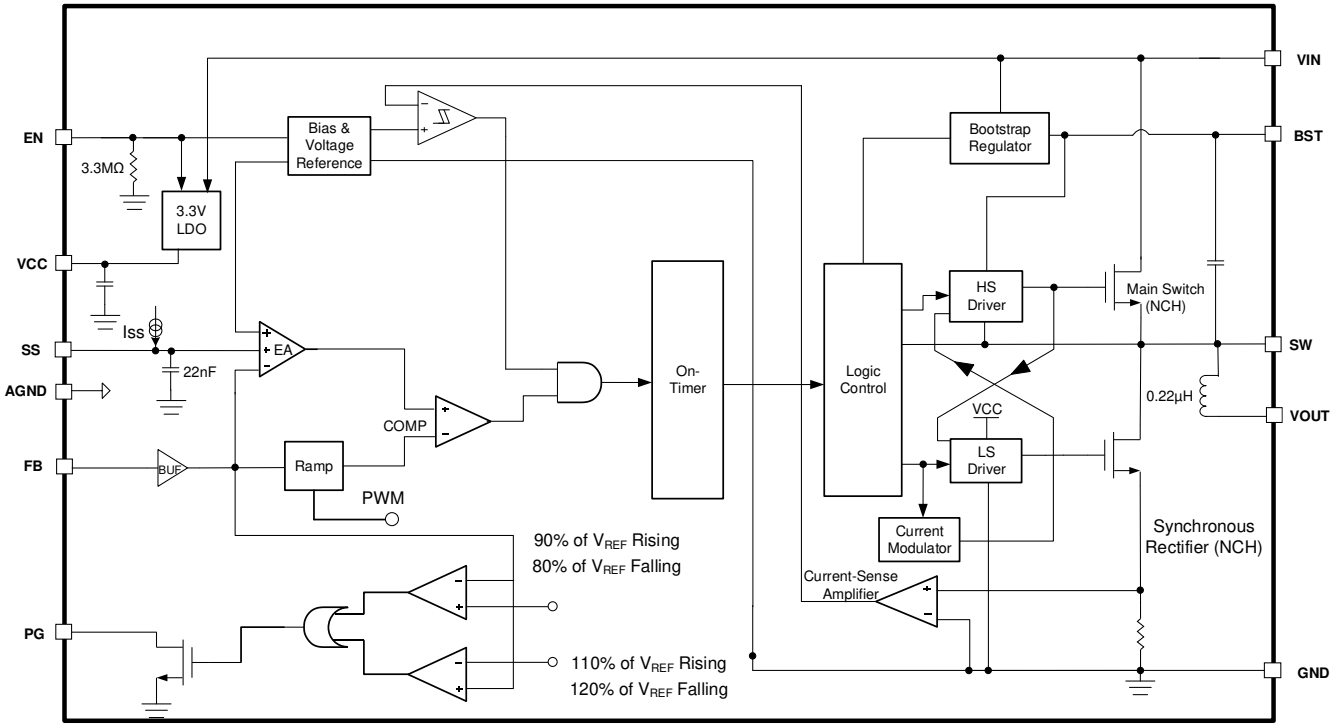


Figure 1: Functional Block Diagram

OPERATION

The MPM3860 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization.

Figure 2 shows the simplified ramp compensation block in the MPM3860. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates that there is an insufficient output voltage. The in period is determined by both the output voltage (V_{OUT}) and input voltage (V_{IN}), to make the switching frequency fairy constant over the entire input voltage range.

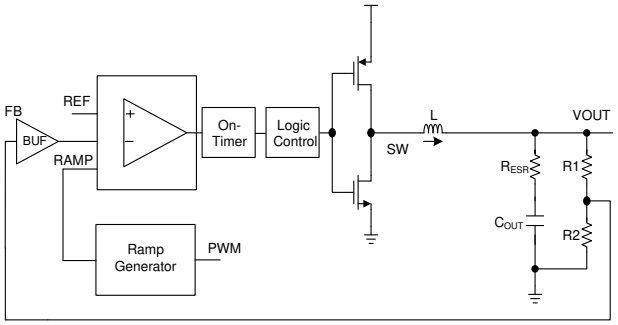


Figure 2: Simplified Ramp Compensation Block

After the on period elapses, the HS-FET turns off, or in other words, enters its off state. It turns on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize the conduction loss. If both the HS-FET and LS-FET are turned on at the same time, a dead short occurs between input and GND. This is called shoot-through. To avoid shoot-through, a dead time (DT) is internally generated between HS-FET off period and the LS-FET on period, and vice versa.

Internal compensation is applied during COT control to ensure more stable operation even when ceramic capacitors are used as output capacitors. This internal compensation also improves jitter performance without affecting the line or load regulation.

Continuous Conduction Mode (CCM)

The MPM3860 works at continuous conduction mode (CCM), the inductor current is always above 0A. Figure 3 shows the details of CCM operation. When V_{FB} is below V_{EAO}, HS-FET turns on for a fixed interval, which is determined by the one-shot on-timer. When the HS-FET is off, the LS-FET stays on until the next clock period. In CCM, the switching frequency is fairly constant.

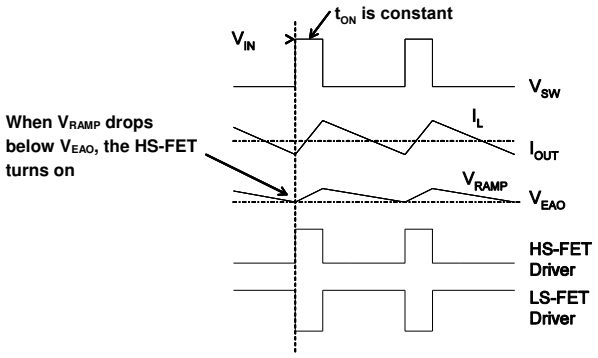


Figure 3: Continuous Conduction Mode

VCC Regulator

The 3.5V internal regulator powers most of the internal circuitry. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 3.5V, the output of the regulator is in full regulation; when V_{IN} falls below 3.5V, the output of the regulator decreases following V_{IN}. This pin has an internal 1μF VCC capacitor.

Enable

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.23V to turn the regulator on; drive it below 1V to turn the regulator off.

When floating, EN is pulled down to GND by an internal 3.3MΩ resistor.

EN can be connected directly to VIN. It supports a 7V input voltage range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM3860 UVLO comparator monitors the output voltage of the internal regulator (VCC). The VCC UVLO rising threshold is about 2.5V, and its falling threshold is 2.3V.

When the input voltage exceeds the UVLO rising threshold voltage, the MPM3860 starts up. It shuts down when the input voltage goes below the UVLO falling threshold voltage. This is a non-latch protection.

Soft Start

The MPM3860 employs a soft start (SS) mechanism to ensure smooth output ramping during start-up. When the EN pin goes high, an internal 6μA current source charges up the SS capacitor from 0V. The SS capacitor voltage feeds to the error amplifier to control the output voltage. The output voltage smoothly ramps up with the SS voltage (V_{SS}). Once V_{SS} exceeds V_{REF}, V_{SS} continues to ramp up until V_{REF} takes over. At this point, soft start finishes and the device enters steady state operation.

The SS capacitor value can be calculated with Equation (1):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

The MPM3860 has an internal 22nF SS capacitor.

If the output capacitance is large, it is not recommended to set the SS time to be too short, since a short SS time means that the device could easily reach the current limit during SS.

Power Good Indicator

The PG pin is the open drain of a MOSFET that connects to VCC or another voltage source through a resistor (eg. 100kΩ). The MOSFET turns on with the application of an input voltage so that the PG pin is pulled to GND before SS is ready. After V_{FB} reaches 90% of V_{REF}, the PG pin is pulled high after a 50μs delay. When V_{FB} drops to 80% of V_{REF}, the PG pin is pulled low.

If UVLO or over-temperature protection (OTP) occurs, the PG pin is pulled low immediately. If over-current protection (OCP) occurs, the PG pin is pulled low when V_{FB} drops below 80% of V_{REF} after a 0.05ms delay. If over-voltage protection (OVP) occurs, PG pin is pulled low when V_{FB} exceeds 120% of V_{REF} after a 0.05ms delay. If V_{FB} falls back below 110% of V_{REF}, the PG pin is pulled high after a 0.05ms delay.

If the input supply fails to power the MPM3860, PG is clamped low, even though it is tied to an external DC source through a pull-up resistor. Figure 4 shows the relationship between the PG voltage and the pull-up current.

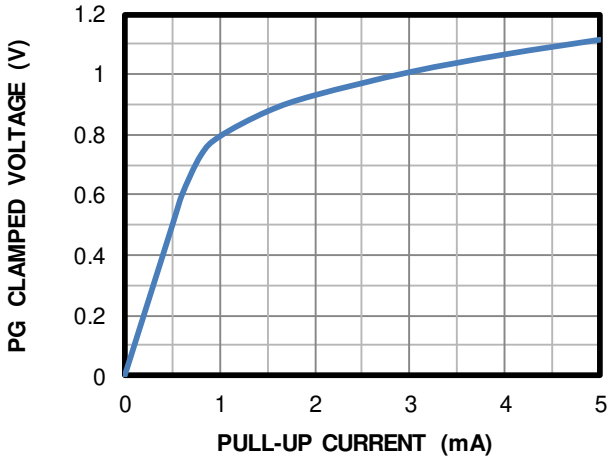


Figure 4: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MPM3860 has valley limit control. The LS-FET monitors the current flow. The HS-FET waits until the valley current limit disappears to turn on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MPM3860 enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device tries to recover from the over-current fault with hiccup mode. That means the chip disables the output power stage, discharges the soft-start capacitor, then automatically tries to soft start again. If the over-current condition still remains after soft start ends, the device repeats this operation cycle until the over-current condition disappears. Then the output rises back to the regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MPM3860 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up and the BST voltage is refreshed and charged, the voltage on the soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor's voltage exceeds the sensed output voltage at the FB pin, the part begins normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 150°C, the whole chip shuts down. Once the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen carefully, as too small a value leads to considerable quiescent current loss while too great a value makes FB noise sensitive. It is recommended to choose a value between 2kΩ and 100kΩ for R2 (see Table 1).

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_F (pF)	R_T (kΩ)
1.0	20	30	39	0
1.2	20	20	39	0
1.5	20	13	39	0
1.8	20	10	39	0
2.5	20	6.34	39	0
3.3	20	4.42	39	0

Typically, setting the current through R2 to less than 250μA provides a good balance between system stability and minimal load loss. Then R1 can be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

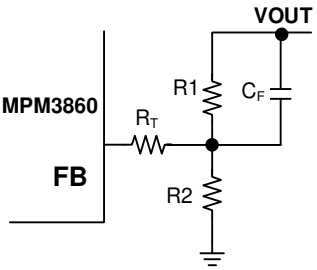


Figure 5: Feedback Network

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

In addition to benefits for the output ripple, a larger output capacitor can also get better load transient response. However, maximum output capacitor limitations should be also considered in design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time, and then the device will fail to regulate. The maximum output capacitor value C_{O_MAX} can be limited using Equation (10):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, t_{SS} is the soft-start time.

PCB Layout Guidelines (7)

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Connect a large ground plane directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure the high-current paths at PGND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor as close to the VIN and PGND pins as possible to minimize high-frequency noise.
5. Keep the paths between the input capacitor and IN as short and wide as possible.
6. Place a VCC decoupling capacitor close to the MPM3860, and connect AGND and PGND at the point of VCC capacitor's ground connection.
7. Connect VIN, VOUT, and PGND to a large copper area to improve thermal performance and long-term reliability.
8. Separate the input PGND area from the other PGND area at the top layer, and connect them together at the internal layers and bottom layer through multiple vias.
9. Ensure that there is a complete GND plane at either the internal layer or the bottom layer.
10. Ensure that any signal trace is placed far away from SW.
11. A 4-layer layout is recommended to achieve better thermal performance. Use multiple vias to connect the power planes to internal layers.

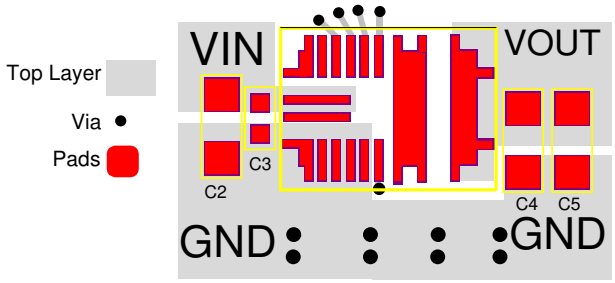


Figure 6: Recommended PCB Layout

Note:

7) The recommended layout is based on Figure 7 (see the Typical Application Circuits section on page 18).

TYPICAL APPLICATION CIRCUITS

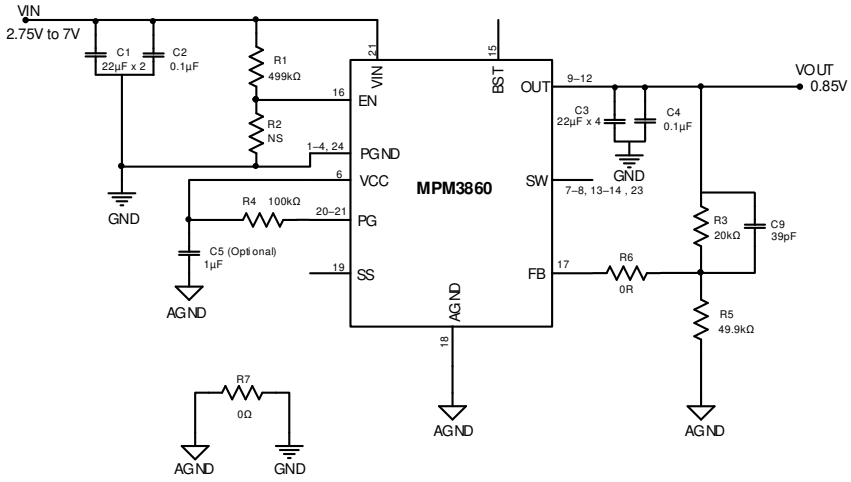


Figure 7: Typical Application Circuit with 0.85V Output

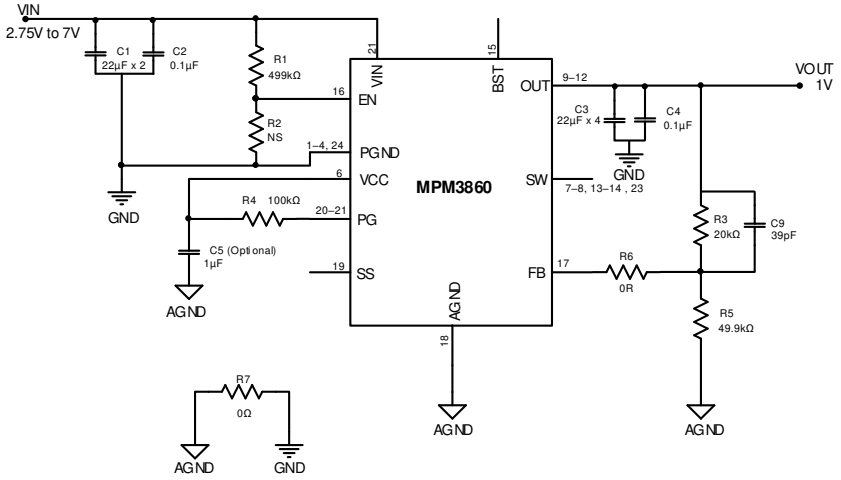


Figure 8: Typical Application Circuit with 1V Output

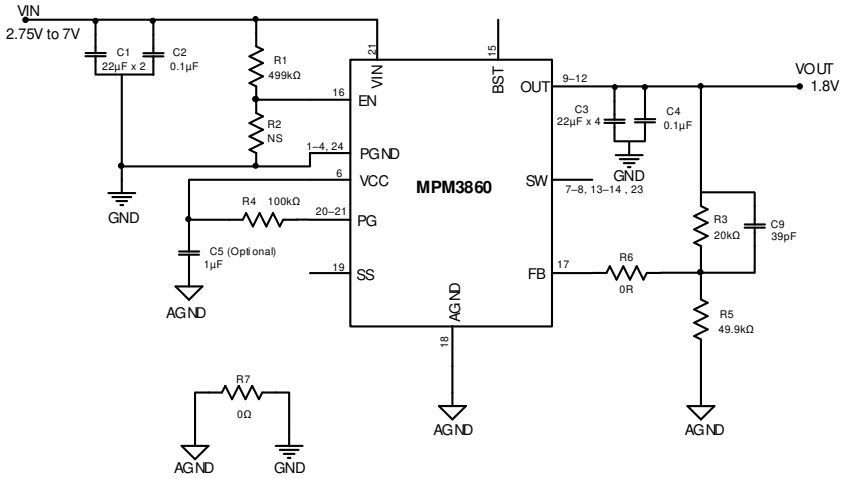
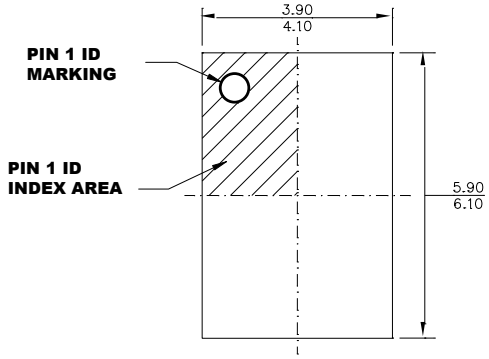


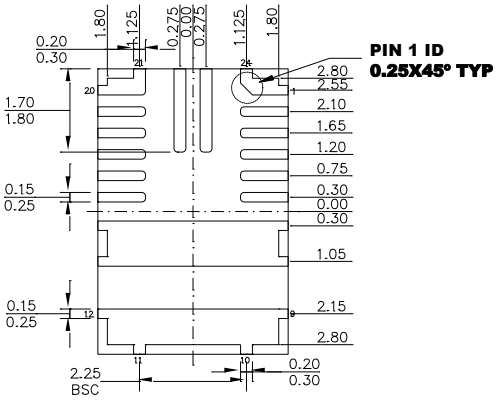
Figure 9: Typical Application Circuit with 1.8V Output

PACKAGE INFORMATION

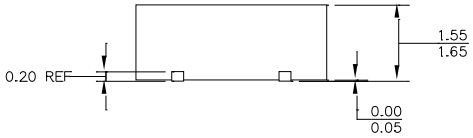
QFN-24 (4mmx6mmx1.6mm)



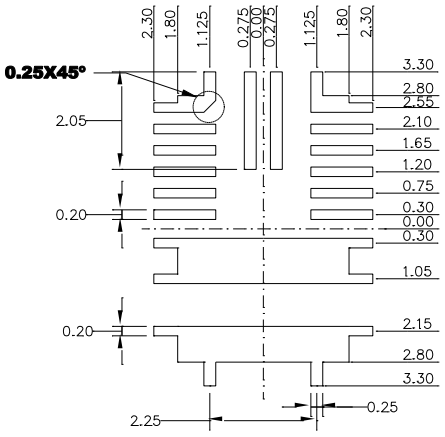
TOP VIEW



BOTTOM VIEW



SIDE VIEW

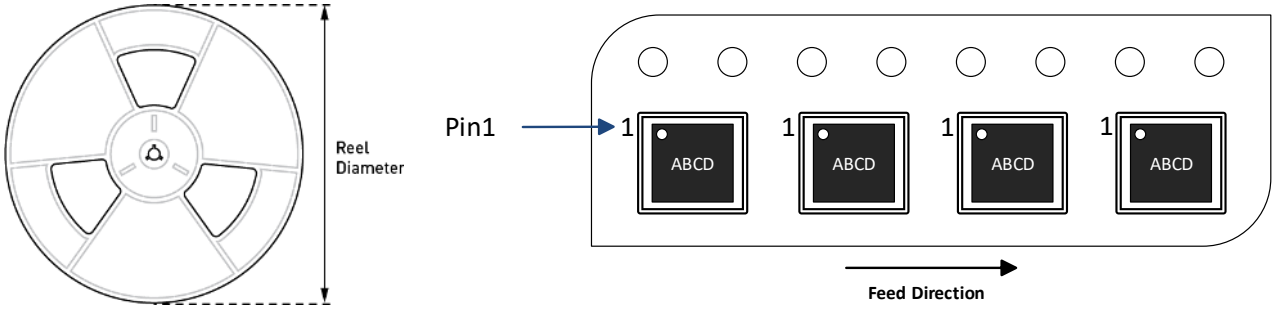


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3860GQW–Z	QFN-24 (4mmx6mmx1.6mm)	2500	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	09/14/2020	Initial Release	-