# ACPL-K370, ACPL-K376

Isolated Voltage/Current Detector

## Data Sheet


### Description

The ACPL-K370 and ACPL-K376 are voltage/current threshold detection optocouplers. The ACPL-K376 is a low-current version of the ACPL-K370. To obtain lower current operation, the ACPL-K376 uses a high-efficiency AlGaAs LED which has higher light output at lower drive currents. Both devices have a threshold sensing input buffer IC that allows threshold levels to be set by a single external resistor over a wide range of input voltages.

The input buffer has several performance enhancing features: hysteresis for extra noise immunity and switching immunity, a diode bridge for easy use with AC input signals, and internal clamping diodes to protect the buffer and LED from over-voltage and over-current transients. Because threshold sensing is done prior to driving the LED, variations in optical coupling from the LED to the detector will not effect the threshold levels.

The ACPL-K370 input buffer IC has a nominal turn-on threshold of 3.8 V($V_{TH+}$) and 2.77 mA ($I_{TH+}$). The buffer IC for the ACPL-K376 is designed for lower input current. The nominal turn-on threshold for the ACPL-K376 is 3.8 V ($V_{TH+}$) and 1.32 mA ($I_{TH+}$), which reduces power dissipation by 52%.

The high-gain output stage features an open-collector output for both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

By combining many unique functions in a single package, the ACPL-K370 and ACPL-K376 are ideal components for industrial control computer input boards and other applications where a predetermined input threshold level is needed.

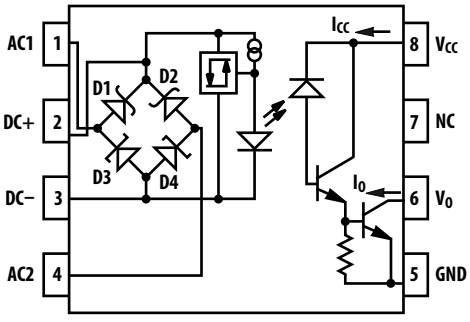
### Features

- ± 5% voltage detection accuracy
- Wide AC or DC detection range: up to 1140 Vpeak
- User configurable single/dual detection levels
- Built-in hysteresis improves noise immunity
- Very low threshold current: 1.32 mA (ACPL-K376)
- Logic compatible output
- Wide output supply voltage: 2 V to 18 V
- –40°C to +105°C operating temperature range
- SSO-8 package with 8 mm creepage and clearance
- Safety and regulatory approval:
  - IEC/EN/DIN EN 60747-5-5: 1140 Vpeak working insulation voltage
  - UL 1577: 5000 Vrms/1minute double protection rating
  - CSA: Component Acceptance Notice #5

### Applications

- Limit switch sensing
- Low voltage detector
- AC mains and DC-link voltage detection
- Relay contact monitor
- Relay coil voltage monitor
- Current sensing
- Microprocessor interfacing
- Telephone ring detection

### Functional Diagram




TRUTH TABLE (POSITIVE LOGIC)

| INPUT | OUTPUT |
|---|---|
| H | L |
| L | H |

Figure 1. Functional Diagram

### Connection Diagram

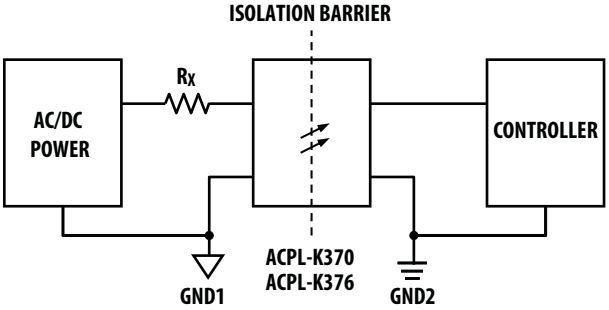



Figure 2. Connection Diagram

## Table 1. Ordering Information

The ACPL-K370 and ACPL-K376 are UL recognized with 5000 Vrms for 1 minute per UL1577.

| Part number | Option RoHS Compliant | Package | Surface Mount | Tape & Reel | IEC/EN/ DIN EN 60747-5-2 | Quantity |
|---|---|---|---|---|---|---|
| ACPL-K370 ACPL-K376 | -000E | Stretched SO-8 | X | | | 80 per tube |
| | -060E | | X | | X | 80 per tube |
| | -500E | | X | X | | 1000 per reel |
| | -560E | | X | X | X | 1000 per reel |

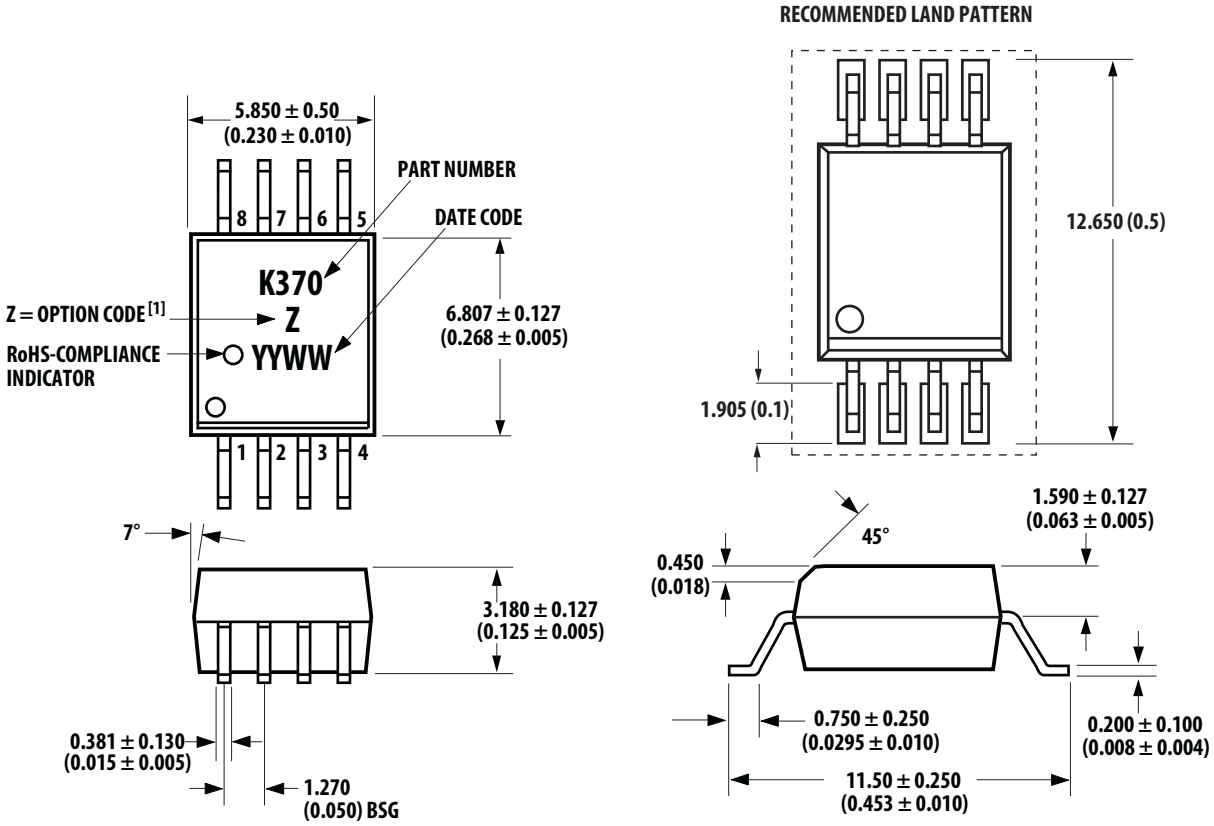
To form a complete ordering part number, choose a part number from the part number column and combine it with the desired option from the option column.

**Example 1:**

ACPL-K370-560E orders an RoHS compliant part with an IEC/EN/DIN EN 60747-5-5 certification and Tape & Reel packaging.

## Package Outline Drawings

### Stretched SO-8 Package (SSO-8)




Note 1. "V" = Options comprise 060; other options are not marked.

Dimensions in millimeters and (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

**Figure 3.**

## Recommended Lead-Free IR Soldering Profile

The recommended reflow soldering profile is  per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

## Regulatory Information

The ACPL-K370/K376 is approved by the following organizations:

**IEC/EN/DIN EN 60747-5-5 (with option 060)**

Approved with a maximum working insulation voltage of $V_{IORM}$ = 1140 Vpeak, and with a highest allowable over-voltage of $V_{IOTM}$ = 8000 Vpeak.

**UL**

Approval under the UL 1577 component recognition program up to $V_{ISO}$ = 5000 $V_{RMS}$ / 1 minute. File E55361.

**CSA**

Approval under CSA Component Acceptance Notice #5, File CA 88324.

**Table 2. Insulation Related Specifications**

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (Clearance) | L(IO1) | 8 | mm | L(IO1) |
| Minimum External Tracking Path (Creepage) | L(IO2) | 8 | mm | Measured from input terminals to output terminals |
| Minimum Internal Plastic Gap (Clearance) | | 0.08 | mm | Through insulation distance conductor to conductor |
| Tracking Resistance | CTI | 175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group (per DIN VDE 0109) | | IIIa | | Material Group DIN VDE 0109 |

**Table 3. IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics [1] (with option 060)**

| Description | Symbol | Characteristic | Units |
|---|---|---|---|
| Installation Classification per DIN VDE 0110/1.89, Table 1: | | | |
| for rated mains voltage ≤ 300 Vrms | | I-IV | |
| for rated mains voltage ≤ 450 Vrms | | I-III | |
| for rated mains voltage ≤ 600 Vrms | | I-III | |
| for rated mains voltage ≤ 1000 Vrms | | I-II | |
| Climatic Classification | | 55/105/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 1140 | Vpeak |
| Input to Output Test Voltage, Method b<br>$V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 second,<br>Partial Discharge < 5 pC | $V_{PR}$ | 2137 | Vpeak |
| Input to Output Test Voltage, Method a<br>$V_{IORM}$ x 1.6 = $V_{PR}$, Type and sample test, $t_m$ = 10 seconds,<br>Partial Discharge < 5 pC | $V_{PR}$ | 1824 | Vpeak |
| Highest Allowable Overvoltage (Transient overvoltage, $t_{ini}$ = 60 seconds) | $V_{IOTM}$ | 8000 | Vpeak |
| Safety Limiting Values (Maximum values allowed in the event of a failure) | | | |
| Case Temperature | $T_S$ | 175 | °C |
| Input Current [2] | $I_{S,INPUT}$ | 230 | mA |
| Output Power [2] | $P_{S,OUTPUT}$ | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | $10^9$ | Ω |

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.
2. Safety-limiting parameters are dependent on case temperature. The input current, $I_{S,INPUT}$, should be derated linearly above 25°C free-air case temperature at a rate of 1.53 mA / °C; the Output Power, $P_{S,OUTPUT}$, should be derated linearly above 25°C free-air case temperature at a rate of 4 mW / °C.

**Table 4. Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Units | Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | 125 | °C | |
| Operating Temperature | $T_A$ | –40 | 105 | °C | |
| Input Current, Average | $I_{IN}$ | | 50 | mA | 1 |
| Input Current, Surge | $I_{IN}$ | | 140 | mA | 1, 2 |
| Input Current, Transient | $I_{IN}$ | | 500 | mA | 1, 2 |
| Input Voltage (Pins 2-3) | $V_{IN}$ | –0.5 | | V | |
| Input Power Dissipation | $P_{IN}$ | | 200 | mW | 3 |
| Total Package Power Dissipation | $P_T$ | | 269 | mW | 4 |
| Output Power Dissipation | $P_O$ | | 163 | mW | 5 |
| Output Current, Average | $I_O$ | | 30 | mA | 6 |
| Supply Voltage (Pins 8-5) | $V_{CC}$ | –0.5 | 20 | V | |
| Output Voltage (Pins 6-5) | $V_O$ | –0.5 | 20 | V | |
| Lead Solder Temperature | | 260°C for 10 seconds, measured at 1.6 mm below seating plane. | | | |

Notes:
1. Current into or out of any single lead.
2. Surge input current duration is 3 ms at a 120 Hz pulse repetition rate. Transient input current duration is 10 µs at a 120 Hz pulse repetition rate. Note that the maximum input power, PIN, must be observed.
3. Derate linearly above 105°C free-air temperature at a rate of 10 mW / °C. The maximum input power dissipation of 200 mW allows an input IC junction temperature of 125°C at an ambient temperature of $T_A$ = 105°C. Excessive $P_{IN}$ and $T_J$ may result in IC chip degradation.
4. Derate linearly above 105°C free-air temperature at a rate of 13.5 mW / °C.
5. Derate linearly above 105°C free-air temperature at a rate of 8.2 mW / °C. A maximum output power dissipation of 163 mW allows an output IC junction temperature of 125°C at an ambient temperature of $T_A$ = 105°C.
6. Derate linearly above 105°C free-air temperature at a rate of 1.5 mA / °C.

**Table 5. Recommended Operating Conditions**

| Parameter | Symbol | Min | Max | Units | Note |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2 | 18 | V | |
| Operating Temperature | $T_A$ | –40 | 105 | °C | |
| Operating Frequency, $V_{CC}$ = 5 V | f | 0 | 9 | kHz | 1 |
| Operating Frequency, $V_{CC}$ = 3.3 V | f | 0 | 5 | kHz | 1 |

Notes:
1. Maximum operating frequency is defined when the output waveform at pin 6 obtains only 90% of $V_{CC}$ with $R_L$ = 4.7 kΩ, $C_L$ = 30 pF using a 5 V square wave input signal.

**Table 6. Electrical Specifications**

Unless otherwise noted, $T_A$ = –40°C to +105°C and $V_{CC}$ = 3 V to 5.5 V.

| Parameter | Sym. | Device | Min | Typ[1] | Max | Units | Test Conditions/Notes | Fig. |
|---|---|---|---|---|---|---|---|---|
| Upper Threshold Voltage, DC Input (Pins 2, 3) | $V_{TH+}$ | | 3.6 (–5%) | 3.8 | 4 (+5%) | V | $T_A$ = 25°C, $V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open | 5, 6 |
| | | | 3.35 | | 4.05 | V | $V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open | 5, 6 |
| Lower Threshold Voltage, DC Input (Pins 2, 3) | $V_{TH–}$ | | 2.45 (–5%) | 2.59 | 2.72 (+5%) | V | $T_A$ = 25°C, $V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open | 5, 6 |
| | | | 2.01 | | 2.96 | V | $V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open | 5, 6 |
| Upper Threshold Voltage, AC Input (Pins 1, 4) | $V_{TH+}$ | | 4.7 (–6%) | 5 | 5.3 (+6%) | V | $T_A$ = 25°C, $V_{IN} = V_{AC1} – V_{AC2}$, DC+ and DC– open; Note 2 | 5, 6 |
| | | | 4.23 | | 5.5 | V | $V_{IN} = V_{AC1} – V_{AC2}$, DC+ and DC– open | 5, 6 |
| Lower Threshold Voltage, AC Input (Pins 1, 4) | $V_{TH–}$ | | 3.57 (–6%) | 3.8 | 4.03 (+6%) | V | $T_A$ = 25°C, $V_{IN} = V_{AC1} – V_{AC2}$, DC+ and DC– open | 5, 6 |
| | | | 2.87 | | 4.42 | V | $V_{IN} = V_{AC1} – V_{AC2}$, DC+ and DC– open | 5, 6 |
| Upper Threshold Current | $I_{TH+}$ | ACPL-K370 | 2.26 | 2.77 | 2.99 | mA | $T_A$ = 25°C | 5, 6 |
| | | | 1.96 | | 3.11 | mA | | 5, 6 |
| Upper Threshold Current | $I_{TH+}$ | ACPL-K376 | 1.03 | 1.32 | 1.46 | mA | $T_A$ = 25°C | 5, 6 |
| | | | 0.87 | | 1.56 | mA | | 5, 6 |
| Lower Threshold Current | $I_{TH–}$ | ACPL-K370 | 1.09 | 1.44 | 1.59 | mA | $T_A$ = 25°C | 5, 6 |
| | | | 1 | | 1.62 | mA | | 5, 6 |
| Lower Threshold Current | $I_{TH–}$ | ACPL-K376 | 0.48 | 0.68 | 0.77 | mA | $T_A$ = 25°C | 5, 6 |
| | | | 0.43 | | 0.8 | mA | | 5, 6 |
| Current Hysteresis | $I_{HYS}$ | ACPL-K370 | | 1.2 | | mA | $I_{HYS} = I_{TH+} – I_{TH–}$ | 5 |
| | | ACPL-K376 | | 0.6 | | mA | | |
| Voltage Hysteresis | $V_{HYS}$ | | | 1.2 | | V | $V_{HYS} = V_{TH+} – V_{TH–}$ | 5 |
| Input Clamp Voltage | $V_{IHC1}$ | | 5.4 | 6.1 | 6.8 | V | $V_{IHC1} = V_{DC+} – V_{DC–}$, $I_{IN}$ = 10 mA, AC1 & AC2 connected to DC– | 4 |
| | $V_{IHC2}$ | | 6.1 | 6.8 | 7.4 | V | $V_{IHC2} = \lvert V_{AC1} – V_{AC2} \rvert$, $\lvert I_{IN} \rvert$ = 10 mA, DC+ and DC– open | 4 |
| | $V_{IHC3}$ | | | 12.5 | 13.4 | V | $V_{IHC3} = V_{DC+} – V_{DC–}$, $I_{IN}$ = 15 mA, AC1 & AC2 open | 4 |
| | $V_{ILC}$ | | | –0.76 | | V | $V_{ILC} = V_{DC+} – V_{DC–}$, $I_{IN}$ = –10 mA | |
| Input Current | $I_{IN}$ | ACPL-K370 | 3.2 | 3.9 | 4.4 | mA | $V_{DC+} – V_{DC–}$ = 5 V, AC1 and AC2 open | 8 |
| Input Current | $I_{IN}$ | ACPL-K376 | 1.5 | 1.9 | 2.2 | mA | $V_{DC+} – V_{DC–}$ = 5 V, AC1 and AC2 open | 8 |
| Bridge Diode Forward Voltage | $V_{D1,2}$ | ACPL-K370 | | 0.59 | | V | $I_{IN}$ = 3 mA | |
| | | ACPL-K376 | | 0.47 | | V | $I_{IN}$ = 1.5 mA | |
| | $V_{D3,4}$ | ACPL-K370 | | 0.78 | | V | $I_{IN}$ = 3 mA | |
| | | ACPL-K376 | | 0.73 | | V | $I_{IN}$ = 1.5 mA | |
| Logic Low Output Voltage | $V_{OL}$ | | | 0.05 | 0.4 | V | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.2 mA; Note 3 | 8 |
| Logic High Output Current | $I_{OH}$ | | | | 100 | µA | $V_{OH} = V_{CC}$ = 18 V; Note 4 | |
| Logic Low Supply Current | $I_{CCL}$ | ACPL-K370 | | 0.9 | 4 | mA | $V_{DC+} – V_{DC–}$ = 5 V, $V_O$ open | 9 |
| | | ACPL-K376 | | 0.5 | 3 | mA | | |
| Logic High Supply Current | $I_{CCH}$ | | | 0.002 | 4 | µA | $V_{CC}$ = 18 V, $V_O$ open | 7 |
| Input Capacitance | $C_{IN}$ | | | 50 | | pF | f = 1 MHz, $V_{IN}$ = 0 V | |

Notes:
1. All typical values are at $T_A$ = 25°C unless otherwise stated.
2. AC voltage is instantaneous voltage.
3. A logic "Low" output level at pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH–}$ once $V_{IN}$ has exceeded $V_{TH+}$.
4. A logic "High" output level at pin 6 occurs under the conditions of $V_{IN} \leq V_{TH–}$ as well as the range of $V_{IN} < V_{TH+}$ once $V_{IN}$ has decreased below $V_{TH–}$.

**Table 7. Switching Specifications**

Unless otherwise noted, $T_A$ = –40°C to +105°C.

| Parameter | Sym | Device | Min | Typ[1] | Max | Units | Test Conditions/Notes | Fig. |
|---|---|---|---|---|---|---|---|---|
| **$V_{CC}$ = 4.5 V** | | | | | | | | |
| Propagation Delay Time to Logic Low at Output | $t_{PHL}$ | ACPL-K370 | | 3.7 | 7.5 | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF; Note 2 | 10 |
| | | ACPL-K376 | | 6.2 | 12.5 | µs | | |
| | | ACPL-K370 | | 3.7 | 7.5 | µs | $R_L$ = 1.8 kΩ, $C_L$ = 15 pF; Note 2 | |
| | | ACPL-K376 | | 6.3 | 12.5 | µs | | |
| Propagation Delay Time to Logic High at Output | $t_{PLH}$ | ACPL-K370 | | 13.8 | 70 | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF; Note 3 | 10 |
| | | ACPL-K376 | | 13.3 | 70 | µs | | |
| | | ACPL-K370 | | 8.5 | 45 | µs | $R_L$ = 1.8 kΩ, $C_L$ = 15 pF; Note 3 | |
| | | ACPL-K376 | | 6.4 | 45 | µs | | |
| Output Rise Time (10-90%) | $t_R$ | ACPL-K370 | | 25 | | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF | 11 |
| | | ACPL-K376 | | 24 | | µs | | |
| Output Fall Time (90-10%) | $t_F$ | ACPL-K370 | | 0.3 | | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF | 11 |
| | | ACPL-K376 | | 0.4 | | µs | | |
| **$V_{CC}$ = 3.3 V** | | | | | | | | |
| Propagation Delay Time to Logic Low at Output | $t_{PHL}$ | ACPL-K370 | | 4 | 7.5 | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF; Note 2 | |
| | | ACPL-K376 | | 6.8 | 12.5 | µs | | |
| | | ACPL-K370 | | 4 | 7.5 | µs | $R_L$ = 1.8 kΩ, $C_L$ = 15 pF; Note 2 | |
| | | ACPL-K376 | | 6.9 | 12.5 | µs | | |
| Propagation Delay Time to Logic High at Output | $t_{PLH}$ | ACPL-K370 | | 19 | 90 | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF; Note 3 | |
| | | ACPL-K376 | | 18.5 | 90 | µs | | |
| | | ACPL-K370 | | 12.8 | 70 | µs | $R_L$ = 1.8 kΩ, $C_L$ = 15 pF; Note 3 | |
| | | ACPL-K376 | | 12.5 | 70 | µs | | |
| Output Rise Time (10-90%) | $t_R$ | ACPL-K370 | | 27 | | µs | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF | |
| | | ACPL-K376 | | 26 | | µs | | |
| Output Fall Time (90-10%) | $t_F$ | ACPL-K370 | | 0.3 | | µs | $R_L$ = 4.7 kΩ, $C_L$= 30 pF | |
| | | ACPL-K376 | | 0.5 | | µs | | |
| **$V_{CC}$ = 3 V to 5.5 V** | | | | | | | | |
| Common Mode Transient Immunity at Logic High Output | $\|CM_H\|$ | | | 10 | | kV/µs | $I_{IN}$ = 0 mA, $R_L$ = 4.7 kΩ, $V_{O,MIN}$ = 2 V, $V_{CM}$ = 1500 V; Notes 4, 5 | |
| Common Mode Transient Immunity at Logic Low Output | $\|CM_L\|$ | ACPL-K370 | | 1 | | kV/µs | $I_{IN}$ = 3.11 mA, $R_L$ = 4.7 kΩ, $V_{O,MAX}$ = 0.8 V, $V_{CM}$ = 500 V; Notes 4, 5 | |
| | | ACPL-K376 | | 1 | | kV/µs | $I_{IN}$ = 1.56 mA, $R_L$ = 4.7 kΩ, $V_{O,MAX}$ = 0.8 V, $V_{CM}$ = 500 V; Notes 4, 5 | |

Notes:

1. All typical values are at $T_A$ = 25°C unless otherwise stated.
2. The $t_{PHL}$ propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse. $C_L$ includes probe and stray wiring capacitance.
3. The $t_{PLH}$ propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 µs fall time) to the 1.5 V level on the trailing edge of the output pulse. $C_L$ includes probe and stray wiring capacitance.
4. Common mode transient immunity with a logic "High" level is the maximum tolerable (positive) $dV_{CM}/dt$ on the leading edge of the common mode pulse, $V_{CM}$, to insure that the output will remain in a logic "High" state (i.e., $V_O$ > 2.0 V). Common mode transient immunity in logic "Low" level is the maximum tolerable (negative) $dV_{CM}/dt$ on the trailing edge of the common mode pulse signal, $V_{CM}$, to insure that the output will remain in a logic "Low" state (i.e., $V_O$ < 0.8 V).
5. In applications where $dV_{CM}/dt$ may exceed 50 kV / µs (such as when a static discharge occurs), a series resistor, $R_{CC}$, should be included to protect the detector IC from destructive high surge currents. The recommended value for $R_{CC}$ is 240 Ω per volt of allowable drop in $V_{CC}$ (between pin 8 and $V_{CC}$) with a minimum value of 240 Ω.

**Table 8. Package Characteristics**

Over recommended temperature range of $T_A$ = –40°C to 105°C unless otherwise specified.

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage | $V_{ISO}$ | 5000 | | | Vrms | RH ≤ 50%, t = 1 min; $T_A$ = 25°C; Notes 1 to 3 |
| Input-Output Resistance | $R_{I-O}$ | | $10^{12}$ | | Ω | $V_{I-O}$ = 500 Vdc; Note 2 |
| Input-Output Capacitance | $C_{I-O}$ | | 0.6 | | pF | f = 1 MHz, $V_{I-O}$ = 0 Vdc; Note 2 |

Notes:
1. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Avago Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.
2. Device considered a two terminal device: pins 1, 2, 3, 4 connected together, and pins 5, 6, 7, 8 connected together.
3. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).

## Typical Performance Plots

Unless otherwise noted, $T_A$ = 25°C.

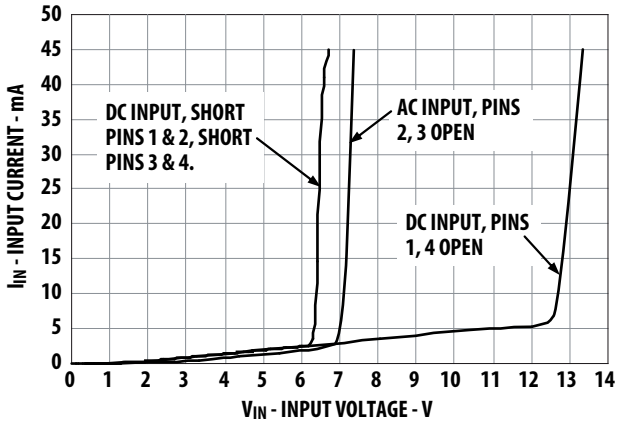
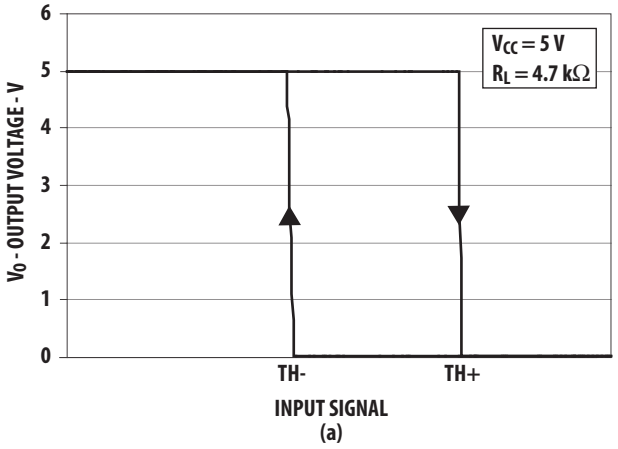



**Figure 4. Typical input characteristics $I_{IN}$ vs. $V_{IN}$ (AC voltage is an instantaneous value).**




| Input Signal | Device | TH+ | TH– | Input Connection |
|---|---|---|---|---|
| $I_{TH}$ | ACPL-K370 | 2.77mA | 1.44mA | PINS 2, 3 OR 1, 4 |
| | ACPL-K376 | 1.32mA | 0.68mA | |
| $V_{TH(DC)}$ | ALL | 3.8V | 2.59V | PINS 2, 3 |
| $V_{TH(AC)}$ | ALL | 5V | 3.8V | PINS 1, 4 |

(b)

**Figure 5. (a) Typical transfer characteristics, and (b) Input threshold levels.**

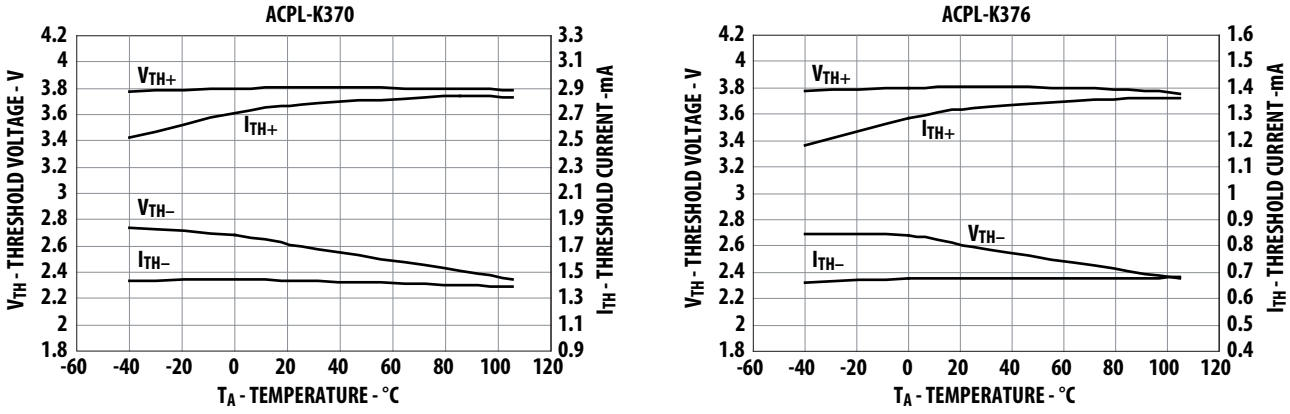



**Figure 6. Typical DC threshold levels vs. temperature for (a) ACPL-K370, and (b) ACPL-K376.**

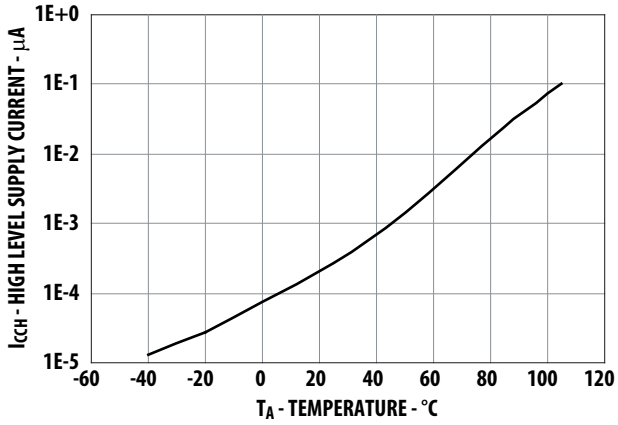



**Figure 7. Typical high level supply current, $I_{CCH}$ vs. temperature.**

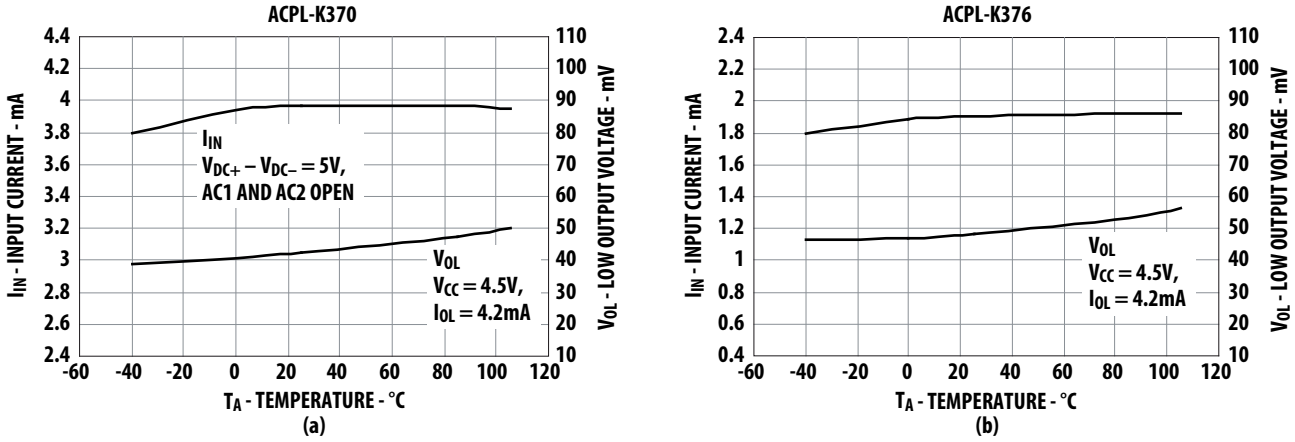



**Figure 8. Typical input current, $I_{IN}$, and low level output voltage, $V_{OL}$ vs. temperature for (a) ACPL-K370 and (b) ACPL-K376.**

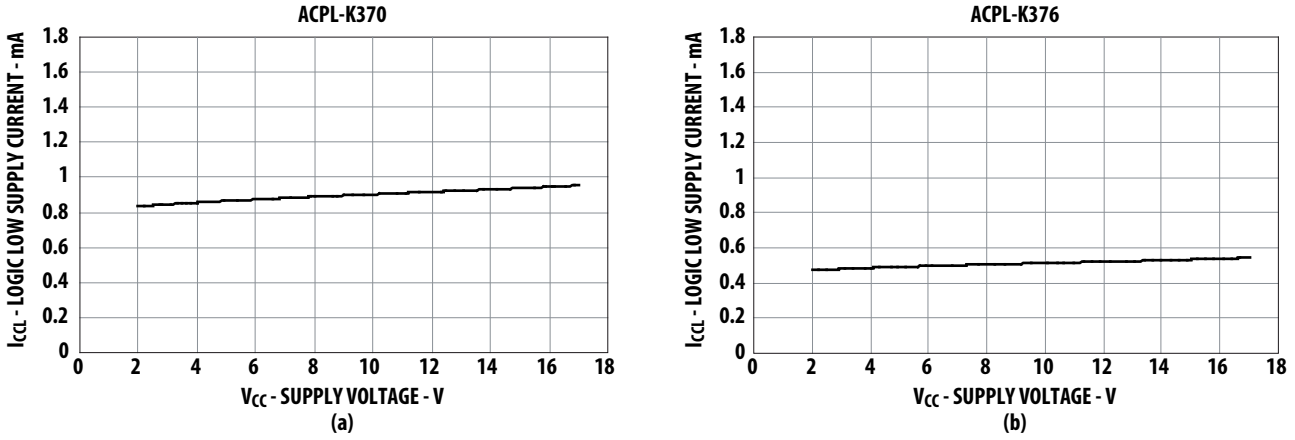



**Figure 9. Typical logic low supply current vs. supply voltage for (a) ACPL-K370 and (b) ACPL-K376.**

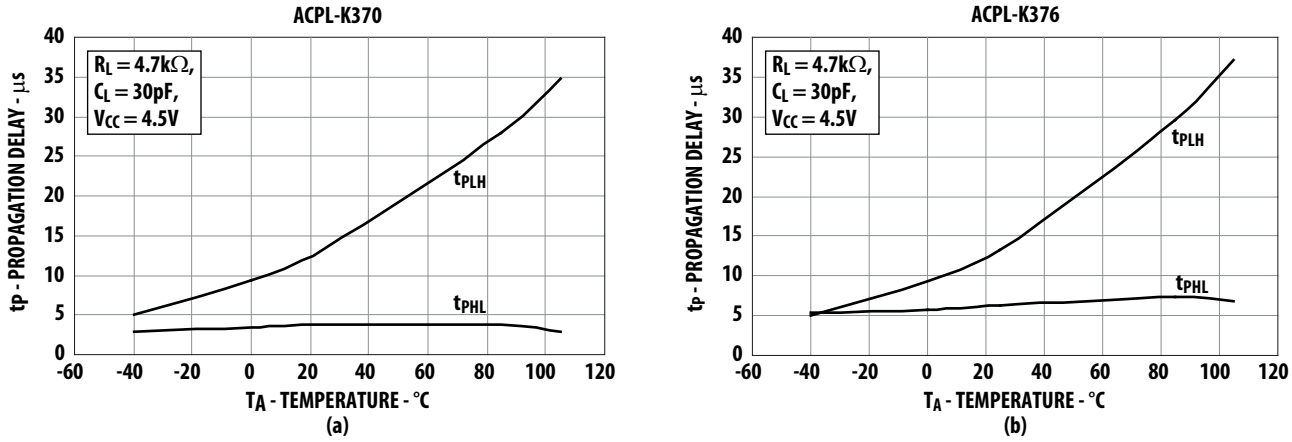



**Figure 10. Typical propagation delay vs. temperature for (a) ACPL-K370 and (b) ACPL-K376.**

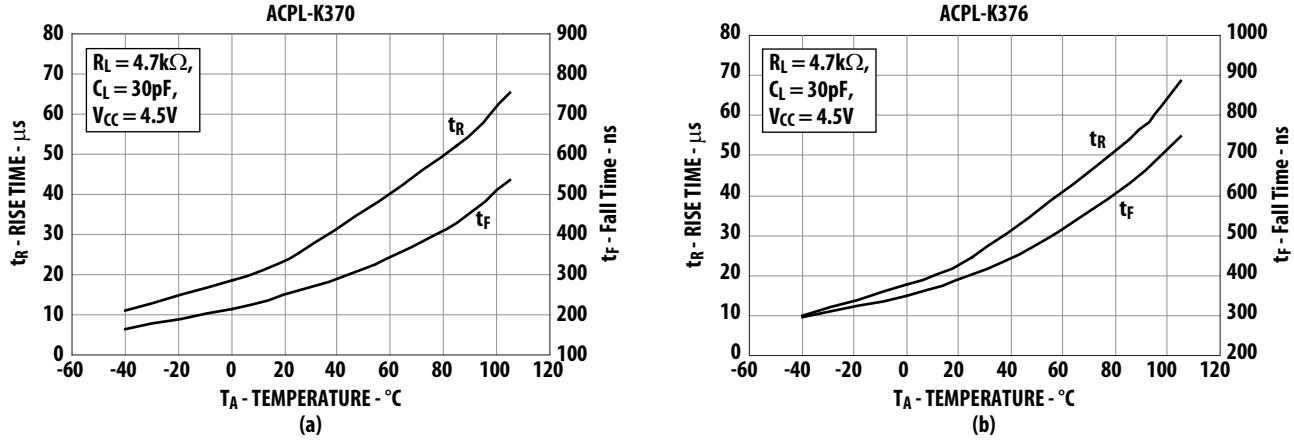



**Figure 11. Typical rise, fall times vs. temperature for (a) ACPL-K370,and (b) ACPL-K376.**

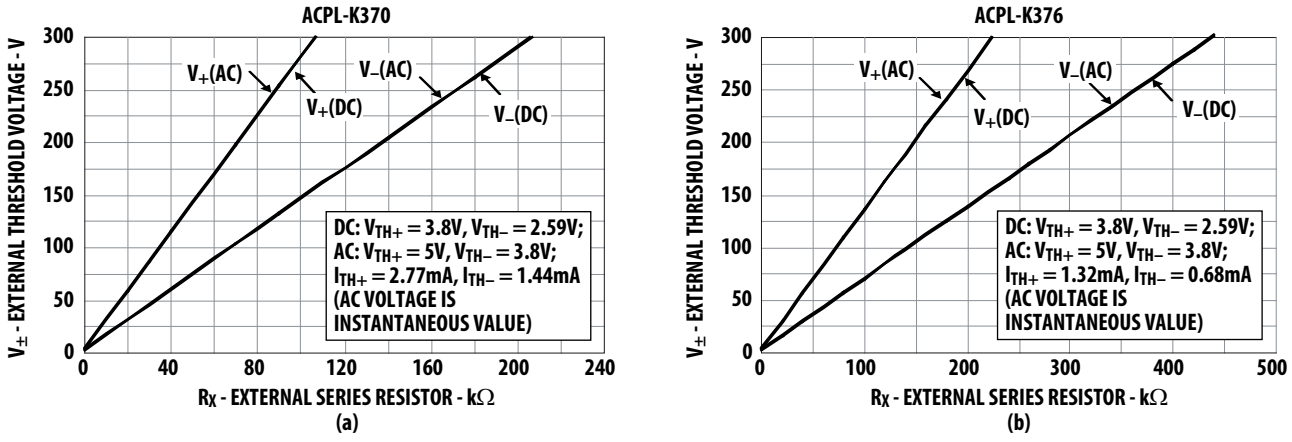



**Figure 12. Typical external threshold characteristics, $V_\pm$ vs. $R_X$ for (a) ACPL-K370 and (b) ACPL-K376.**

## Electrical Considerations

The ACPL-K370/K376 optocouplers have internally temperature compensated, predictable voltage and current threshold points. This allows a single external resistor, $R_X$, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, the approximate $R_x$ value is shown in Figure 12. Equation 1 can be used to calculate Rx.

$V_+$ and $V_-$ voltage threshold levels can be simultaneously set with two resistors, $R_X$ and $R_P$, as shown in Figure 13 and determined by Equations 4 and 5.

$R_X$ can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the ACPL-K370/K376 in combination with $R_X$ and $R_P$ can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 4). It is recommended that the low clamp condition be used when possible. The low clamp condition in conjunction with the low input current feature will ensure extremely low input power dissipation.

In applications where $dV_{CM}/dt$ may be extremely large (such as with a static discharge), a series resistor, $R_{CC}$, should be connected in series with $V_{CC}$ and pin 8 to protect the detector IC from destructive high surge currents. The recommended value for $R_{CC}$ is 240 Ω per volt of allowable drop in $V_{CC}$ (between Pin 8 and $V_{CC}$) with a minimum value of 240 Ω. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μF be placed between pins 5 and 8 to reduce the effect of power supply noise.

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pull-up resistor of 1.5 kΩ and 20 μF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For AC input applications, a filter capacitor can be placed across the DC input terminals for either signal or transient filtering.

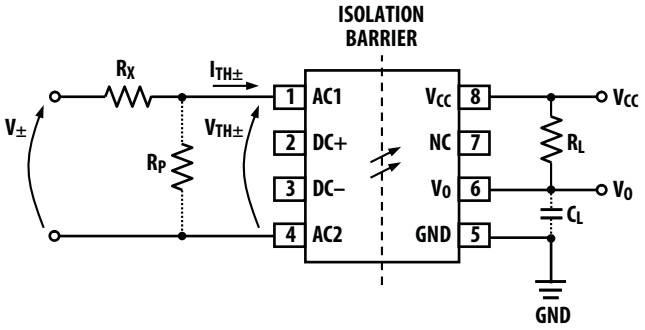



**Figure 13. External threshold voltage level selection.**

Either AC (pins 1 and 4) or DC (pins 2 and 3) input can be used to determine external threshold levels. For single specifically selected external threshold voltage level $V_+$ or $V_-$, $R_X$ can be determined without use of $R_P$ via:

$$R_X = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \qquad \textbf{Equation 1}$$

For dual specifically selected external threshold voltage levels, $V_+$ and $V_-$, the use of $R_X$ and $R_P$ will permit this selection. Two equations can be written:

$$V_+ = R_x \left( I_{TH+} + \frac{V_{TH+}}{R_P} \right) + V_{TH+} \qquad \textbf{Equation 2}$$

$$V_- = R_x \left( I_{TH-} + \frac{V_{TH-}}{R_P} \right) + V_{TH-} \qquad \textbf{Equation 3}$$

Solving these equations for $R_X$ and $R_P$ yields the following two expressions:

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \qquad \textbf{Equation 4}$$

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \qquad \textbf{Equation 5}$$

where

$V_+$ and $V_-$ are the desired external voltage threshold levels, and values for $V_{TH\pm}$ and $I_{TH\pm}$ are found from the data sheet.

Equations 4 and 5 are valid only if the conditions of Equations 6 or 7 are met. With the $V_{TH\pm}$ and $I_{TH\pm}$ values, the denominator of Equation 4 is checked to see if it is positive or negative. If it is positive, then the following ratios must be met:

$$\frac{V_+}{V-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}} \qquad \textbf{Equation 6}$$

Conversely, if the denominator of Equation 4 is negative, then the following ratios must hold:

$$\frac{V_+}{V-} \leq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}} \qquad \textbf{Equation 7}$$

Refer to Application Note 1004 for more application information and worked out examples.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**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