

SN74ALS746 OCTAL BUFFER AND LINE DRIVER WITH INPUT PULLUP RESISTORS

SDAS052A – AUGUST 1984 – REVISED JANUARY 1995

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Pullup Resistors Added for Data-Bus Termination
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

description

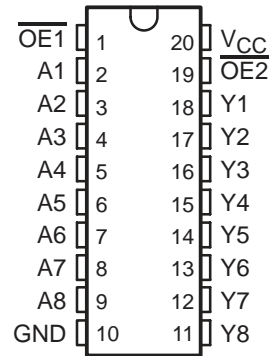
This octal buffer and line driver is designed to have the performance of the 'ALS240A and, at the same time, offers a pinout with inputs and outputs on opposite sides of the package. This arrangement facilitates printed-circuit-board layout. In addition, 20-kΩ resistors have been added between all inputs and V_{CC} . This eliminates adding external resistors in applications where the data bus must be at a high level when all other connecting devices are at a high-impedance state.

The 3-state control gate is a 2-input NOR such that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

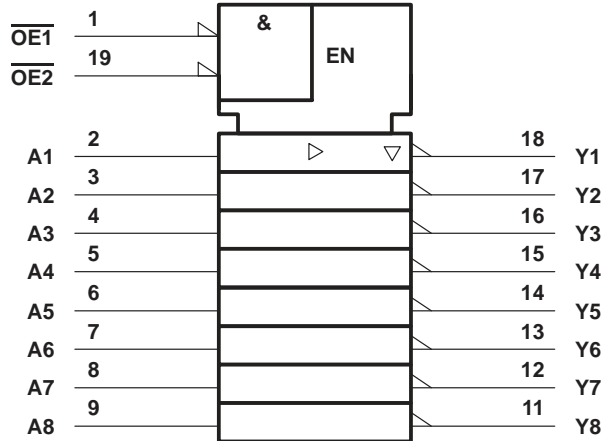
The SN74ALS746 provides inverted data at the outputs.

The SN74ALS746 is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE
(TOP VIEW)

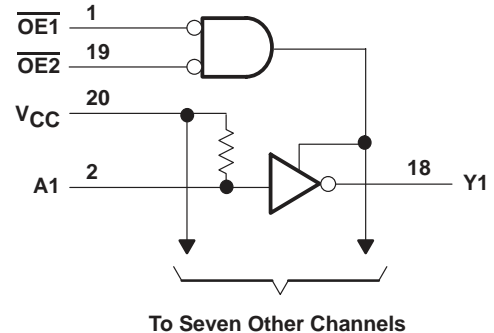


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



All input pullup resistors are 20 kΩ.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			-15	mA
I_{OL} Low-level output current			24	mA
T_A Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5 V$, $I_I = -18 mA$			-1.2	V
V_{OH}	$V_{CC} = 4.5 V$ to $5.5 V$, $I_{OH} = -0.4 mA$	$V_{CC} - 2$			V
	$V_{CC} = 4.5 V$, $I_{OH} = -3 mA$	2.4	3.2		
	$V_{CC} = 4.5 V$, $I_{OH} = -15 mA$	2			
V_{OL}	$V_{CC} = 4.5 V$	$I_{OL} = 12 mA$	0.25	0.4	V
		$I_{OL} = 24 mA$	0.35	0.5	
I_{OZH}	$V_{CC} = 5.5 V$, $V_O = 2.7 V$			20	μA
I_{OZL}	$V_{CC} = 5.5 V$, $V_O = 0.4 V$			-20	μA
I_I	$V_{CC} = 5.5 V$	$V_I = 5.5 V$		0.1	mA
		$V_I = 7 V$		0.1	
I_{IH}	$V_{CC} = 5.5 V$, $V_I = 2.7 V$			-0.2	mA
				20	
I_{IL}	$V_{CC} = 5.5 V$, $V_I = 0.4 V$			-0.6	mA
				-0.1	
$I_{O\text{§}}$	$V_{CC} = 5.5 V$, $V_O = 2.25 V$	-30		-112	mA
I_{CC}	$V_{CC} = 5.5 V$	Outputs high	7	12	mA
		Outputs low	13	22	
		Outputs disabled	11	19	

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			MIN	MAX	
t _{PLH}	A	Y	3	12	ns
t _{PHL}			2	9	
t _{PZH}	$\overline{\text{OE}}$	Y	5	15	ns
t _{PZL}			8	20	
t _{PHZ}	$\overline{\text{OE}}$	Y	1	10	ns
t _{PLZ}			2	12	

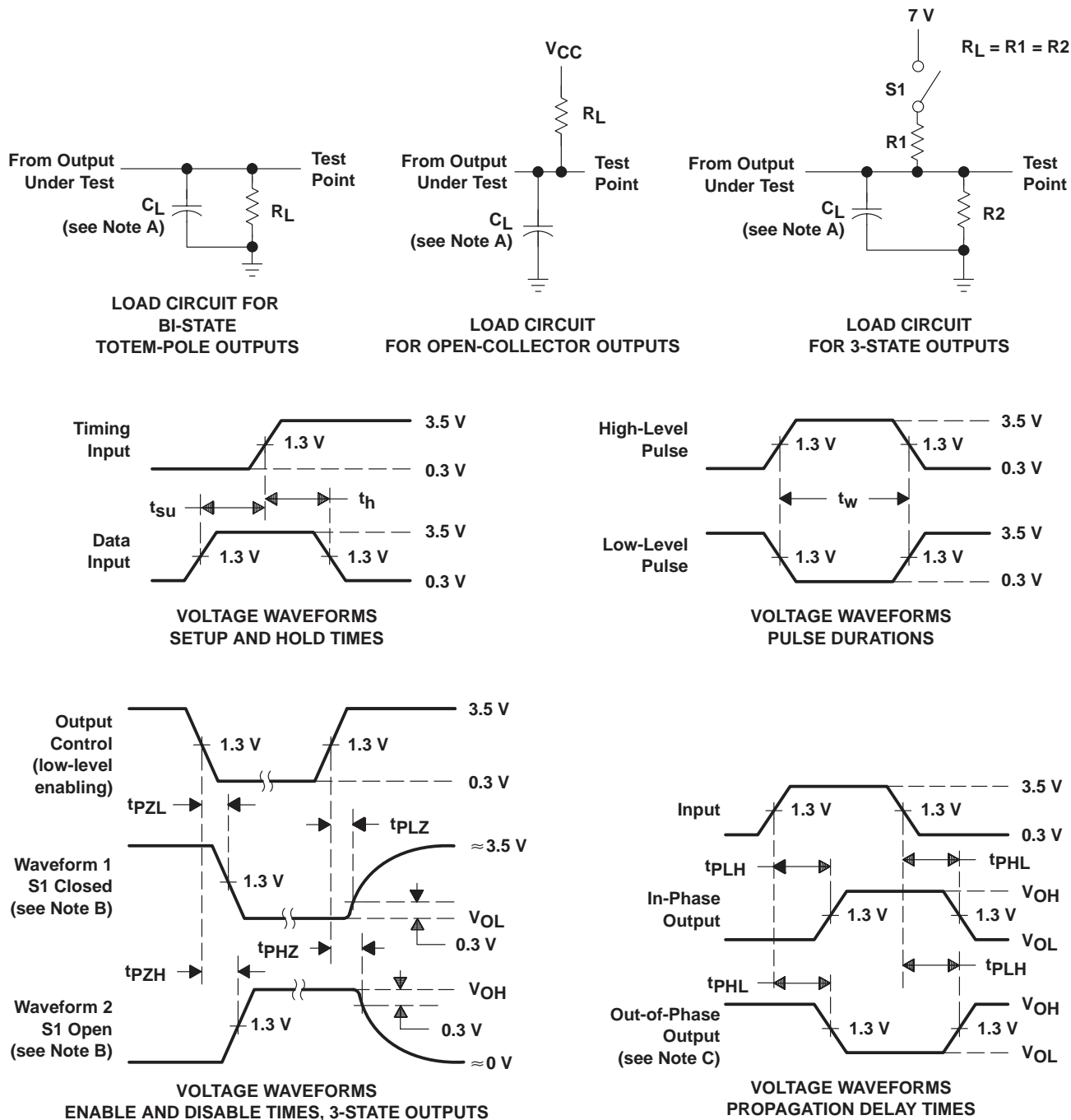
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74ALS746DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS746DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS746N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

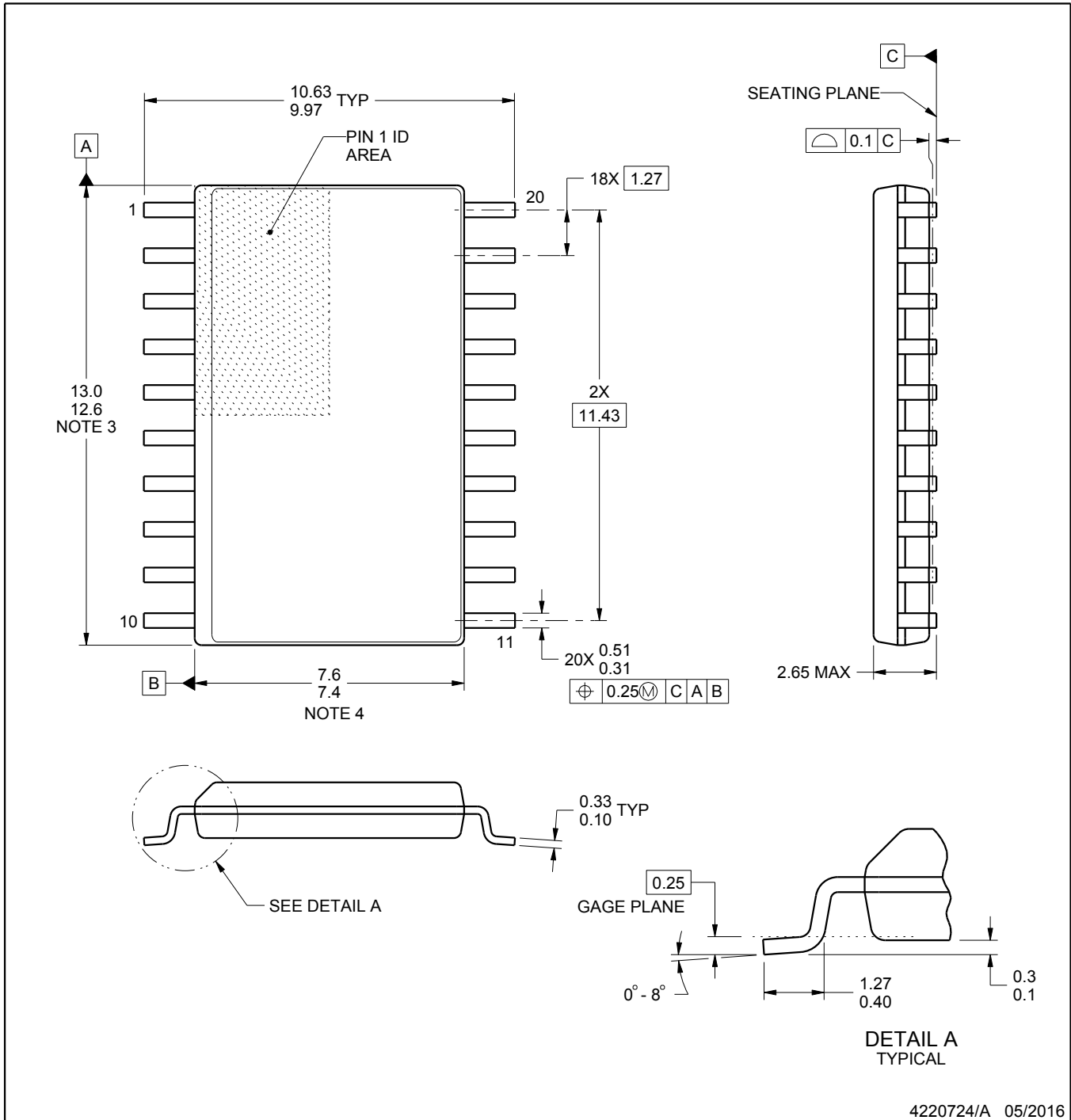
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

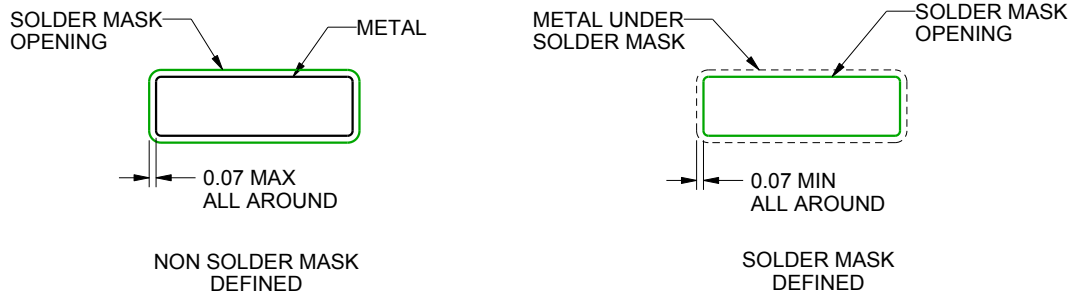
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

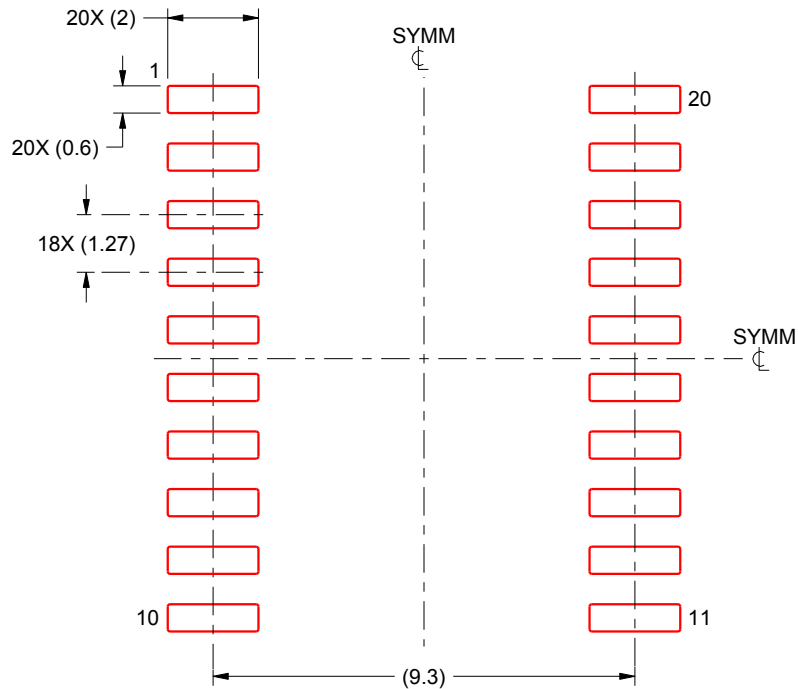
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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