TPS40170 4.5 V to 60 V, Wide-Input Synchronous PWM Buck Controller

1 Features

- Wide Input Voltage Range from 4.5 V to 60 V
- 600 mV Reference Voltage with 1% Accuracy
- Programmable UVLO and Hysteresis
- Voltage Mode Control With Voltage Feed Forward
- Programmable Frequency Between 100 kHz and 600 kHz
- Bi-directional -Frequency Synchronization With Master/Slave Option
- Low-side FET Sensing Overcurrent Protection and High-Side FET Sensing Short-Circuit Protection With Integrated Thermal Compensation
- Programmable Closed Loop Soft-Start
- Supports Pre-Biased Outputs
- Thermal Shutdown at 165°C with Hysteresis
- Voltage Tracking
- Powergood
- ENABLE with 1-µA Low Current Shutdown
- 8.0-V and 3.3-V LDO Output
- Integrated Bootstrap Diode
- 20-Pin 3.5 mm × 4.5 mm VQFN (RGY) Package
- Create a Custom Design with WEBENCH Tools

2 Applications

- POL Modules
- Wide Input Voltage, High-Power Density DC - DC Converters for Industrial, Networking and Telecom Equipment

3 Description

TPS40170 is a full-featured, synchronous PWM buck controller that operates at an input voltage between 4.5 V and 60 V and is optimized for high-power density, high-reliability DC-DC converter applications. The controller implements voltage-mode control with input voltage feed-forward compensation that enables instant response to input voltage change. The switching frequency is programmable from 100 kHz to 600 kHz.

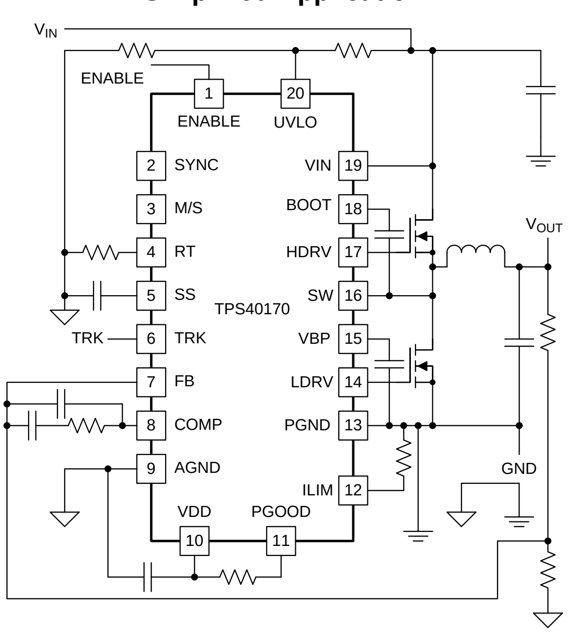
The TPS40170 has a complete set of system protection and monitoring features such as programmable undervoltage lockout (UVLO), programmable overcurrent protection (OCP) by sensing the low-side FET, selectable short-circuit protection (SCP) by sensing the high-side FET and thermal shutdown. The ENABLE pin allows for system shutdown in a low-current (1 µA typical) mode. The controller supports pre-biased output, provides an open-drain PGOOD signal, and has closed-loop soft-start, output voltage tracking and adaptive dead-time control.

Device Information(1)

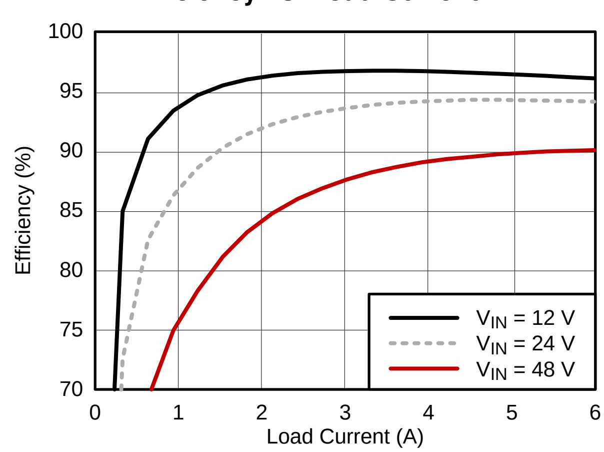
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40170	VQFN (20)	3.50 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application



Efficiency vs. Load Current



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4 Revision History

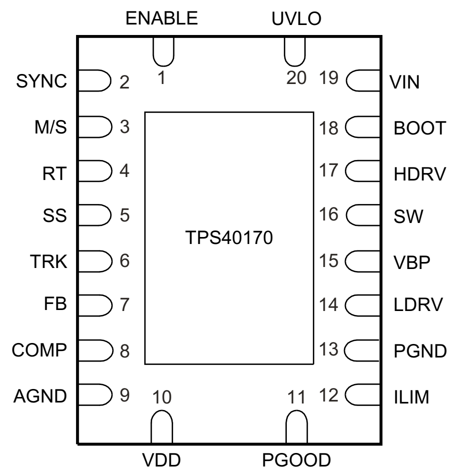
Changes from Revision B (December 2014) to Revision C	Page

Changes from Revision A (November 2013) to Revision B	Page
• Added *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	3

Changes from Original (March 2011) to Revision A	Page
• Deleted *Ordering Information* table. Replaced with *Package Option Addenda* inserted after the last page of this data sheet.	3
• Added clarity to Figure 20	16
• Added significant clarity to and corrected typographic errors in DESIGN EXAMPLE	32

5 Pin Configuration and Functions

RGY PACKAGE
QFN-20
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9	—	Analog signal ground. This pin must be electrically connected to power ground PGND externally.
BOOT	18	O	Boot capacitor node for high-side FET gate driver. The boot capacitor is connected from this pin to SW.
COMP	8	O	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the FB pin.
ENABLE	1	I	This pin must be high for the device to be enabled. If this pin is pulled low, the device is put in a low-power consumption shutdown mode.
FB	7	I	Negative input to the error amplifier. The output voltage is fed back to this pin through a resistor divider network.
HDRV	17	O	Gate driver output for the high-side FET.
ILIM	12	I	A resistor from this pin to PGND sets the overcurrent limit. This pin provides source current used for overcurrent protection threshold setting.
LDRV	14	O	Gate driver output for the low-side FET. Also, a resistor from this pin to PGND sets the multiplier factor to determine short-circuit current limit. If no resistor is present the multiplier defaults to 7 times the ILIM pin voltage.
M/S	3	I	Master or slave mode selector pin for frequency synchronization. This pin must be tied to VIN for master mode. In the slave mode this pin must be tied to AGND or left floating. If the pin is tied to AGND, the device synchronizes with a 180° phase shift. If the pin is left floating, the device synchronizes with a 0° phase shift.
PGND	13	—	Power ground. This pin must externally connect to the AGND at a single point.
PGOOD	11	O	Power good indicator. This pin is an open-drain output pin and a 10 kΩ pull-up resistor is recommended to be connected between this pin and VDD.
RT	4	I	A resistor from this pin to AGND sets the oscillator frequency. Even if operating in slave mode, it is required to have a resistor at this pin to set the free running switching frequency.
SS	5	I	Soft-start. A capacitor must be connected at this pin to AGND. The capacitor value sets the soft-start time.
SW	16	I	This pin must connect to the switching node of the synchronous buck converter. The high-side and low-side FET current sensing are also done from this node.
SYNC	2	I/O	Synchronization. This is a bi-directional pin used for frequency synchronization. In the master mode, it is the SYNC output pin. In the slave mode, it is a SYNC input pin. If unused, this pin can be left open.
TRK	6	I	Tracking. External signal at this pin is used for output voltage tracking. This pin goes directly to the internal error amplifier as a positive reference. The lesser of the voltages between V_{TRK} and the internal 600 mV reference sets the output voltage. If not used, this pin should be pulled up to VDD.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
UVLO	20	I	Undervoltage lockout. A resistor divider on this pin from VIN to AGND can be used to set the UVLO threshold.
VBP	15	O	8 V regulated output for gate driver. A ceramic capacitor with a value from 1 µF to 10 µF must be connected from this pin to PGND and placed close to this pin.
VDD	10	O	3.3 V regulated output. A ceramic by-pass capacitor with a value from 0.1 µF to 1 µF must be connected from this pin to AGND and placed close to this pin.
VIN	19	I	Input voltage for the controller which is also the input voltage for the DC/DC converter. A ceramic by-pass capacitor with a value from 0.1 µF to 1 µF must be connected from this pin to PGND and placed close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	62	V
	M/S	–0.3	VIN	
	UVLO	–0.3	16	
	SW	–5	V_{VIN}	
	SW (for duration less than 200 ns)	–10	V_{VIN}	
	BOOT		V_{SW} + 8.8	
Output voltage	HDRV	V_{SW}	BOOT	V
	BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	–0.3	8.8	
	VBP, LDRV, COMP, RT, ENABLE, PGOOD, SYNC	–0.3	8.8	
	VDD, FB, TRK, SS, ILIM	–0.3	3.6	
	AGND-PGND, PGND-AGND	200	200	mV
	PowerPAD to AGND (must be electrically connected external to device)		0	
Lead Temperature			260	°C
Operating junction temperature	T_J	–40	125	°C

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)		1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	4.5	60	V
T_J	Operating junction temperature range	-40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS40170 RGY 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	36.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for -40ºC ≤ T_J ≤ 125ºC, V_{VIN}=12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN}	Input voltage range		4.5		60	V
I_{SD}	Shutdown current	V_{ENABLE} < 100 mV		1	2.5	µA
I_Q	Operating current, drivers not switching	V_{ENABLE} ≥ 2 V, f_{SW} = 300 kHz			4.5	mA
ENABLE						
V_{DIS}	ENABLE pin voltage to disable the device				100	mV
V_{EN}	ENABLE pin voltage to enable the device		600			mV
I_{ENABLE}	ENABLE pin source current				300	nA
8-V AND 3.3-V REGULATORS						
V_{BP}	8 V regulator output voltage	V_{ENABLE} ≥ 2 V, 8.2 V < V_{IN} ≤ 60 V, 0 mA < I_{IN} < 20 mA	7.8	8.0	8.3	V
V_{DO}	8 V regulator dropout voltage, V_{IN-BP}	4.5 < V_{IN} ≤ 8.2 V, V_{EN} ≥ 2.0 V, I_{IN} = 10 mA		110	200	mV
V_{VDD}	3.3 V regulator output voltage	V_{ENABLE} ≥ 2 V, 4.5 V < V_{IN} ≤ 60 V, 0 mA < I_{IN} < 5 mA	3.22	3.30	3.42	V
FIXED AND PROGRAMMABLE UVLO						
V_{UVLO}	Programmable UVLO ON voltage (at UVLO pin)	V_{ENABLE} ≥ 2 V	878	900	919	mV
I_{UVLO}	Hysteresis current out of UVLO pin	V_{ENABLE} ≥ 2 V , UVLO pin > V_{UVLO}	4.06	5.00	6.20	µA
$VBP_{(ON)}$	VBP turn-on voltage	V_{ENABLE} ≥ 2 V, UVLO pin > V_{UVLO}	3.85		4.40	V
$VBP_{(OFF)}$	VBP turn-off voltage	V_{ENABLE} ≥ 2 V, UVLO pin > V_{UVLO}	3.60		4.05	V
$VBP_{(HYS)}$	VBP UVLO Hysteresis voltage	V_{ENABLE} ≥ 2 V, UVLO pin > V_{UVLO}	180		400	mV
REFERENCE						
V_{REF}	Reference voltage (+ input of the error amplifier)	T_J = 25°C, 4.5 V < V_{IN} ≤ 60 V	594	600	606	mV
		–40°C ≤ T_J ≤ 125ºC, 4.5 V < V_{IN} ≤ 60 V	591	600	609	mV
OSCILLATOR						
f_{SW}	Switching frequency	Range (typical)	100		600	kHz
		R_{RT} = 100 kΩ, 4.5 V <V_{IN} ≤ 60 V	90	100	110	kHz
		R_{RT} = 31.6 kΩ, 4.5 V <V_{IN} ≤ 60 V	270	300	330	kHz
		R_{RT} = 14.3 kΩ, 4.5 V <V_{IN} ≤ 60 V	540	600	660	kHz
V_{VALLEY}	Valley voltage		0.7	1	1.2	V
K_{PWM} [1]	PWM Gain (V_{IN} / V_{RAMP})	4.5 V < V_{IN} ≤ 60 V	14	15	16	V/V
PWM AND DUTY CYCLE						
$t_{ON(min)}$ [1]	Minimum controlled pulse	V_{IN} = 4.5 V, f_{SW} = 300 kHz		100	150	ns
		V_{IN} = 12 V, f_{SW} = 300 kHz		75	100	ns
		V_{IN} = 60 V, f_{SW} = 300 kHz		50	80	ns
$t_{OFF(max)}$ [1]	Minimum OFF time	V_{IN} = 12V, f_{SW} = 300 kHz		170	250	ns

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for -40ºC ≤ T_J ≤ 125ºC, V_{VIN}=12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{MAX} (1)	Maximum duty cycle	f_{SW} = 100 kHz, 4.5 V < V_{IN} ≤ 60 V	95%			
		F_{SW} = 300 kHz, 4.5 V < V_{IN} ≤ 60 V	91%			
		f_{SW} = 600 kHz, 4.5 V < V_{IN} ≤ 60 V	82%			
ERROR AMPLIFIER						
GBWP (2)	Gain bandwidth product		7	10	13	MHz
A_{OL} (2)	Open-loop gain		80	90	95	dB
I_{IB}	Input bias current				100	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	2			mA
I_{EAOM}	Output sink current	V_{FB} = 1 V	2			mA
PROGRAMMABLE SOFT-START						
$I_{SS(source,start)}$	Soft-start source current at V_{SS} < 0.5 V	V_{SS} = 0.25 V	42	52	62	µA
$I_{SS(source,normal)}$	Soft-start source current at V_{SS} > 0.5 V	V_{SS} = 1.5 V	9.3	11.6	13.9	µA
$I_{SS(sink)}$	Soft-start sink current	V_{SS} = 1.5 V	0.77	1.05	1.33	µA
$V_{SS(fltH)}$	SS pin HIGH voltage during fault (OC or thermal) reset timing		2.38	2.50	2.61	V
$V_{SS(fltL)}$	SS pin LOW voltage during fault (OC or thermal) reset timing		235	300	375	mV
$V_{SS(steady\_state)}$	SS pin voltage during steady-state		3.25	3.30	3.50	V
$V_{SS(offst)}$	Initial offset voltage from SS pin to error amplifier input		525	650	775	mV
TRACKING						
$V_{TRK(ctrl)}$ (2)	Range of TRK which overrides V_{REF}	4.5 V < V_{IN} ≤ 60 V	0		600	mV
SYNCHRONIZATION (MASTER/SLAVE)						
V_{MSTR}	M/S pin voltage in master mode		3.9		VIN	V
$V_{SLV(0)}$	M/S pin voltage in slave 0 deg mode		1.25		1.75	V
$V_{SLV(180)}$	M/S pin voltage in slave 180 deg mode		0		0.75	V
$I_{SYNC(in)}$	SYNC pin pull-down current	M/S configured as slave- 0 degrees or slave-180 degrees	8	11	14	µA
$V_{SYNC(in\_high)}$	SYNC pin input high-voltage level	M/S configured as slave- 0 degrees or slave-180 degrees	2			V
$V_{SYNC(in\_low)}$	SYNC pin input low-voltage level	M/S configured as slave- 0 degrees or slave-180 degrees			0.8	V
$t_{SYNC(high\_min)}$	Minimum SYNC high pulse-width	M/S configured as slave- 0 degrees or slave-180 degrees	40	50		ns
$t_{SYNC(low\_min)}$	Minimum SYNC low pulse-width	M/S configured as slave- 0 degrees or slave-180 degrees	40	50		ns
GATE DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	C_{LOAD} = 2.2 nF, I_{DRV} = 300 mA	1.37	2.64	3.50	Ω
R_{HDLO}	High-side driver pull-down resistance	C_{LOAD} = 2.2 nF, I_{DRV} = 300 mA	1.08	2.40	3.35	Ω
R_{LDHI}	Low-side driver pull-up resistance	C_{LOAD} = 2.2 nF, I_{DRV} = 300 mA	1.37	2.40	3.20	Ω
R_{LDLO}	Low-side driver pull-down resistance	C_{LOAD} = 2.2 nF, I_{DRV} = 300 mA	0.44	1.10	1.70	Ω
$t_{NON-OVERLAP1}$	Time delay between HDRV fall and LDRV rise	C_{LOAD} = 2.2 nF, V_{HDRV} = 2 V, V_{LDRV} = 2 V		50		ns
$t_{NON-OVERLAP2}$	Time delay between HDRV rise and LDRV fall	C_{LOAD} = 2.2 nF, V_{HDRV} = 2 V, V_{LDRV} = 2 V		60		ns
OVERCURRENT PROTECTION (LOW-SIDE MOSFET SENSING)						
I_{ILIM}	ILIM pin source current	4.5 V < V_{IN} < 60 V, T_J = 25°C	9.00	9.75	10.45	µA
$I_{ILIM,(ss)}$	ILIM pin source current during Soft-start	4.5 V < V_{IN} < 60 V, T_J = 25°C		15		µA
$I_{ILIM,\ Tc}$ (2)	Temperature coefficient of ILIM current	4.5 V < V_{IN} < 60 V		1400		ppm
V_{ILIM} (2)	ILIM pin voltage operating range	4.5 V < V_{IN} < 60 V	50		300	mV
OCP_{TH}	Overcurrent protection threshold (Voltage across low-side FET for detecting overcurrent)	R_{ILIM} = 10 kΩ, I_{ILIM} = 10 µA (V_{ILIM} = 100 mV)	–110	–100	–84	mV
SHORT CIRCUIT PROTECTION HIGH-SIDE MOSFET SENSING)						
$V_{LDRV(max)}$	LDRV pin maximum voltage during calibration	R_{LDRV} = open		300	360	mV
A_{OC3}	Multiplier factor to set the SCP based on OCP level setting at the ILIM pin	R_{LDRV} = 10 kΩ	2.75	3.20	3.60	V/V
A_{OC7}	Multiplier factor to set the SCP based on OCP level setting at the ILIM pin	R_{LDRV} = open	6.40	7.25	7.91	V/V
A_{OC15}	Multiplier factor to set the SCP based on OCP level setting at the ILIM pin	R_{LDRV} = 20 kΩ	13.9	16.4	18.0	V/V

(2) Specified by design. Not production tested.

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for -40ºC ≤ T_J ≤ 125ºC, V_{VIN}=12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
$T_{SD,set}$ (3)	Thermal shutdown set threshold	4.5 V < V_{IN} < 60 V	155	165	175	°C
$T_{SD,reset}$ (3)	Thermal shutdown reset threshold		125	135	145	
T_{hyst} (3)	Thermal shutdown hysteresis			30		
POWERGOOD						
V_{OV}	FB pin voltage upper limit for power good	4.5 V < V_{IN} < 60 V	627	647	670	mV
V_{UV}	FB pin voltage lower limit for power good		527	552	570	
$V_{PG,HYST}$	Power good hysteresis voltage at FB pin		8.5	20.0	32.0	
$V_{PG(out)}$	PGOOD pin voltage when FB pin voltage > V_{OV} or < V_{UV}, I_{PGD}=2 mA				100	
$V_{PG(np)}$	PGOOD pin voltage when device power is removed	V_{IN} is open, 10 kΩ to V_{EXT} = 5 V		1	1.5	V
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I = 20 mA	0.5	0.7	0.9	V
$R_{BOOT-SW}$	Discharge resistor from BOOT to SW			1		MΩ

(3) Specified by design. Not production tested.

6.6 Typical Characteristics

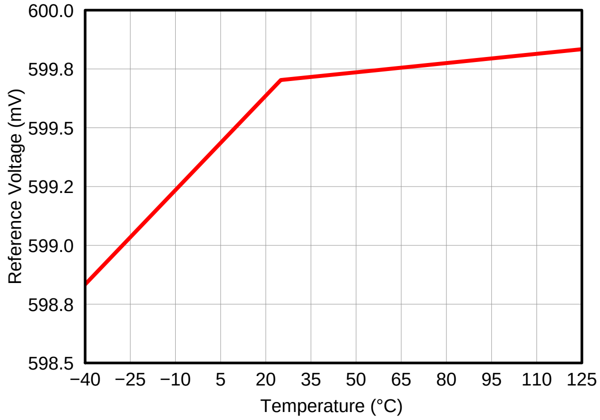


Figure 1. Reference Voltage vs. Junction Temperature

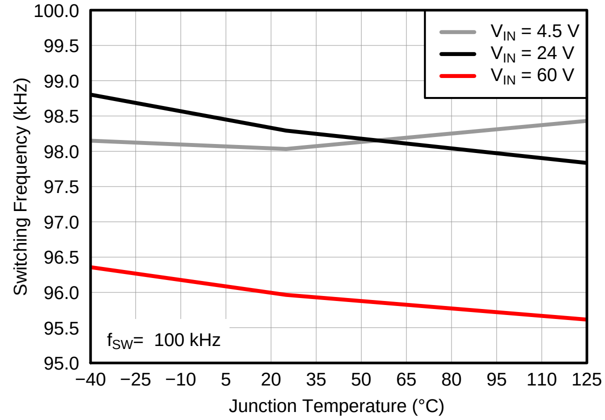


Figure 2. Switching Frequency vs. Junction Temperature (f_{SW} = 100 kHz)

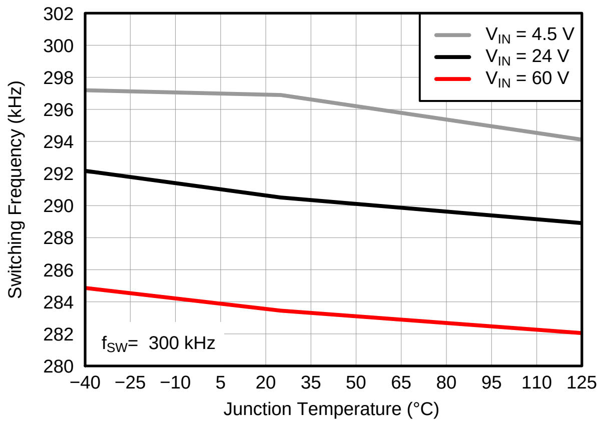


Figure 3. Switching Frequency vs. Junction Temperature (f_{SW} = 300 kHz)

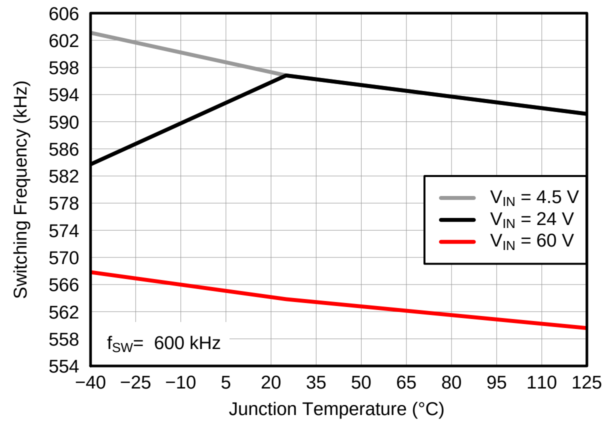


Figure 4. Switching Frequency vs. Junction Temperature (f_{SW} = 600 kHz)

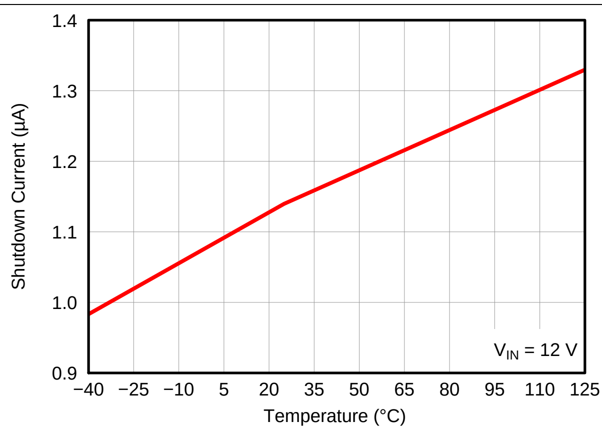


Figure 5. Shutdown Current vs. Junction Temperature

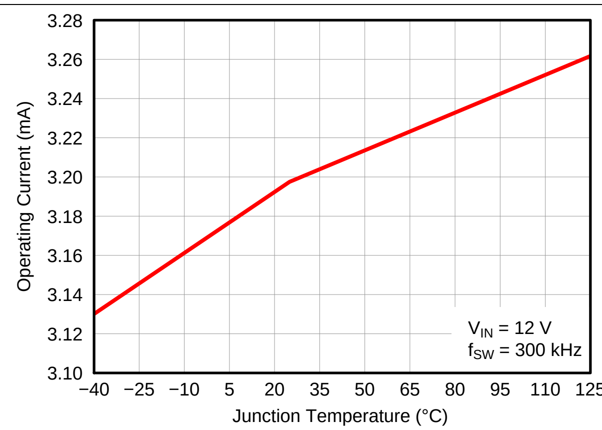


Figure 6. Operating Current vs. Junction Temperature

Typical Characteristics (continued)

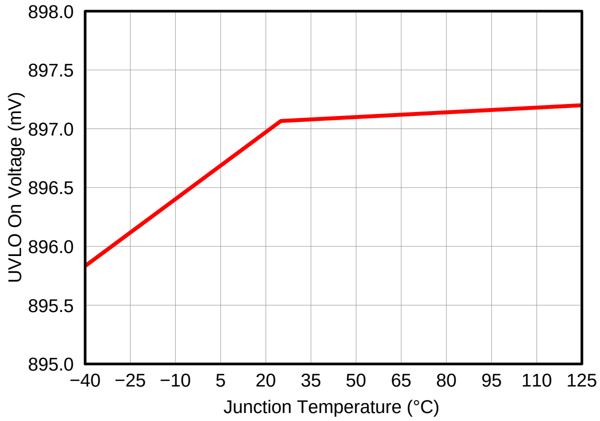


Figure 7. UVLO Pin On Voltage vs. Junction Temperature

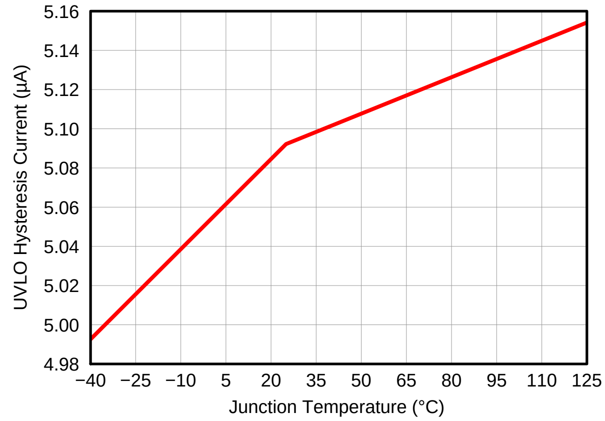


Figure 8. UVLO Pin Hysteresis Current vs. Junction Temperature

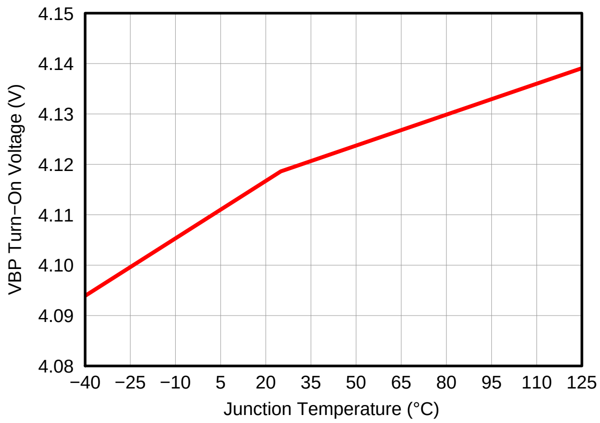


Figure 9. VBP Turn-On Voltage vs. Junction Temperature

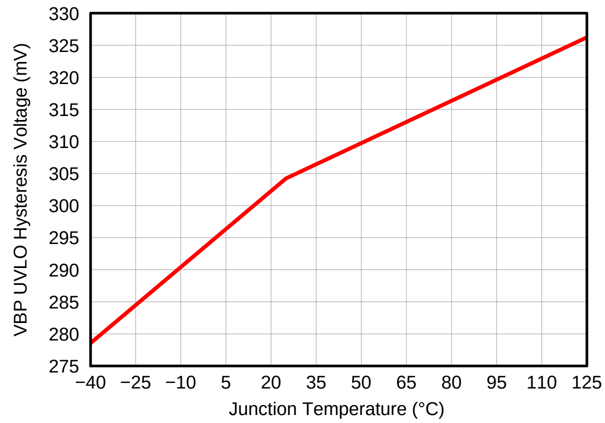


Figure 10. VBP UVLO Hysteresis Voltage

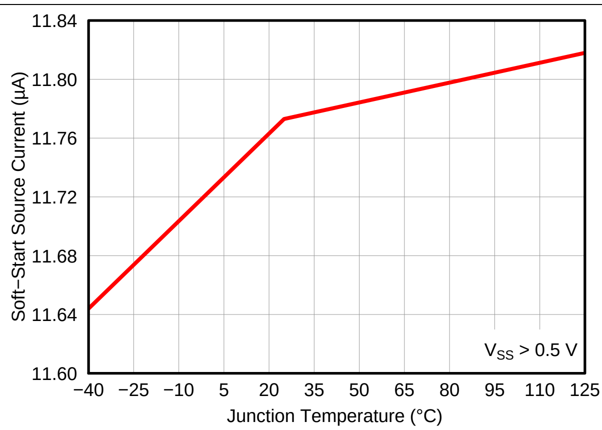


Figure 11. Soft-Start Source Current vs. Junction Temperature (V_{SS} > 0.5 V)

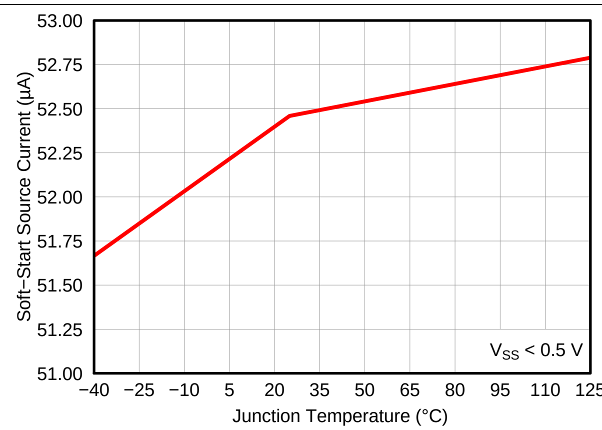


Figure 12. Soft-Start Source Current vs. Junction Temperature (V_{SS} < 0.5 V)

Typical Characteristics (continued)

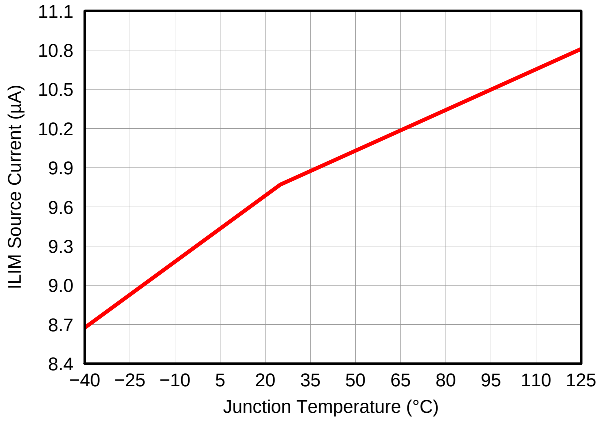


Figure 13. ILIM Source Current vs. Junction Temperature

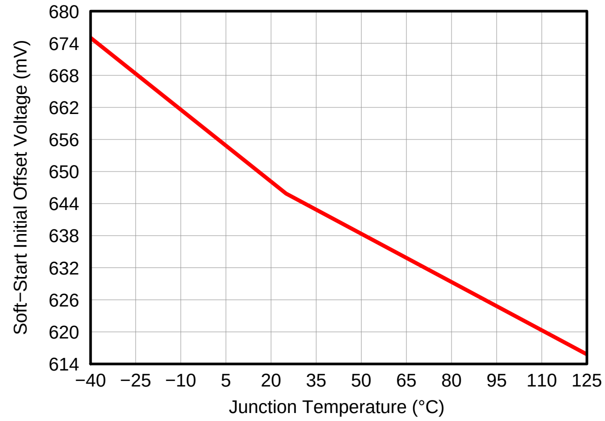


Figure 14. Soft-Start Initial Offset Voltage vs. Junction Temperature

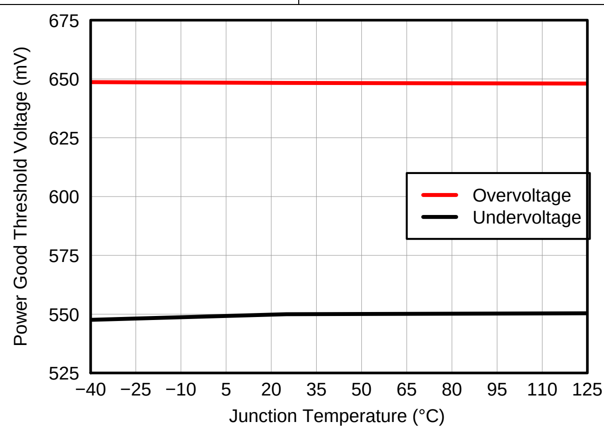


Figure 15. V_{OV}/V_{UV} Power Good Threshold Voltage

7 Detailed Description

7.1 Overview

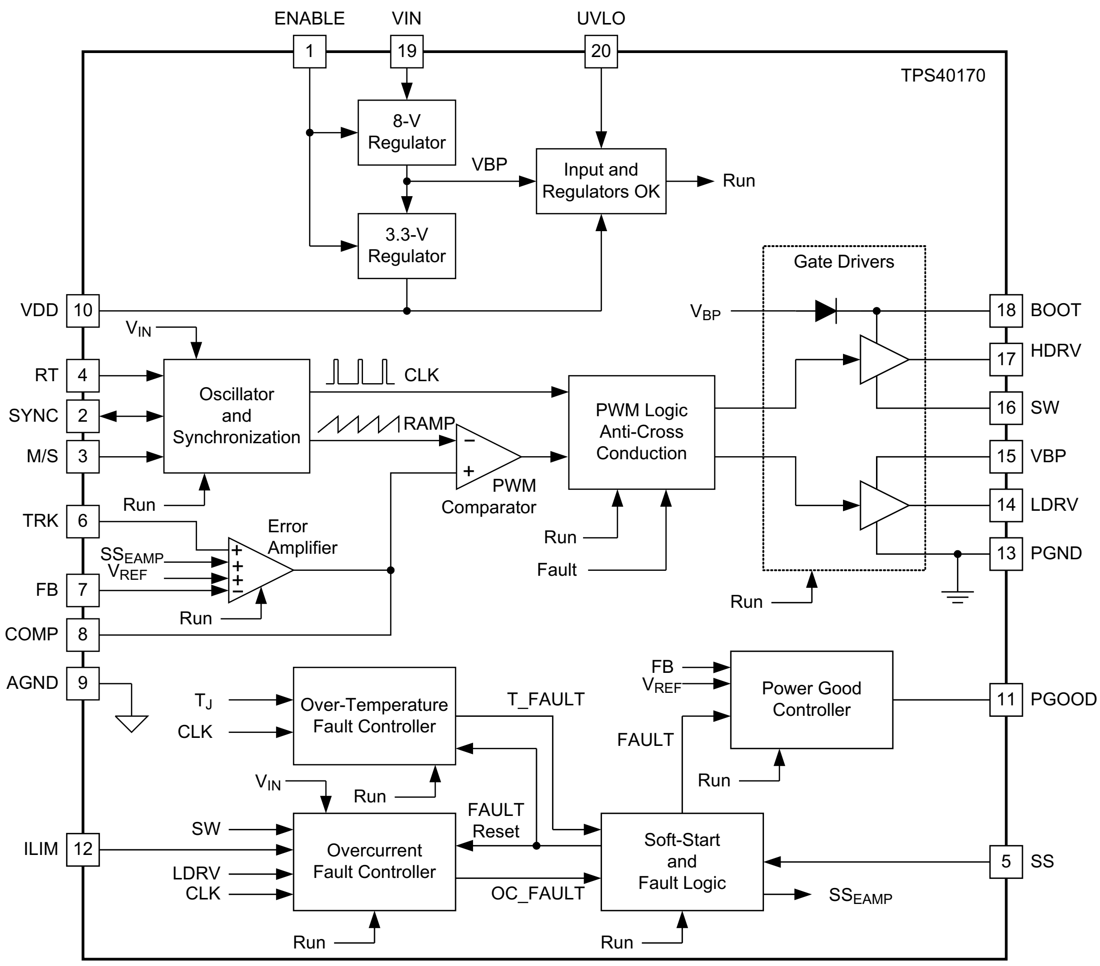
The TPS40170 is a synchronous PWM buck controller that accepts a wide range of input voltage from 4.5 V to 60 V and features voltage-mode control with input-voltage, feed-forward compensation. The switching frequency is programmable from 100 kHz to 600 kHz.

The TPS40170 has a complete set of system protections such as programmable undervoltage lockout (UVLO), programmable overcurrent protection (OCP), selectable short-circuit protection (SCP) and thermal shutdown. The ENABLE pin allows for system shutdown in a low-current (1 µA typical) mode. The controller supports pre-biased outputs, provides an open-drain PGOOD signal, and has closed loop programmable soft-start, output voltage tracking and adaptive dead time control.

The TPS40170 provides accurate output voltage regulation via 1% specified accuracy.

Additionally, the controller implements a novel scheme of bidirectional synchronization with one controller acting as the master other downstream controllers acting as slaves, synchronized to the master in-phase or 180° out-of-phase. Slave controllers can be synchronized to an external clock within ±30% of the internal switching frequency.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 LDO Linear Regulators and Enable

The TPS40170 has two internal low-drop-out (LDO) linear regulators. One has a nominal output voltage of V_{VBP} and is present at the VBP pin. This is the voltage that is mainly used for the gate-driver output. The other linear regulator has an output voltage of V_{VDD} and is present at the VDD pin. This voltage can be used in external low-current logic circuitry. The maximum allowable current drawn from the VDD pin must not exceed 5 mA.

The TPS40170 has a dedicated device enable pin (ENABLE). This simplifies user level interface design because no multiplexed functions exist. If the ENABLE pin of the TPS40170 is higher than V_{EN}, then the LDO regulators are enabled. To ensure that the LDO regulators are disabled, the ENABLE pin must be pulled below V_{DIS}. By pulling the ENABLE pin below V_{DIS}, the device is completely disabled and the current consumption is very low (nominally, 1 µA). Both LDO regulators are actively discharged when the ENABLE pin is pulled below V_{DIS}. A functionally equivalent circuit to the enable circuitry on the TPS40170 is shown in Figure 16.

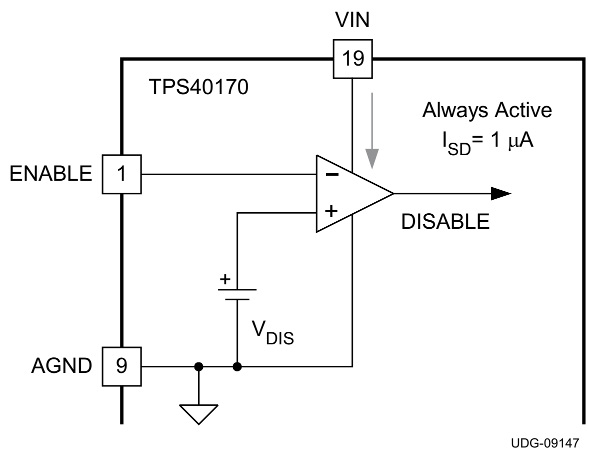


Figure 16. TPS40170 Enable Functional Block

The ENABLE pin must not be allowed to float. If the ENABLE function is not needed for the design, then it is suggested that the ENABLE pin be pulled up to VIN by a high value resistor ensuring that the current into the ENABLE pin does not exceed 10 µA. If it is not possible to meet this clamp current requirement, then it is suggested that a resistor divider from VIN to GND be used to connect to ENABLE pin. The resistor divider should be such that the ENABLE pin should be higher than V_{EN} and lower than 8 V.

NOTE

To avoid potential erroneous behavior of the enable function, the ENABLE signal applied must have a minimum slew rate of 20 V/s.

7.3.2 Input Undervoltage Lockout (UVLO)

The TPS40170 has both fixed and programmable input undervoltage lockout (UVLO). In order for the device to turn ON, all of the following conditions must be met:

- The ENABLE pin voltage must be greater than V_{EN}
- The VBP voltage (at VBP pin) must be greater than $VBP_{(on)}$
- The UVLO pin must be greater than V_{UVLO}

In order for the device to turn OFF, any one of the following conditions must be met:

- The ENABLE pin voltage must be less than V_{DIS}
- The VBP voltage (at VBP pin) must be less than $VBP_{(off)}$
- The UVLO pin must be less than V_{UVLO}

Feature Description (continued)

Programming the input UVLO can be accomplished using the UVLO pin. A resistor divider from the input voltage (VIN pin) to GND sets the UVLO level. Once the input voltage reaches a value that meets the V_{UVLO} level at the UVLO pin, then a small hysteresis current, I_{UVLO} at the UVLO pin is switched in. The programmable UVLO function is shown in Figure 17.

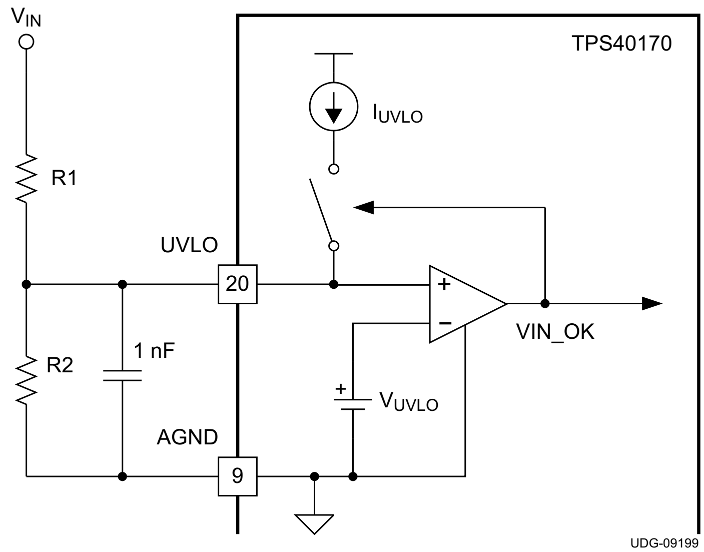


Figure 17. UVLO Functional Block Schematic

7.3.2.1 Equations for Programming the Input UVLO:

Components R1 and R2 represent external resistors for programming UVLO and hysteresis and can be calculated in Equation 1 and Equation 2 respectively.

$$R_1 = \frac{V_{ON} - V_{OFF}}{I_{UVLO}} \tag{1}$$

$$R_2 = R_1 \times \frac{V_{UVLO}}{\left(V_{ON} - V_{UVLO}\right)}$$

where

- V_{ON} is the desired turn-on voltage of the converter
- V_{OFF} is the desired turn-off voltage for the converter
- I_{UVLO} is the hysteresis current generated by the device, 5.0 µA (typ)
- V_{UVLO} is the UVLO pin threshold voltage, 0.9 V (typ) (2)

NOTE

If the UVLO pin is connected to a voltage greater than 0.9 V, the programmable UVLO is disabled and the device defaults to an internal UVLO ($VBP_{(on)}$ and $VBP_{(off)}$). For example, the UVLO pin can be connected to VDD or the VBP pin to disable the programmable UVLO function.

A 1 nF ceramic by-pass capacitor must be connected between the UVLO pin and GND.

7.3.3 Oscillator and Voltage Feed-Forward

TPS40170 implements an oscillator with input-voltage feed-forward compensation that enables instant response to input voltage changes. Figure 18 shows the oscillator timing diagram for the TPS40170. The resistor from the RT pin to GND sets the free running oscillator frequency. The voltage V_{RT} on the RT pin is made proportional to the input voltage (see Equation 3).

Feature Description (continued)

$$V_{RT} = \frac{V_{IN}}{K_{PWM}}$$

where

- $K_{PWM} = 15$ (3)

The resistor at the RT pin sets the current in the RT pin. The proportional current charges an internal 100-pF oscillator capacitor. The ramp voltage on this capacitor is compared with the RT pin voltage, V_{RT}. Once the ramp voltage reaches V_{RT}, the oscillator capacitor is discharged. The ramp that is generated by the oscillator (which is proportional to the input voltage) acts as voltage feed-forward ramp to be used in the PWM comparator.

The time between the start of the discharging oscillator capacitor and the start of the next charging cycle is fixed at 170 ns (typical). During the fixed discharge time, the PWM output is maintained as OFF. This is the minimum OFF-time of the PWM output.

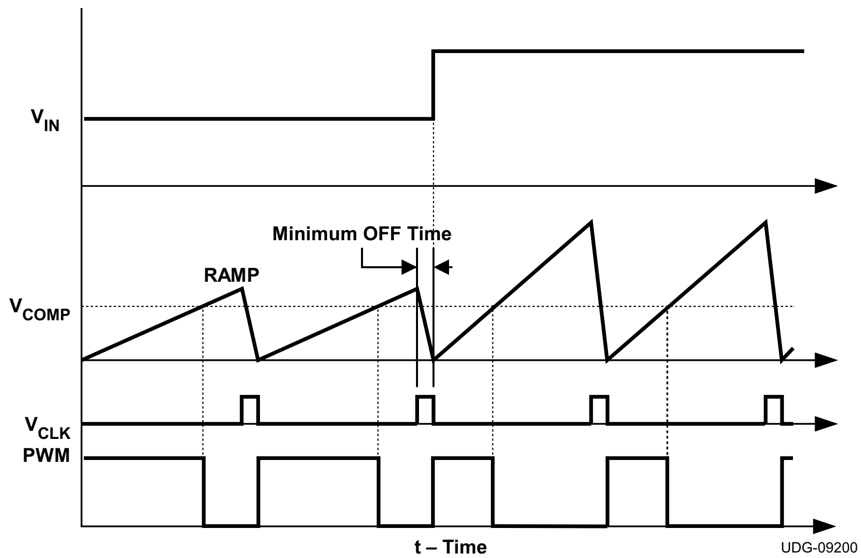


Figure 18. Feed-Forward Oscillator Timing Diagram

7.3.3.1 *Calculating the Timing Resistance (R_{RT})*

$$R_{RT} = \left(\frac{10^4}{f_{SW}}\right) - 2(k\Omega)$$

where

- f_{SW} is the switching frequency in kHz
- R_{RT} is the resistor connected from RT pin to GND in kΩ (4)

NOTE

The switching frequency can be adjusted between 100 kHz and 600 kHz. The maximum switching frequency before skipping pulses is determined by the input voltage, output voltage, FET resistances, DCR of the inductor, and the minimum on time of the TPS40170. Use Equation 5 to determine the maximum switching frequency. For further details, please see application note SLYT293.

$$f_{SW(max)} = \frac{V_{OUT(min)} + \left(I_{OUT(min)} \times \left(R_{DS2} + R_{LOAD}\right)\right)}{t_{ON(min)} \times \left(V_{IN(max)} - I_{OUT(min)} \times \left(R_{DS1} - R_{DS2}\right)\right)}$$

Feature Description (continued)

where

- $f_{SW(max)}$ is the maximum switching frequency
- $V_{OUT(min)}$ is the minimum output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(min)}$ is the minimum output current
- R_{DS1} is the high-side FET resistance
- R_{DS2} is the low-side FET resistance
- and R_{LOAD} is the inductor series resistance (5)

7.3.4 Overcurrent Protection and Short-Circuit Protection (OCP and SCP)

The TPS40170 has the capability to set a two-level overcurrent protection. The first level of overcurrent protection (OCP) is the normal overload setting based on low-side MOSFET voltage sensing. The second level of protection is the heavy overload setting such as short-circuit based on the high-side MOSFET voltage sensing. This protection takes effect immediately. The second level is termed short-circuit protection (SCP).

The OCP level is set by the ILIM pin voltage. A current (I_{ILIM}) is sourced into the ILIM pin from which a resistor R_{ILIM} is connected to GND. Resistor R_{ILIM} sets the first level of overcurrent limit. The OCP is based on the low-side FET voltage at the switch-node (SW pin) when the LDRV is ON after a blanking time, which is the product of inductor current and low-side FET turn-on resistance $R_{DS(on)}$. The voltage is inverted and compared to ILIM pin voltage. If it is greater than the ILIM pin voltage, then a 3-bit counter inside the device increments the fault-count by 1 at the start of the next switching cycle. Alternatively, if it is less than the ILIM pin voltage, then the counter inside the device decrements the fault-count by 1. When the fault-count reaches 7, an overcurrent fault (OC_FAULT) is declared and both the HDRV and LDRV are turned OFF. The resistor R_{ILIM} can be calculated by the following Equation 6.

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)}}{I_{ILIM}} = \frac{I_{OC} \times R_{DS(on)}}{9.0\,\mu A} \tag{6}$$

The SCP level is set by a multiple of the ILIM pin voltage. The multiplier has three discrete values, 3, 7 or 15 times, which can be selected by respectively choosing a 10-kΩ, open circuit, or 20 kΩ resistor from LDRV pin to GND. This multiplier AOC information is translated during the t_{CAL} time, which starts after the enable and UVLO conditions are met.

The SCP is based on sensing the high-side FET voltage drop from V_{VIN} to V_{SW} when the HDRV is ON after a blanking time, which is product of inductor current and high-side FET turn-on resistance $R_{DS(on)}$. The voltage is compared to the product of multiplier and the ILIM pin voltage. If it exceeds the product, then the fault-count is immediately set to 7 and the OC_FAULT is declared. The HDRV is terminated immediately without waiting for the duty cycle to end. When an OC_FAULT is declared, both the HDRV and LDRV are turned OFF. The appropriate multiplier (A), can be selected using Equation 7.

$$A = \frac{I_{SC} \times R_{DS(on)HS}}{I_{OC} \times R_{DS(on)LS}} \tag{7}$$

Figure 19 shows the functional block of the two-level overcurrent protection.

Feature Description (continued)

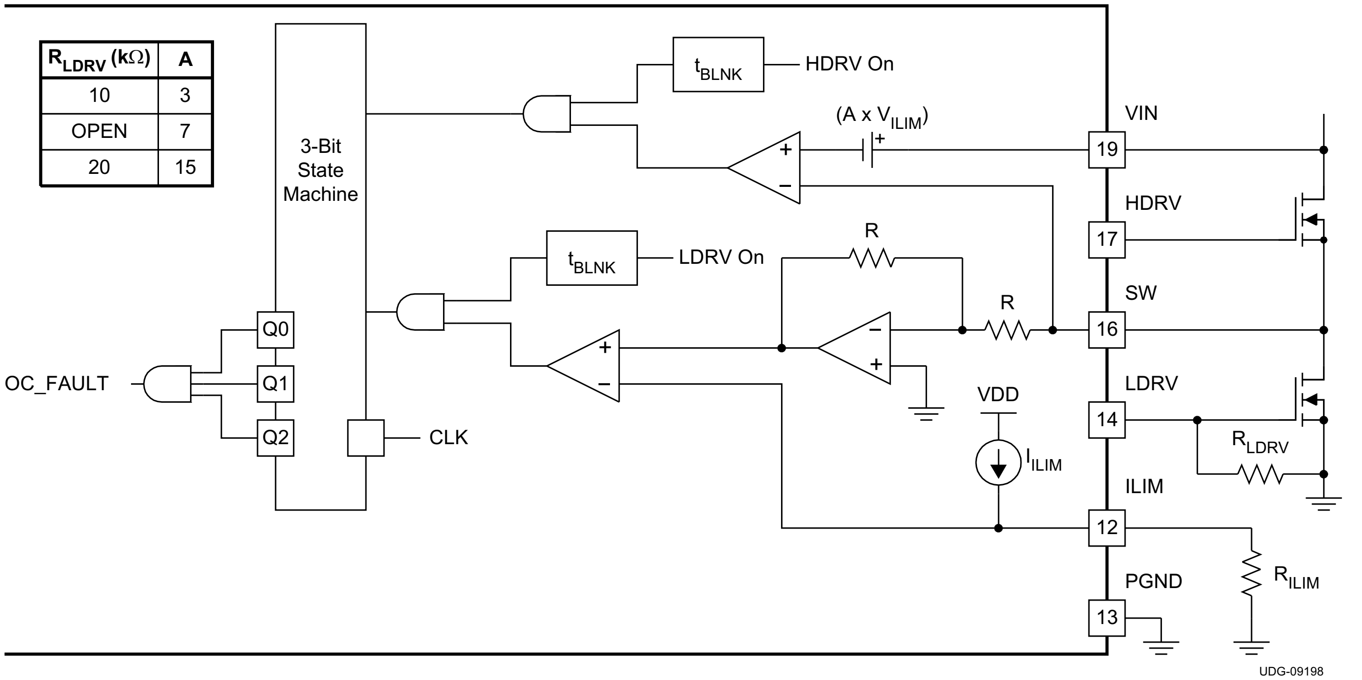


Figure 19. OCP and SCP Protection Functional Block Diagram

NOTE

Both OCP and SCP are based on low-side and high-side MOSFET voltage sensing at the SW node. Excessive ringing on the SW node can have negative impact on the accuracy of OCP and SCP. Adding an RC snubber from the SW node to GND helps minimize the potential impact.

7.3.5 Soft-Start and Fault-Logic

A capacitor from the SS pin to GND defines the SS time, t_{SS}. The TPS40170 enters into soft-start immediately after completion of the overcurrent calibration. The SS pin goes through the device's internal level-shifter circuit before reaching one of the positive inputs of the error amplifier. The SS pin must reach approximately 0.65 V before the input to the error amplifier begins to rise above 0 V. To charge the SS pin from 0 V to 0.65 V faster, at the beginning of the soft-start in addition to the normal charging current, (11.6 µA, typ.), an extra charging current (40.4 µA, typ.) is switched-in to the SS pin. As the SS capacitor reaches 0.5 V, the extra charging current is turned off and only the normal charging current remains. Figure 20 shows the soft-start function block.

Feature Description (continued)

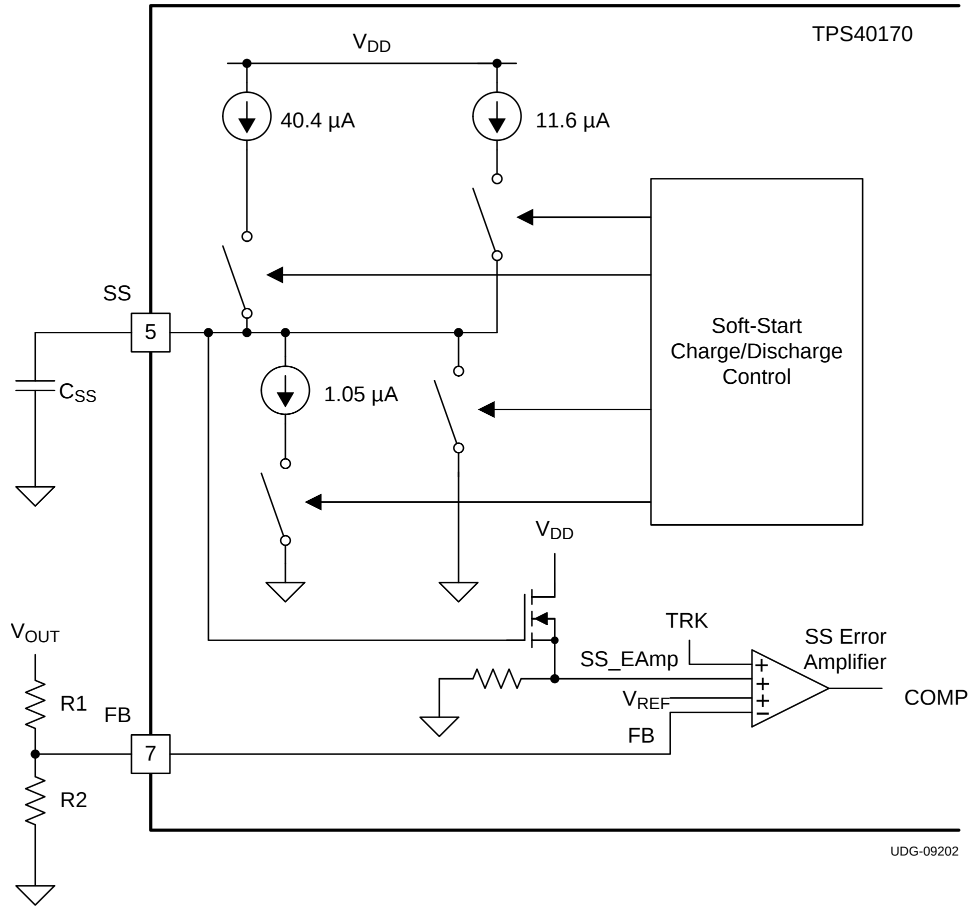


Figure 20. Soft-Start Schematic Block

As the SS pin voltage approaches 0.65 V, the positive input to the error amplifier begins to rise (see Figure 21). The output of the error amplifier (the COMP pin) starts rising. The rate of rise of the COMP voltage is mainly limited by the feedback loop compensation network. Once V_{COMP} reaches the valley of the PWM ramp, the switching begins. The output is regulated to the error amplifier input through the FB pin in the feedback loop. Once the FB pin reaches the 600 mV reference voltage, the feedback node is regulated to the reference voltage, V_{REF}. The SS pin continues to rise and is clamped to VDD.

The SS pin is discharged through an internal switch during the following conditions:

- Input (VIN) undervoltage lock out UVLO pin less than V_{UVLO}
- Overcurrent protection calibration time (t_{CAL})
- VBP less than threshold voltage ($VBP_{(off)}$)

Because it is discharged through an internal switch, the discharging time is relatively fast compared with the discharging time during the fault restart which is discussed in the *Soft-Start During Overcurrent Fault* section.

Feature Description (continued)

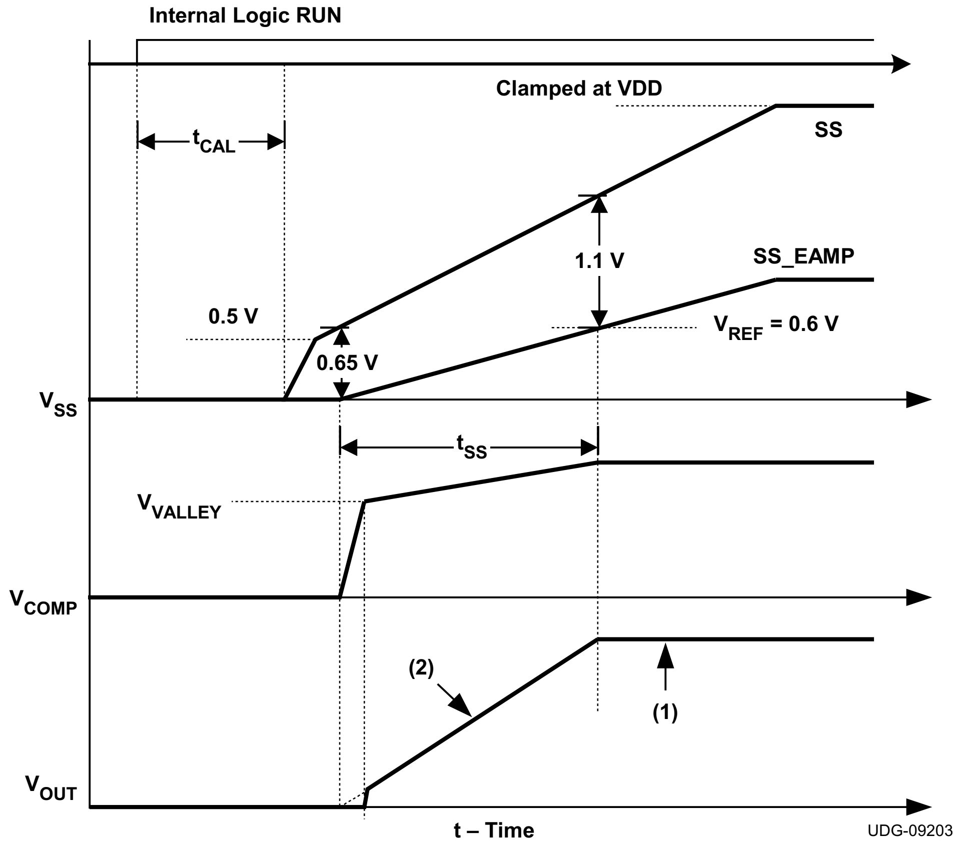


Figure 21. Soft-Start Waveforms

NOTE

Referring to Figure 21

- (1) VREF dominates the positive input of the error amplifier
- (2) SS_EAMP dominates the positive input of the error amplifier

For $0 < V_{SS\_EAMP} < V_{REF}$

$$V_{OUT} = V_{SS(EAMP)} \times \frac{(R1 + R2)}{R2} \quad (8)$$

For $V_{SS\_EAMP} > V_{REF}$

$$V_{OUT} = V_{REF} \times \frac{(R1 + R2)}{R2} \quad (9)$$

7.3.5.1 Soft-Start During Overcurrent Fault

The soft-start block also has a role to controls the fault-logic timing. If an overcurrent fault (OC_FAULT) is declared, the soft-start capacitor is discharged internally through the device by a small current $I_{SS(sink)}$ (1.05 µA, typ.). Once the SS pin capacitor is discharged to below $V_{SS(flt,low)}$ (300 mV, typ.), the soft-start capacitor begins charging again. If the fault is persistent, a fault is declared which is determined by the overcurrent protection state machine. If the soft-start capacitor is below $V_{SS(flt,high)}$ (2.5 V, typ.), then the soft-start capacitor continues to charge until it reaches $V_{SS(flt,high)}$ before a discharge cycle is initiated. This ensures that the re-start time-interval is always constant. Figure 22 shows the restart timing.

Feature Description (continued)

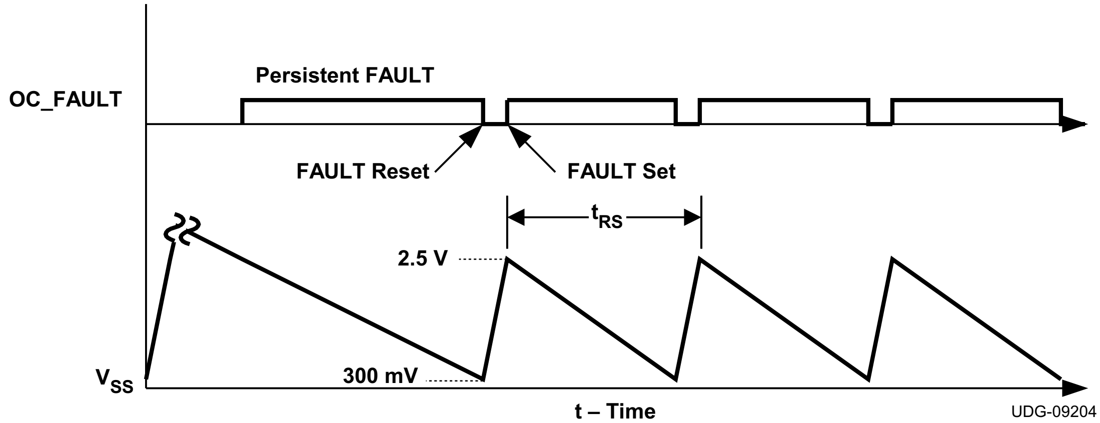


Figure 22. Overcurrent Fault Restart Timing

NOTE

For the feedback to be regulated to the SS_EAMP voltage, the TRK pin must be pulled up high directly or through a resistor to VDD.

7.3.5.2 Equations for Soft-Start and Restart Time

The soft-start time (t_{SS}) is defined as the time taken for the internal SS_EAMP node to go from 0 V to the 0.6 V, V_{REF} voltage. The SS_EAMP starts rising as the SS pin goes beyond 0.65 V. The offset voltage between the SS and the SS_EAMP starts increasing as the SS pin voltage starts rising. Figure 21, shows that the SS time can be defined as the time taken for the SS pin voltage to change by 1.05 V (see Equation 10).

The restart time (t_{RS}) is defined in Equation 11 as the time taken for the soft-start capacitor (C_{SS}) to discharge from 2.5 V to 0.3 V and to then recharge up to 2.5 V.

$$C_{SS} = \frac{t_{SS}}{0.09} \quad (10)$$

$$t_{RS} \approx 2.28 \times C_{SS}$$

where

- C_{SS} is the soft-start capacitance in nF
- t_{SS} is the soft-start time in ms
- t_{RS} is the re-start time in ms (11)

NOTE

During soft-start (V_{SS} < 2.5 V), the overcurrent protection limit is 1.5 times normal overcurrent protection limit. This allows higher output capacitance to fully charge without activating overcurrent protection.

7.3.6 Over-Temperature Fault

Figure 23 shows the over-temperature protection scheme. If the junction temperature of the device reaches the thermal shutdown limit of $t_{SD(set)}$ (165°C, typ) and SS charging is completed, an over-temperature FAULT is declared. The soft-start capacitor begins to be discharged. During soft-start discharging period, the PWM switching is terminated; therefore both HDRV and LDRV are driven low, turning off both MOSFETs.

Feature Description (continued)

The soft-start capacitor begins to charge and over-temperature fault is reset whenever the soft-start capacitor is discharged below $V_{SS(flt,low)}$ (300 mV, typ.). During each restart cycle, PWM switching is turned on. When SS is fully charged, PWM switching is terminated. These restarts repeat until the temperature of the device has fallen below the thermal reset level, $t_{SD(reset)}$ (135°C typ). PWM switching continues and system returns to normal regulation.

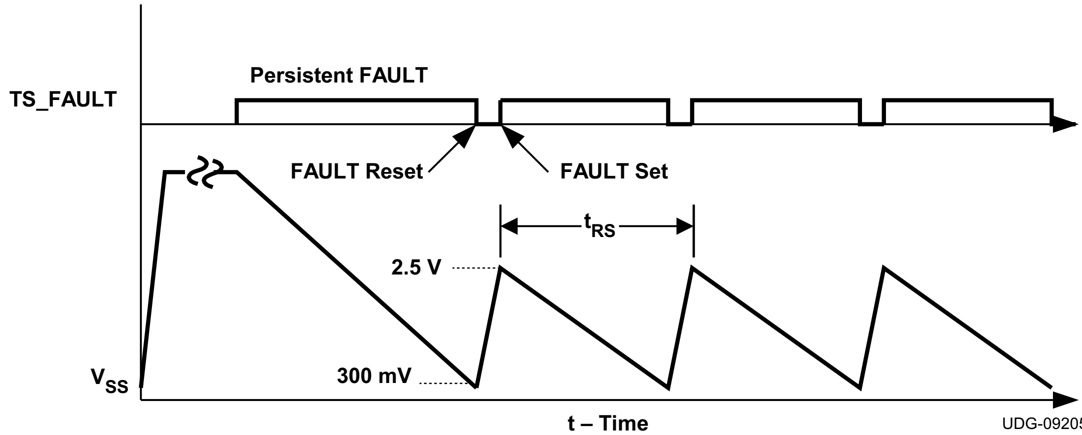


Figure 23. Over-Temperature Fault Restart Timing

The soft-start timing during over-temperature fault is the same as the soft-start timing during overcurrent fault. See the *Equations for Soft-Start and Restart Time* section.

7.3.7 Tracking

The TRK pin is used for output voltage tracking. The output voltage is regulated so that the FB pin equals the lowest of the internal reference voltage (V_{REF}) or the level-shifted SS pin voltage (SS_{EAMP}) or the TRK pin voltage. Once the TRK pin goes above the reference voltage, then the output voltage is no longer governed by the TRK pin, but it is governed by the reference voltage.

If the voltage tracking function is used, then it should be noted that the SS pin capacitor must remain connected as the SS pin and is also used for FAULT timing. For proper tracking using the TRK pin, the tracking voltage should be allowed to rise only after SS_{EAMP} has exceeded V_{REF}, so that there is no possibility of the TRK pin voltage being higher than the SS_{EAMP} voltage. From Figure 21, for SS_{EAMP} = 0.6 V, the SS pin voltage is typically 1.7 V.

The maximum slew rate on the TRK pin should be determined by the output capacitance and feedback loop bandwidth. A higher slew rate can possibly trip overcurrent protection.

Figure 24 shows the tracking functional block. For SS_{EAMP} voltages greater than TRK pin voltage, the V_{OUT} is given by Equation 12 and Equation 13.

Feature Description (continued)

For 0 V < V_{TRK} < V_{REF}

$$V_{OUT} = V_{TRK} \times \frac{(R1 + R2)}{R2} \quad (12)$$

For V_{TRK} > V_{REF}

$$V_{OUT} = V_{REF} \times \frac{(R1 + R2)}{R2} \quad (13)$$

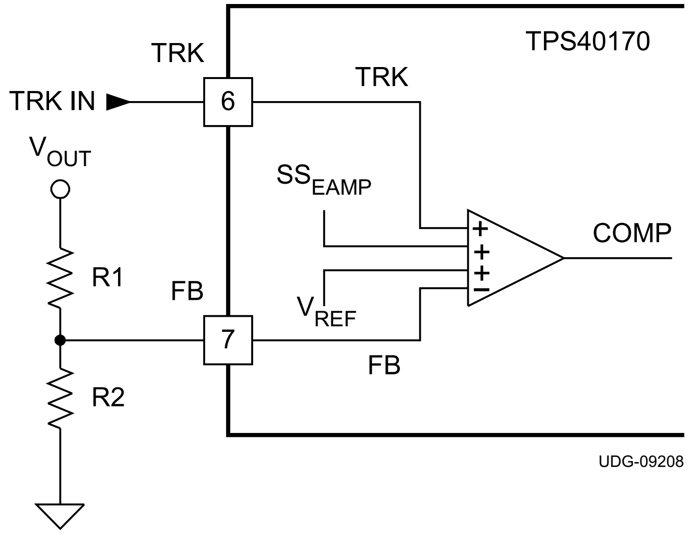


Figure 24. Tracking Functional Block

There are three potential applications for the tracking function.

- simultaneous voltage tracking
- ratiometric voltage tracking
- sequential startup mode

The tracking function configurations and waveforms are shown in Figure 25, Figure 27, and Figure 29 respectively.

In simultaneous voltage tracking shown in Figure 25, tracking signals, V_{TRK1} and V_{TRK2}, of two modules, POL1 and POL2, start up at the same time and their output voltages V_{OUT1} initial and V_{OUT2} initial are approximately the same during initial startup. Since V_{TRK1} and V_{TRK2} are less than V_{REF} (0.6 V, typ), Equation 12 is used. As a result, components selection should meet Equation 14.

$$\left(\frac{(R_1 + R_2)}{R_1}\right) \times V_{TRK1} = \left(\frac{(R_3 + R_4)}{R_3}\right) \times V_{TRK2} \Rightarrow \frac{R_5}{R_6} = \left(\frac{\left(\frac{R_1}{(R_1 + R_2)}\right)}{\left(\frac{R_3}{(R_3 + R_4)}\right)} - 1\right) \quad (14)$$

After the lower output voltage setting reaches output voltage V_{OUT1} set point, where V_{TRK1} increases above V_{REF}, the output voltage of the other one (V_{OUT2}) continues increasing until it reaches its own set point, where V_{TRK2} increases above V_{REF}. At that time, Equation 13 is used. As a result, the resistor settings should meet Equation 15 and Equation 16.

$$V_{OUT1} = \left(\frac{(R_1 + R_2)}{R_1}\right) \times V_{REF} \quad (15)$$

$$V_{OUT2} = \left(\frac{(R_3 + R_4)}{R_3}\right) \times V_{REF} \quad (16)$$

Equation 14 can be simplified into Equation 17 by replacing with Equation 15 and Equation 16

$$\left(\frac{R_5}{R_6}\right) = \left(\left(\frac{V_{OUT2}}{V_{OUT1}}\right) - 1\right) \quad (17)$$

Feature Description (continued)

If 5 V = V_{OUT2} and 2.5 V = V_{OUT1} are required, according to Equation 15, Equation 16 and Equation 17, the selected components can be as following:

- $R_5 = R_6 = R_4 = R_2 = 10\ k\Omega$
- $R_1 = 3.16\ k\Omega$
- $R_3 = 1.37\ k\Omega$

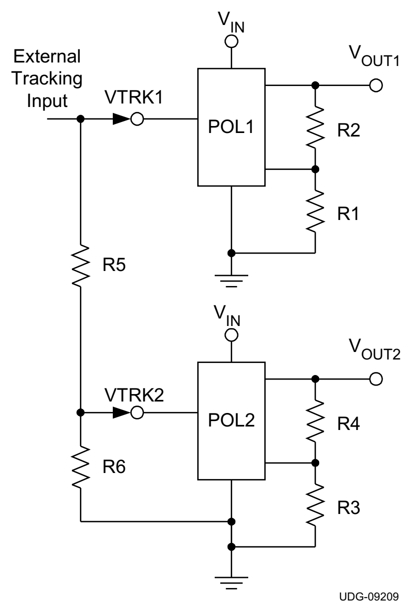


Figure 25. Simultaneous Voltage Tracking Schematic

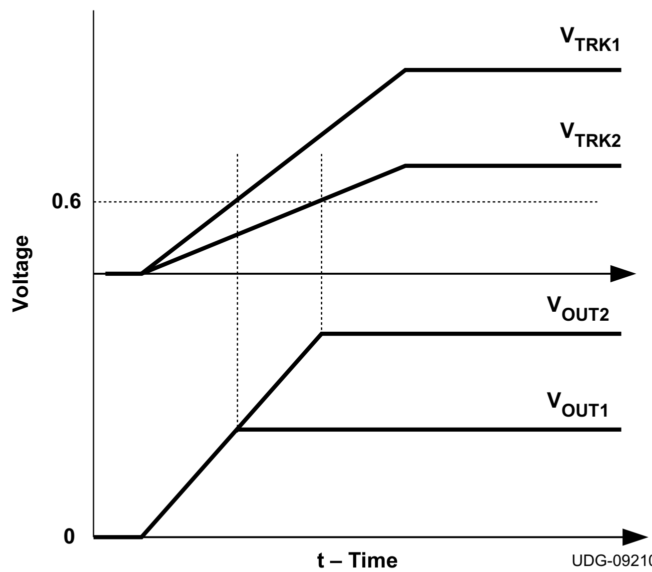


Figure 26. Simultaneous Voltage Tracking Waveform

Feature Description (continued)

In ratiometric voltage tracking shown in Figure 27, the two tracking voltages, V_{TRK1} and V_{TRK2}, for two modules, POL1 and POL2, are the same. Their output voltage, V_{OUT1} and V_{OUT2}, are different with different voltage divider R2/R1 and R4/R3. V_{OUT1} and V_{OUT2} increase proportionally and reach their output voltage set points at about the same time.

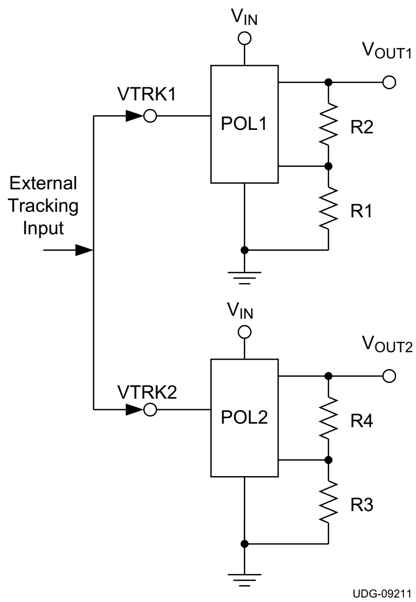


Figure 27. Ratiometric Voltage Tracking Schematic

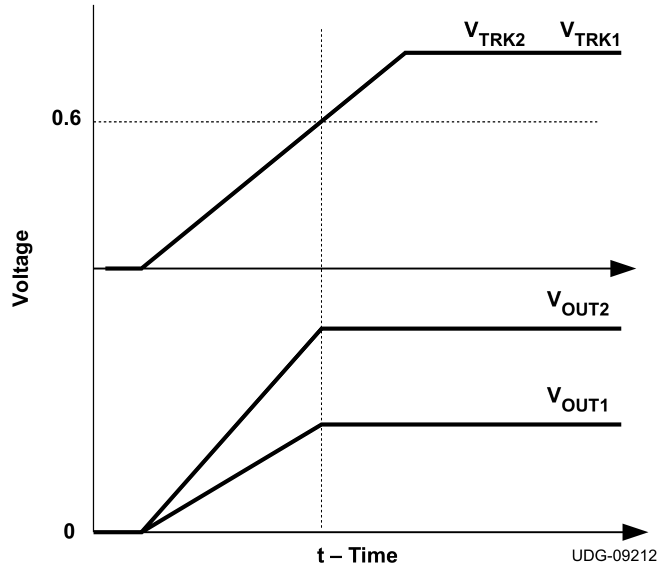


Figure 28. Ratiometric Voltage Tracking Waveform

Feature Description (continued)

Sequential startup is shown in Figure 29. During start-up of the first module, POL1, its PGOOD1 is pulled to low. Since PGOOD1 is connected to soft-start SS2 of the second module, POL2, is not able to charge its soft-start capacitor. After output voltage V_{OUT1} of POL1 reaches its setting point, PGOOD1 is released. POL2 starts charging its soft-start capacitor. Finally, output voltage V_{OUT2} of POL2 reaches its setting point.

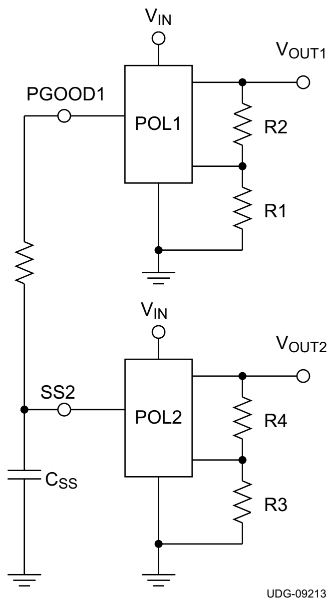


Figure 29. Sequential Start-Up Schematic

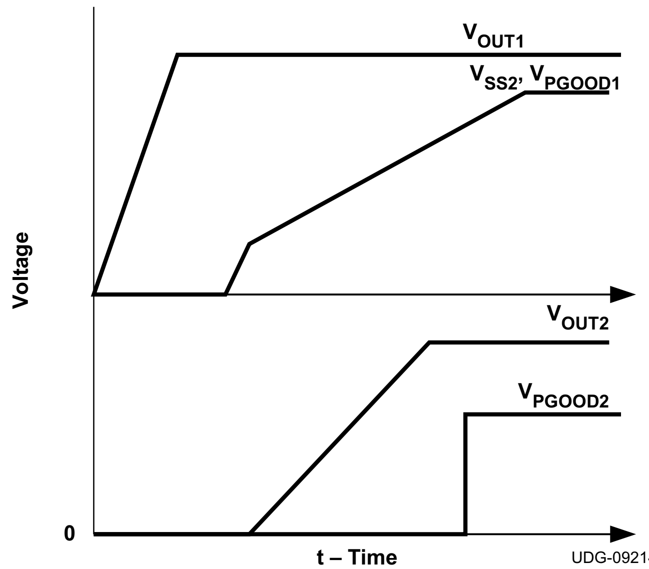


Figure 30. Sequential Start-Up Waveform

NOTE

The TRK pin has high impedance, so it is a noise sensitive terminal. If the tracking function is used, a small RC filter is recommended at the TRK pin to filter out high-frequency noise.

If the tracking function is not used, the TRK pin must be pulled up directly or through a resistor (with a value between 10 kΩ and 100 kΩ) to VDD.

7.3.8 Adaptive Drivers

The drivers for the external high-side and low-side MOSFETs are capable of driving a gate-to-source voltage, V_{BP}. The LDRV driver for the low-side MOSFET switches between VBP and PGND, while the HDRV driver for the high-side MOSFET is referenced to SW and switches between BOOT and SW. The drivers have non-overlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier.

7.3.9 Start-Up into Pre-Biased Output

The TPS40170 contains a circuit to prevent current from being pulled out of the output during startup in case the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [V_{FB}]), the controller slowly activates synchronous rectification by starting the first LDRV pulses with a narrow on-time (see Figure 31), where:

- V_{IN} = 5 V
- V_{OUT} = 3.3 V
- V_{PRE} = 1.4 V

Feature Description (continued)

- f_{SW} = 300 kHz
- L = 0.6 µH

It then increments the on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensures that the output voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased startup to normal mode operation with minimal disturbance to the output voltage. The time from the start of switching until the low-side MOSFET is turned on for the full (1-D) interval is between approximately 20 and 40 clock cycles.

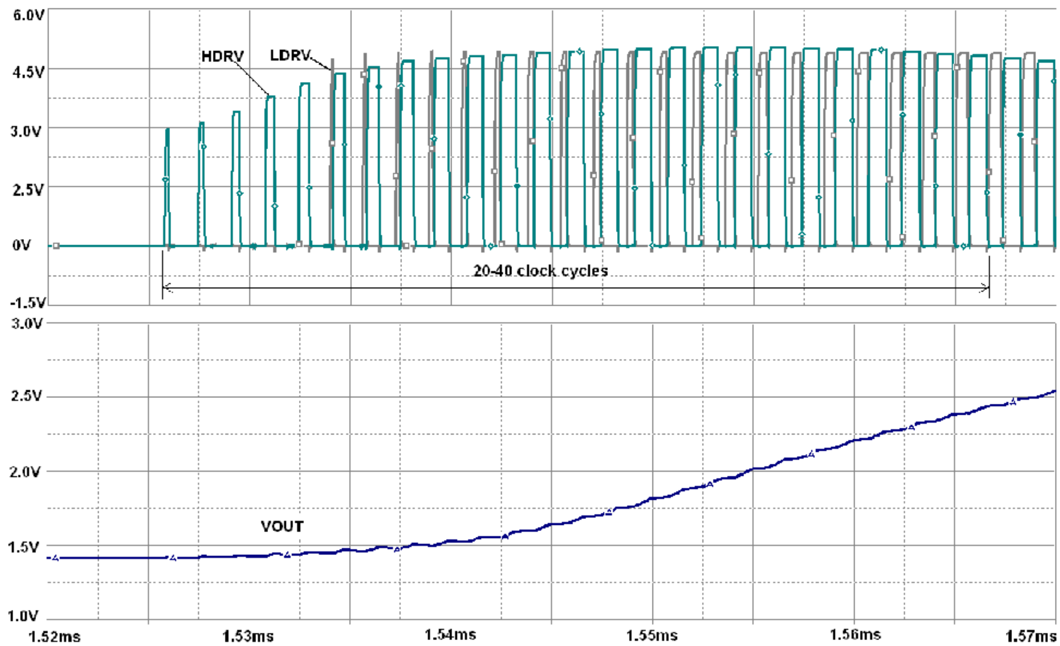


Figure 31. Start-Up Switching Waveform during Pre-Biased Condition

If the output is pre-biased to a voltage higher than the voltage commanded by the reference, then the PWM switching does not start.

NOTE

When output is pre-biased at $V_{PRE-BIAS}$, that voltage also applies to the SW node during start-up. When the pre-bias circuitry commands the first few high-side pulses before the first low-side pulse is initiated, the gate voltage for the high-side MOSFET is as described in Equation 18. Alternatively, If pre-bias level is high, it is possible that SCP can be tripped due to high turn-on resistance of the high-side MOSFET with low gate voltage. Once tripped, the device resets and then attempts to re-start. The device may not be able to start up until output is discharged to a lower voltage level by either an active load or through feedback resistors.

In the case of a high pre-bias level, a low gate-threshold voltage rated device is recommended for the high-side MOSFET and increasing the SCP level also helps alleviate the problem.

Feature Description (continued)

$$V_{GATE(hs)} = \left(V_{BP} - V_{DFWD} - V_{PRE-BIAS}\right)$$

where

- $V_{GATE(hs)}$ is the gate voltage for the high-side MOSFET
- V_{BP} is the BP regulator output
- V_{DFWD} is bootstrap diode forward voltage (18)

7.3.10 Powergood (PGOOD)

The TPS40170 provides an indication that the output voltage of the converter is within the specified limits of the regulation as measured at the FB pin. The PGOOD pin is an open-drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} is not within the PGOOD threshold limits.
- Soft-start is active, i.e., SS pin voltage is below $V_{SS,FLT,HIGH}$ limit.
- An undervoltage condition exists for the device.
- An overcurrent or short-circuit fault is detected.
- An over-temperature fault is detected.

Figure 32 shows a situation where no fault is detected during the startup, (the normal PGOOD situation). It shows that PGOOD goes high t_{PGD} (20 µs, typ.) after all the conditions (listed above) are met.

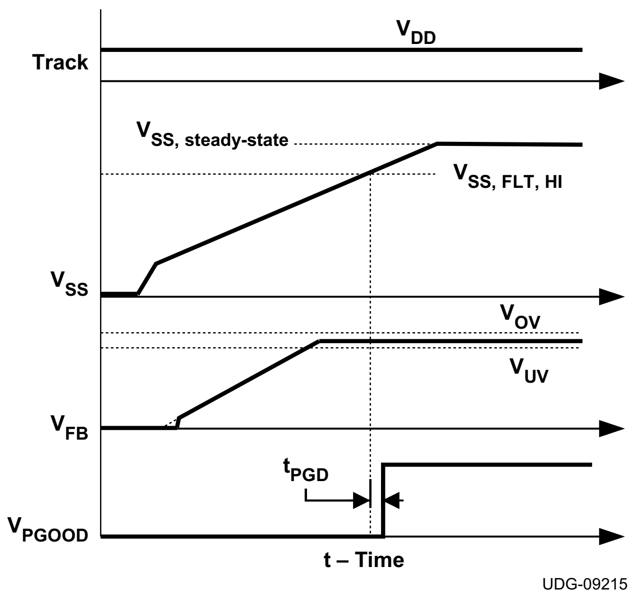


Figure 32. PGOOD Signal

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built-in resistor connected from drain to gate on the PGOOD pull-down device allows the PGOOD pin to operate like as a diode to GND.

7.3.11 PGND and AGND

TPS40170 provides separate signal ground (AGND) and power ground (PGND) pins. PGND is primarily used for gate driver ground return. AGND is an internal logic signal ground return. These two ground signals are internally loosely connected by two anti-parallel diodes. PGND and AGND must be electrically connected externally.

7.4 Device Functional Modes

7.4.1 Frequency Synchronization

The TPS40170 has three modes.

- **Master mode**: In this mode the master/slave selector pin, (M/S) is connected to VIN. The SYNC pin emits a stream of pulses at the same frequency as the PWM switching frequency. The pulse stream at the SYNC pin is at 50% duty cycle and the same amplitude as V_{VBP}. Also, the falling edge of the voltage on SYNC pin is synchronized with the rising edge of the HDRV.
- **Slave-180° mode**: In this mode the M/S pin is connected to GND. The SYNC pin of the TPS40170 accepts a synchronization clock signal, and the HDRV is synchronized with the rising edge of the incoming synchronization clock.
- **Slave-0° mode**: In this mode, the M/S pin is left open. The SYNC pin of the TPS40170 accepts a synchronization clock signal, and the HDRV is synchronized with the falling edge of the incoming synchronization clock.

The two slave modes can be synchronized to an external clock through the SYNC pin. They are shown in Figure 33. The synchronization frequency should be within ±30% of its programmed free running frequency.

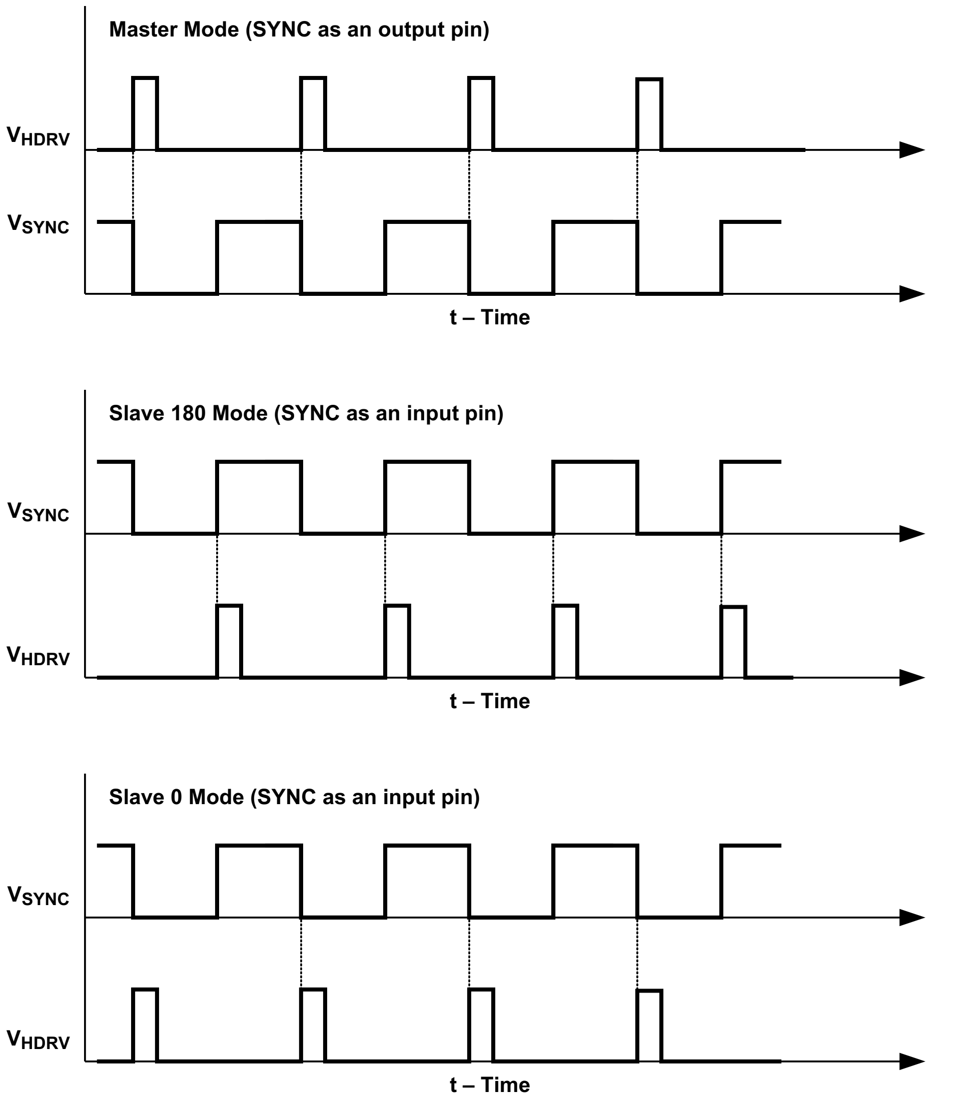


Figure 33. Frequency Synchronization Waveforms In Different Modes

Device Functional Modes (continued)

TPS40170 provides a smooth transition for the SYNC clock signal loss at slave mode. In slave mode, a synchronization clock signal is provided externally through the SYNC pin to the device. The switching frequency is synchronized to the external SYNC clock signal. If for some reason the external clock signal is missing, the device switching frequency is automatically overridden by a transition frequency which is 0.7 times its programmed free running frequency. This transition time is approximately 20 µs. After that, the device switching frequency is changed to its programmed free running frequency. Figure 34 shows this process.

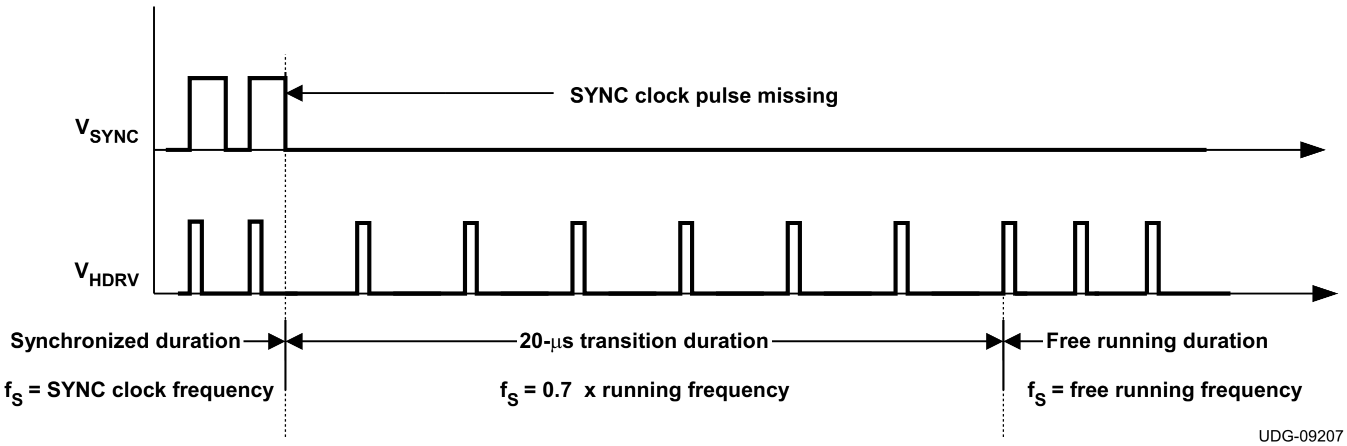


Figure 34. Transition for Sync Clock Signal Missing (For Slave-180 Mode)

NOTE

When the device is operating in the master mode with duty ratio around 50%, PWM jittering may occur. Always configure the device into the slave mode by either connecting the M/S pin to GND or leaving it floating if master mode is not used.

When an external SYNC clock signal is used for synchronization, limit maximum slew rate of the clock signal to 10 V/µs to avoid potential PWM jittering and connect the SYNC pin to the external clock signal via a 5-kΩ resistor.

7.4.2 Operation Near Minimum VIN (V_{VIN} ≤ 4.5 V)

The TPS40170 is designed to operate with input voltages above 4.5 V. With voltages below 4.5 V if the EN pin is above its 600 mV turn on threshold the VDD and VBP internal regulators are active. These regulators will operate in drop out and output the highest voltage possible for the given VIN. The EN pin voltage must be below 100 mV to disable the VDD and VBP regulators. Switching is disabled while the VBP output voltage is below the VBP turn-on voltage of 4.4 V maximum. When there is sufficient VIN voltage to regulate the VBP voltage above 4.4 V the final condition for switching to begin is the UVLO pin voltage must be above its 900 mV typical threshold. Once all three conditions are met the TPS40170 will begin switching and the soft-start sequence is initiated. The device starts at the soft-start time determined by the external capacitance at the SS/TR pin. If a design requires operation near the minimum VIN voltage, due to lower VBP voltage when operating in dropout, lower gate threshold MOSFETs are recommended

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The wide input TPS40170 controller can function in a very wide range of applications. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.1.1 Bootstrap Resistor

A small resistor in series with the bootstrap capacitor reduces the turn-on speed of the high-side MOSFET, thereby reducing the rising edge ringing of the SW node and reduces short through induced by dv/dt. A bootstrap resistor value that is too large delays the turn-on time of the high-side switch and may trigger an apparent SCP fault.

8.1.2 SW Node Snubber Capacitor

Observable voltage ringing at the SW node is caused by fast switching edges and parasitic inductance and capacitance. If the ringing results in excessive voltage on the SW node, or erratic operation of the converter, an RC snubber may be used to dampen the ringing and ensure proper operation over the full load range. See design example.

8.1.3 Input Resistor

The TPS40170 has a wide input voltage range which allows for the device input to share power source with power stage input. Power stage switching noise may pollute the device power source if the layout is not adequate in minimizing noise. It may trigger short-circuit fault. If so, adding a small resistor between the device input and power stage input is recommended. This resistor composites an RC filter with the device input capacitor and filter out the switching noise from power stage. See R1 in the design example.

8.1.4 LDRV Gate Capacitor

Power device selection is important for proper switching operation. If the low-side MOSFET has low gate capacitance C_{GS} (if C_{GS}<C_{GD}), there is a risk of short-through induced by high dv/dt at switching node (See reference[1]) during high-side turned-on. If this happens, add a small capacitance between LDRV and GND. See design example.

8.2 Typical Application

This example describes the design process for a very wide input (10 V to 60 V) to a regulated 5 V output at a load current of 6 A. The schematic shown in Figure 35 is configured for the design parameters provided in Table 1. Alternatively the WEBENCH software can be used to generate a complete design with the TPS40170.

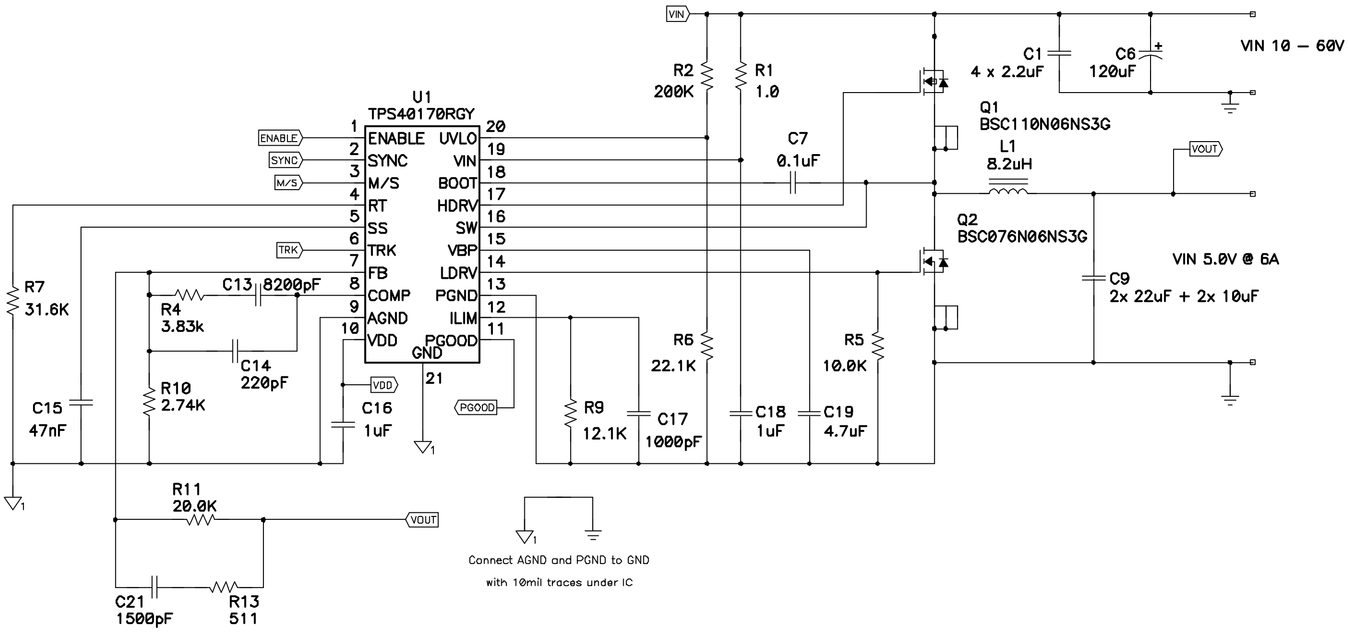


Figure 35. Typical Design Application

8.2.1 Design Requirements

Table 1. Design Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		10		60	
$V_{IN(ripple)}$	Input ripple	I_{OUT} = 6 A			0.5	V
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 20 A	4.8	5.0	5.2	
	Line regulation	10 V ≤ V_{IN} ≤ 60 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 6 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT} = 6 A			100	
V_{OVER}	Output overshoot	ΔI_{OUT} = 2.5 A		250		mV
V_{UNDER}	Output undershoot	ΔI_{OUT} = -2.5 A		250		
I_{OUT}	Output current	10 V ≤ V_{IN} ≤ 60 V	0		6	A
t_{SS}	Soft-start time	V_{IN} = 24 V		4		ms
I_{SCP}	Short circuit current trip point		8			A
η	Efficiency	V_{IN} = 24 V, I_{OUT} = 6 A		94%		
f_{SW}	Switching frequency			300		kHz
	Size				1.5	in^2

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance,
   – Run thermal simulations to understand the thermal performance of your board,
   – Export your customized schematic and layout into popular CAD formats,
   – Print PDF reports for the design, and share your design with colleagues.

8.2.2.2 List of Materials

Table 2. Design Example List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUF
C1	4	2.2 µF	Capacitor, Ceramic, 100 V, X7R, 15%	1210	Std	Std
C6	1	120 µF	Capacitor, Aluminum, 63 V, 20%, KZE Series	0.315"	KZE63VB121M10X16LL	Chemi-con
C7	1	0.1 µF	Capacitor, Ceramic, 50 V, X7R, 15%	603	Std	Std
C9	2 ea	22 µF 10 µF	Capacitor, Ceramic, 16 V, X7R, 15%	1210	Std	Std
C13	1	8200 pF	Capacitor, Ceramic, 50 V, X7R, 15%	603	Std	Std
C14	1	220 pF	Capacitor, Ceramic, 50 V, X7R, 15%	603	Std	Std
C15	1	47 nF	Capacitor, Ceramic, 50 V, X7R, 15%	603	Std	Std
C16	1	1 µF	Capacitor, 1 6V, X7R, 15%	603	Std	Std
C17	1	1000 pF	Capacitor, Ceramic, 50 V, X7R, 15%	603	Std	Std
C18	1	1 µF	Capacitor, Ceramic, 100 V, X7R, 15%	1206	Std	Std
C19	1	4.7 µF	Capacitor, Ceramic, 16 V, X5R, 15%	805	Std	Std
C21	1	1500 pF	Capacitor, Ceramic, 50 V, X7R, 15%	603	Std	Std
L1	1	8.2 µH	Inductor, SMT, 10 A, 16 mΩ	0.51"2	IHLP5050FDER8R2M01	Vishay
Q1	1		MOSFET, N-channel, 60 V, 50 A, 11 mΩ		BSC110N06NS3G	Infineon
Q2	1		MOSFET, N-channel, 60 V, 50 A, 7.6 mΩ		BSC076N06NS3G	Infineon
R10	1	2.74 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R4	1	3.83 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R5	1	10.0 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R9	1	12.1 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R11	1	20.0 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R6	1	22.1 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R7	1	31.6 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R2	1	200 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
R13	1	511 kΩ	Resistor, Chip, 1/16W, 1%	603	Std	R603
U1			IC, 4.5 V - 60 V wide input sync. PWM buck controller		TPS40170RGY	Texas Instruments

8.2.2.3 Select a Switching Frequency

To maintain acceptable efficiency and meet minimum on-time requirements, a 300 kHz switching frequency is selected.

8.2.2.4 Inductor Selection (L1)

Synchronous buck power inductors are typically sized for approximately 20-40% peak-to-peak ripple current (I_{RIPPLE}) Given this target ripple current, the required inductor size can be calculated in Equation 19.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{60\,V - 5\,V}{0.3 \times 6\,A} \times \frac{5\,V}{60\,V} \times \frac{1}{300\,kHz} = 8.5\,\mu H \tag{19}$$

Selecting a standard 8.2 µH inductor value, solving for I_{RIPPLE} = 1.86 A.

The RMS current through the inductor is approximated by Equation 20.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \tfrac{1}{12} \times \left(I_{RIPPLE}\right)^2} = \sqrt{\left(I_{OUT}\right)^2 + \tfrac{1}{12} \times \left(I_{RIPPLE}\right)^2} = \sqrt{(6)^2 + \tfrac{1}{12} \times (1.86)^2} = 6.02\,A \tag{20}$$

8.2.2.5 Output Capacitor Selection (C9)

The selection of the output capacitor is typically driven by the output transient response. The Equation 21 and Equation 22 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance:

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{\left(I_{TRAN}\right)^2 \times L}{V_{OUT} \times C_{OUT}} \tag{21}$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{\left(V_{IN} - V_{OUT}\right)} = \frac{\left(I_{TRAN}\right)^2 \times L}{\left(V_{IN} - V_{OUT}\right) \times C_{OUT}} \tag{22}$$

If $V_{IN(min)}$ > 2 x V_{OUT}, use overshoot to calculate minimum output capacitance. If $V_{IN(min)}$ < 2 x V_{OUT}, use undershoot to calculate minimum output capacitance.

$$C_{OUT(min)} = \frac{\left(I_{TRAN(max)}\right)^2 \times L}{V_{OUT} \times V_{OVER}} = \frac{(3)^2 \times 8.2\,\mu H}{5 \times 250\,mV} = 59\,\mu F \tag{23}$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated Equation 24.

$$ESR_{MAX} = \frac{V_{RIPPLE(tot)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(tot)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{100\,mV - \left(\frac{1.86\,A}{8 \times 59\,\mu F \times 300\,kHz}\right)}{1.86\,A} = 47\,m\Omega \tag{24}$$

Two 1210, 22 µF, 16 V X7R ceramic capacitors plus two 0805 10 µF, 16 V X7R ceramic capacitors are selected to provide more than 59 µF of minimum capacitance (including tolerance and DC bias derating) and less than 47 mΩ of ESR (parallel ESR of approximately 4 mΩ).

8.2.2.6 Peak Current Rating of Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated in Equation 25.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{5\,V \times \left(2 \times 22\,\mu F + 2 \times 10\,\mu F\right)}{4\,ms} = 0.08\,A \tag{25}$$

$$I_{L(peak)} = I_{OUT(max)} + \left(\tfrac{1}{2} \times I_{RIPPLE}\right) + I_{CHARGE} = 6\,A + \tfrac{1}{2} \times 1.86\,A + 0.08\,A = 7.01\,A \tag{26}$$

An IHLP5050FDER8R2M01 8.2 µH is selected. This 10-A, 16-mΩ inductor exceeds the minimum inductor ratings in a 13 mm × 13 mm package.

8.2.2.7 Input Capacitor Selection (C1, C6)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 400 mV and $V_{RIPPLE(ESR)}$ = 100 mV. The minimum capacitance and maximum ESR are estimated by:

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN} \times f_{SW}} = \frac{6\,A \times 5\,V}{400\,mV \times 10\,V \times 300\,kHz} = 25\,\mu F \tag{27}$$

$$ESR_{MAX} = \frac{V_{RIPPLE(esr)}}{I_{LOAD} + \frac{1}{2} \times I_{RIPPLE}} = \frac{100\,mV}{6.93A} = 14.4\,m\Omega \tag{28}$$

The RMS current in the input capacitors is estimated in Equation 29.

$$I_{RMS(cin)} = I_{LOAD} \times \sqrt{D \times (1-D)} = 6\,A \times \sqrt{0.5 \times (1-0.5)} = 3.0\,A \tag{29}$$

To achieve these values, four 1210, 2.2 µF, 100 V, X7R ceramic capacitors plus a 120 µF electrolytic capacitor are combined at the input. This provides a smaller size and overall cost than 10 ceramic input capacitors or an electrolytic capacitor with the ESR required.

Table 3. Inductor Summary

PARAMETER		VALUE	UNIT
L	Inductance	8.2	µH
$I_{L(rms)}$	RMS current (thermal rating)	6.02	A
$I_{L(peak)}$	Peak current (saturation rating)	7.01	A

8.2.2.8 MOSFET Switch Selection (Q1, Q2)

Using the J/K method for MOSFET optimization, apply Equation 30 through Equation 33.

High-side gate (Q1):

$$J = (10)^{-9} \times \left(\frac{V_{IN} \times I_{OUT}}{I_{DRIVE}} + \frac{Q_G}{Q_{SW}} \times V_{DRIVE} \right) \times f_{SW} \quad \left(W/_{nC} \right) \tag{30}$$

$$K = (10)^{-3} \left((I_{OUT})^2 + \frac{1}{12} \times (I_{P-P})^2 \right) \times \left(\frac{V_{OUT}}{V_{IN}} \right) \quad \left(W/_{m\Omega} \right) \tag{31}$$

Low-side gate (Q2):

$$K = (10)^{-3} \left((I_{OUT})^2 + \frac{1}{12} \times (I_{P-P})^2 \right) \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad \left(W/_{m\Omega} \right) \tag{32}$$

$$J = 10^{-9} \left(\frac{V_{FD} \times I_{OUT}}{I_{DRIVE}} + \frac{Q_G}{Q_{SW}} \times V_{DRIVE} \right) \times f_{SW} \quad \left(W/_{nC} \right) \tag{33}$$

Optimizing for 300 kHz, 24 V input, 5 V output at 6 A, calculate ratios of 5.9 mΩ/nC and 0.5 mΩ/nC for the high-side and low-side FETS respectively. BSC110N06NS2 (Ratio 1.2) and BSC076N06NS3 (Ratio 0.69) MOSFETS are selected.

8.2.2.9 Timing Resistor (R7)

The switching frequency is programmed by the current through R_{RT} to GND. The R_{RT} value is calculated using Equation 34.

$$R_{RT} = \frac{(10)^4}{f_{SW}} - 2\,k\Omega = \frac{(10)^4}{300\,kHz} - 2 = 31.3\,k\Omega \approx 31.6\,k\Omega \tag{34}$$

8.2.2.10 UVLO Programming Resistors (R2, R6)

The UVLO hysteresis level is programmed by R2 using Equation 35.

$$R_{UVLO(hys)} = \frac{V_{UVLO(on)} - V_{UVLO(off)}}{I_{UVLO}} = \frac{9\,V - 8\,V}{5.0\,\mu A} = 200\,k\Omega \quad (35)$$

$$R_{UVLO(set)} > R_{UVLO(hys)} \frac{V_{UVLO(max)}}{\left(V_{UVLO\_ON(min)} - V_{UVLO(max)}\right)} = 200\,k\Omega \frac{0.919\,V}{\left(9.0\,V - 0.919\,V\right)} = 22.7k\Omega \approx 22.1k\Omega \quad (36)$$

8.2.2.11 Boot-Strap Capacitor (C7)

A bootstrap capacitor with a value between 0.1 µF and 0.22 µF must be placed between the BOOT pin and the SW pin. It should be 10 times higher than MOSFET gate capacitance. To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to less than 250 mV.

$$C_{BOOST} = \frac{Q_{G1}}{V_{BOOT(ripple)}} = \frac{25\,nC}{250\,mV} = 100\,nF \quad (37)$$

8.2.2.12 VIN Bypass Capacitor (C18)

Place a capacitor with a value of 1.0 µF. Select a capacitor with a value from 0.1 µF to 1.0 µF, X5R or better ceramic bypass capacitor for VIN as specified in *Recommended Operating Conditions*. For this design a 1.0-µF, 100-V, X7R capacitor has been selected.

8.2.2.13 VBP Bypass Capacitor (C19)

Select a capacitor with a value from 1.0 µF to 10 µF, X5R or better ceramic bypass capacitor for VBP as specified in *Recommended Operating Conditions*. It should be at least 10 times higher than the bootstrap capacitance. For this design a 4.7-µF, 16-V capacitor has been selected.

8.2.2.14 VDD Bypass Capacitor (C16)

Select a capacitor with a value between 0.1 µF and 1 µF, X5R or better ceramic bypass capacitor for VDD as specified in *Recommended Operating Conditions*. For this design a 1-µF, 16-V capacitor has been selected.

8.2.2.15 SS Timing Capacitor (C15)

The soft-start capacitor provides smooth ramp of the error amplifier reference voltage for controlled start-up. The soft-start capacitor is selected by using Equation 38.

$$C_{SS} = \frac{t_{SS}}{0.09} = \frac{4\,ms}{0.09} = 44\,nF \approx 47\,nF \quad (38)$$

8.2.2.16 ILIM Resistor (R9, C17)

The TPS40170 use the negative drop across the low-side FET at the end of the "OFF" time to measure the inductor current. Allowing for 30% over the minimum current limit for transient recovery and 20% rise in $R_{DS(on)Q2}$ for self-heating of the MOSFET, the voltage drop across the low-side FET at current limit is given by Equation 39.

$$V_{OC} = \left(\left(1.3 \times I_{OCP(min)}\right) + \left(\tfrac{1}{2} \times I_{RIPPLE}\right)\right) \times 1.25 \times R_{DS(on)G2} = (1.3 \times 8\,A + \tfrac{1}{2} \times 1.86\,A) \times 1.25 \times 7.6\,m\Omega = 107.6\,mV \quad (39)$$

The internal current limit temperature coefficient helps compensate for the MOSFET $R_{DS(on)}$ temperature coefficient, so the current limit programming resistor is selected by Equation 40.

$$R_{ILIM} = \frac{V_{OC}}{I_{OCSET(min)}} = \frac{107.6\,mV}{9.0\,\mu A} = 12.0k\Omega \approx 12.1k\Omega \quad (40)$$

A 1000 pF capacitor is placed in parallel to improve noise immunity of the current limit set-point.

8.2.2.17 SCP Multiplier Selection (R5)

The TPS40170 controller uses a multiplier (A_{OC}) to translate the low-side over-current protection into a high-side $R_{DS(on)}$ pulse-by-pulse short circuit protection. Ensure that Equation 41 is true.

$$A_{OC} > \frac{I_{OCP(min)} + \left(\frac{1}{2} \times I_{RIPPLE}\right)}{I_{OCP(min)} + \left(\frac{1}{2} \times I_{RIPPLE}\right)} \times \frac{R_{DS(on)Q1}}{R_{DS(on)Q2}} = \frac{8\,A + \frac{1}{2} \times 1.86\,A}{8\,A + \frac{1}{2} \times 1.86\,A} \times \frac{11\,m\Omega}{7.6\,m\Omega} = 1.45 \tag{41}$$

A_{OC} = 3 is selected as the next greater A_{OC}. The value of R5 is set to 10 kΩ.

8.2.2.18 Feedback Divider (R10, R11)

The TPS40170 controller uses a full operational amplifier with an internally fixed 0.6 V reference. The value of R11 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With the value of R11 set to 20 kΩ, the output voltage is programmed with a resistor divider given by Equation 42.

$$R10 = \frac{V_{FB} \times R11}{\left(V_{OUT} - V_{FB}\right)} = \frac{0.600\,V \times 20.0\,k\Omega}{\left(5.0\,V - 0.600\,V\right)} = 2.73\,k\Omega \approx 2.74\,k\Omega \tag{42}$$

8.2.2.19 Compensation: (R4, R13, C13, C14, C21)

Using the TPS40k Loop Stability Tool for a 60 kHz bandwidth and a 50° phase margin with an R11 value of 20.0 kΩ, the following values are obtained. The tool is available from the TI website, SLUC263.

- C21 = C1 = 1500 pF
- C13 = C2 = 8200 pF
- C14 = C3 = 220 pF
- R13 = R2 = 511 Ω
- R4 = R3 = 3.83 kΩ

8.2.3 Application Curves

Figure 36 shows an input from 10 V to 60 V for an output of 5.0 V at 6 A, efficiency graph for this design. Figure 37 shows an input of 24 V for an output of 5.0 V at 6 A, loop response where V_{IN} = 24V and I_{OUT} = 6A, yielding 58 kHz bandwidth, 51° phase margin. Figure 38 shows the output ripple 20 mV/div, 2 µs/div, 20 MHz bandwidth.

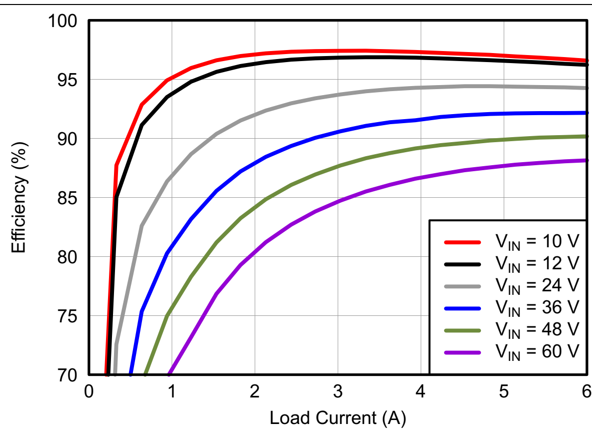


Figure 36. Efficiency vs. Load Current

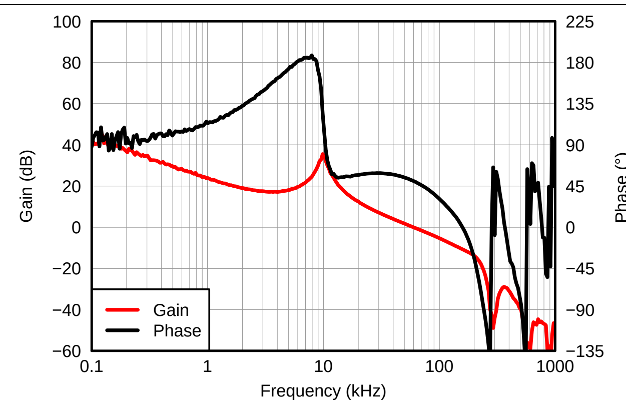


Figure 37. Loop Response

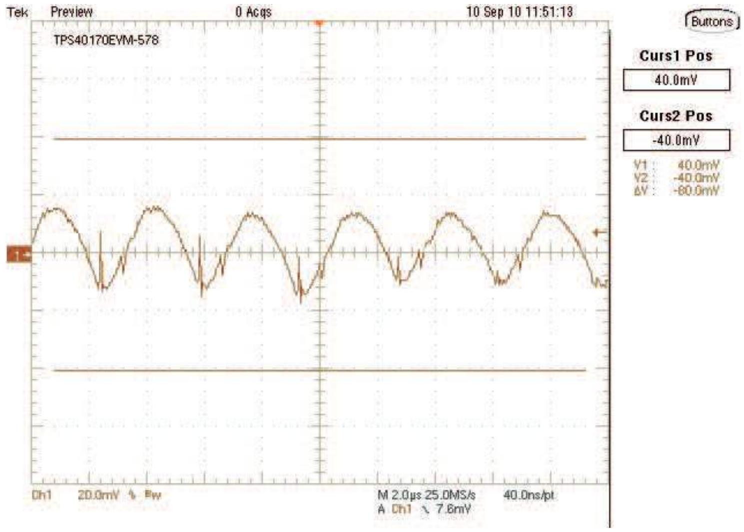


Figure 38. Output Ripple Waveform

9 Power Supply Recommendations

The TPS40170 is designed for operation from an input voltage supply range between 4.5 V and 60 V. Good regulation of this input supply is essential. If the input supply is more distant than a few inches from the TPS40170 and the buck power stage, the circuit may require additional bulk capacitance in addition to ceramic bypass capacitors. An electrolytic capacitor with a value of 120 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Figure 39 illustrates an example layout. For the controller, it is important to carefully connect noise sensitive signals such as RT, SS, FB, and comp as close to the IC as possible and connect to AGND as shown. The PowerPad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The AGND and PGND should be connected at a single point.

When using high-performance FETs such as NexFET™ from Texas Instruments, careful attention to the layout is required. Minimize the distance between positive node of the input ceramic capacitor and the drain pin of the control (high-side) FET. Minimize the distance between the negative node of the input ceramic capacitor and the source pin of the syncronization (low-side) FET. Becasue of the large gate drive, smaller gate charge, and faster turn-on times of the high-performance FETs, it is recommended to use a minimum of 4, 10 µF ceramic input capacitors such as TDK #C3216X5R1A106M. Ensure the layout allows a continuous flow of the power planes.

The layout of the HPA578 EVM is shown in Figure 39 through Figure 42 for reference.

10.2 Layout Example

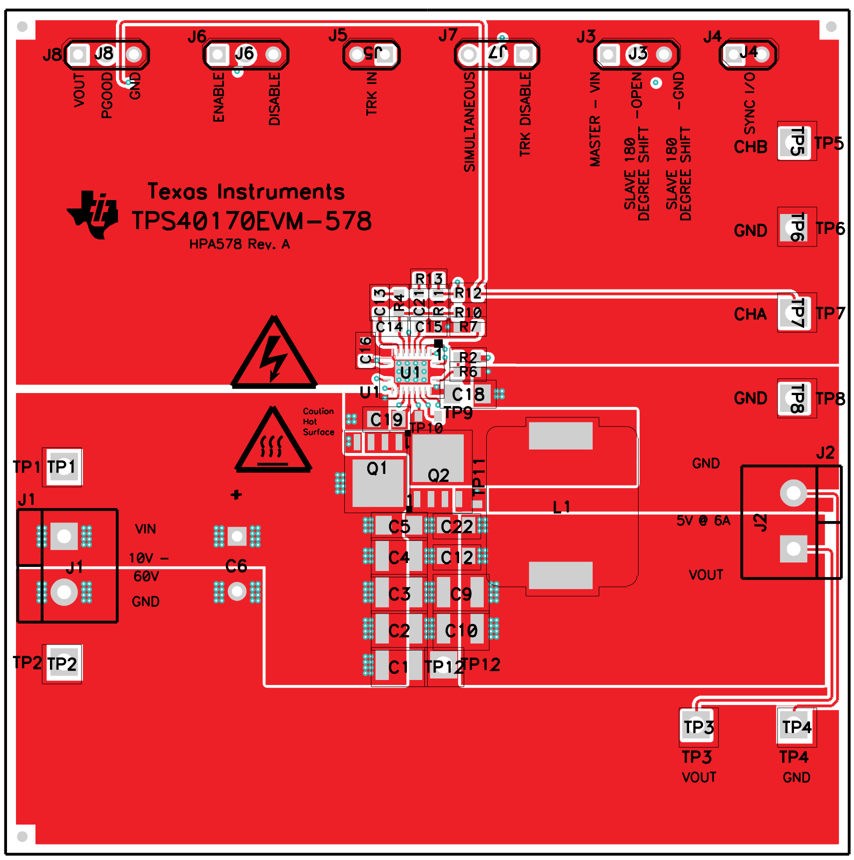


Figure 39. Top Copper, Viewed From Top

Layout Example (continued)

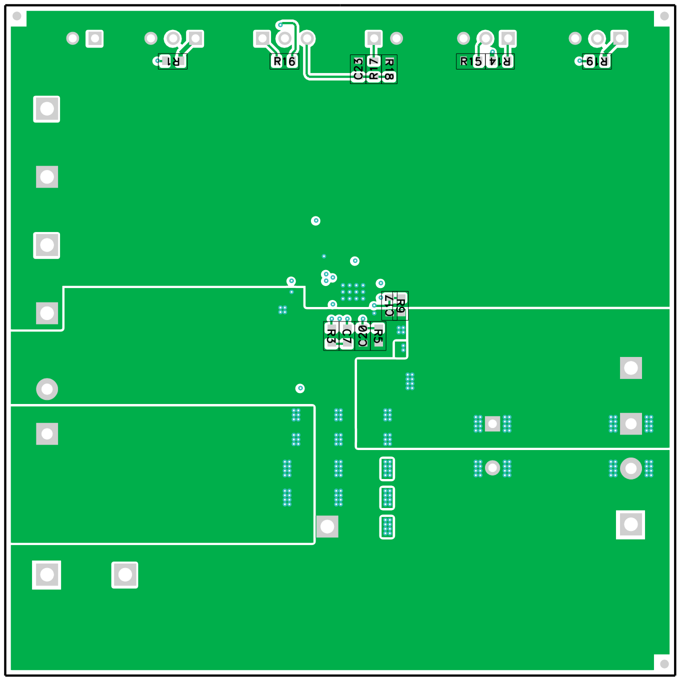


Figure 40. Bottom Copper, Viewed From Bottom

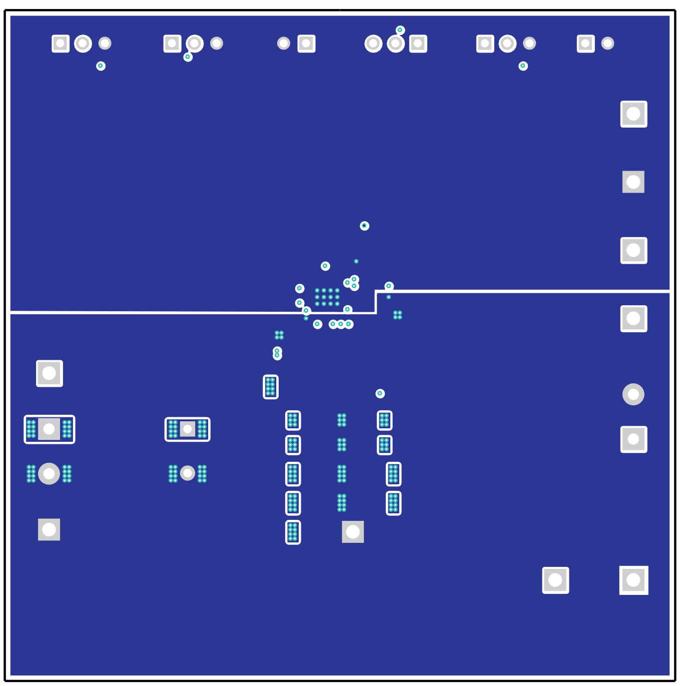


Figure 41. Internal Layer 1, Viewed from Top

Layout Example (continued)

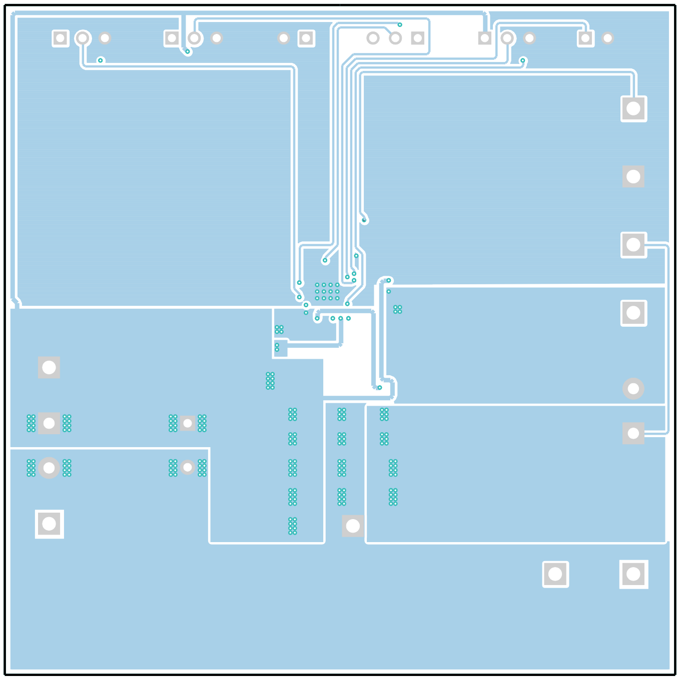


Figure 42. Internal Layer 2, Viewed from Top

11 Device and Documentation Support

11.1 Custom Design with WEBENCH Tools

Create a Custom Design with WEBENCH Tools

11.2 Device Support

11.2.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2.2 Related Devices

The following device has characteristics similar to the TPS40170 and may be of interest.

DEVICE	DESCRIPTION
TPS40057	Wide Input Synchronous Buck Controller

11.3 Trademarks

WEBENCH is a registered trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40170RGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40170	Samples
TPS40170RGYT	ACTIVE	VQFN	RGY	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40170	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS40170 :

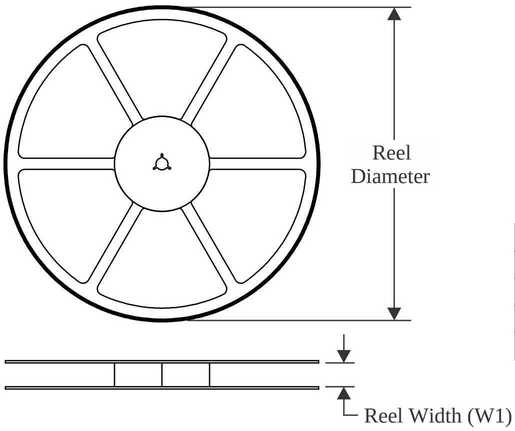
- Automotive: TPS40170-Q1
- Enhanced Product: TPS40170-EP

NOTE: Qualified Version Definitions:

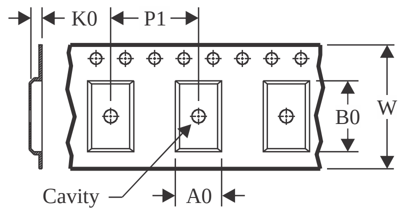
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

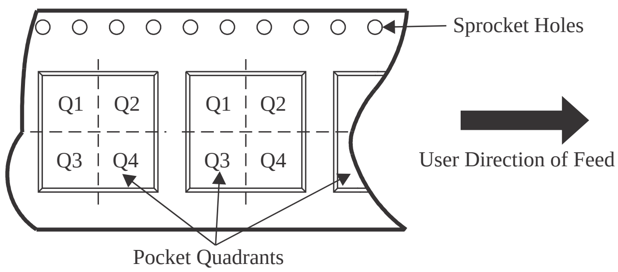


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

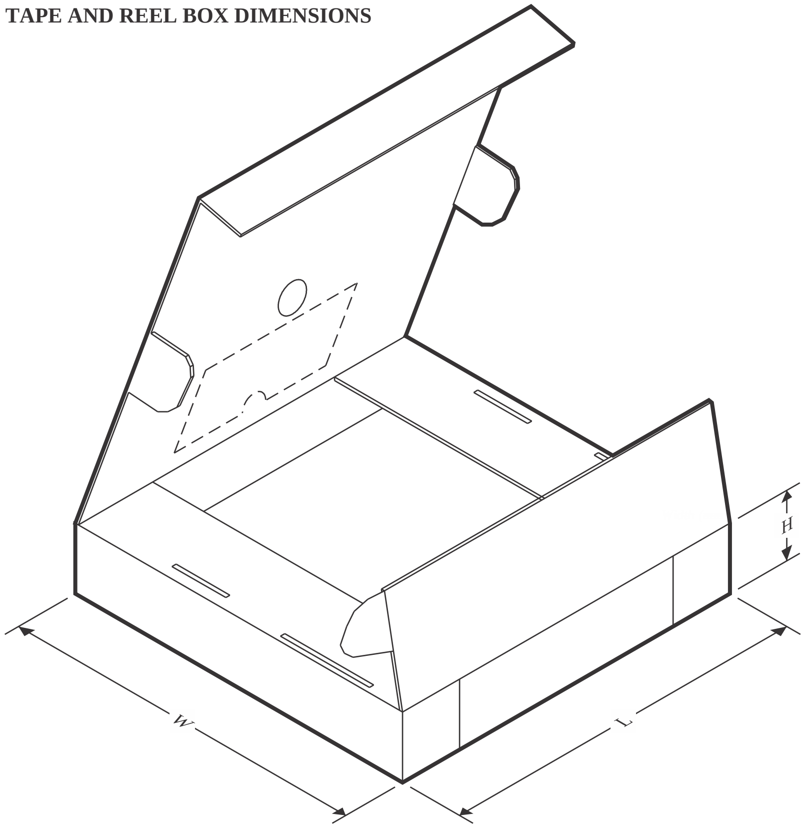
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40170RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TPS40170RGYT	VQFN	RGY	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

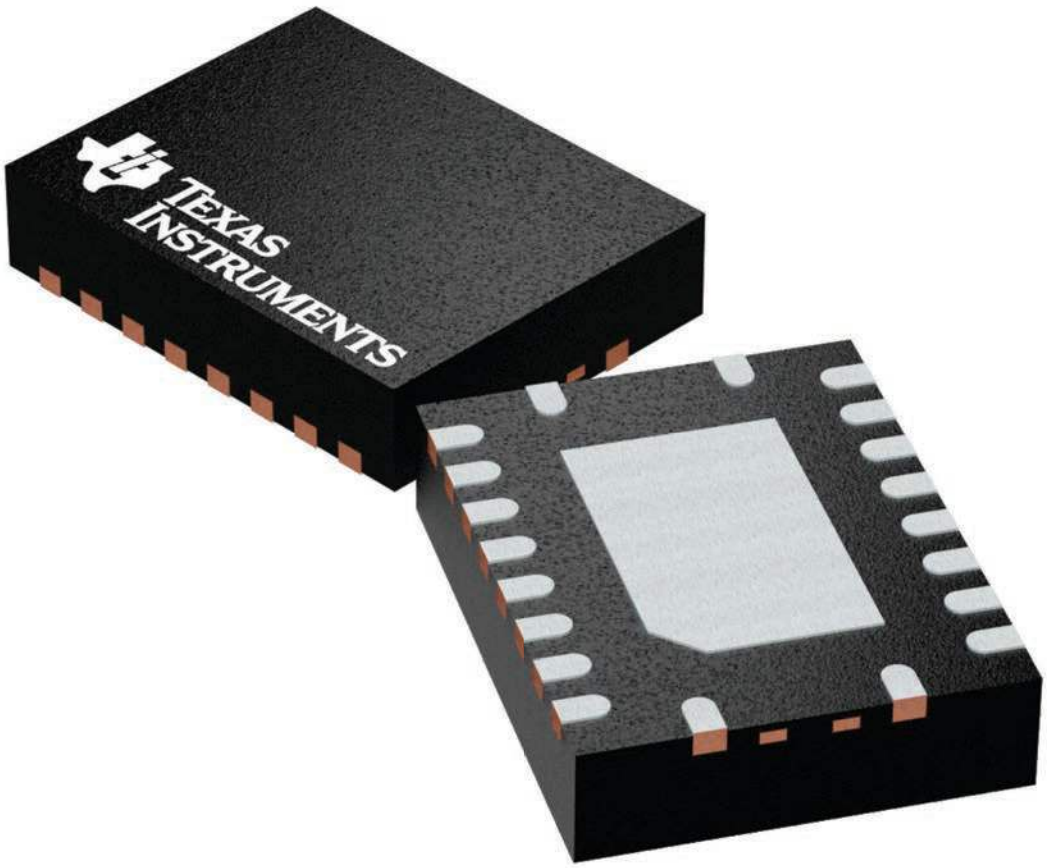
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40170RGYR	VQFN	RGY	20	3000	356.0	356.0	35.0
TPS40170RGYT	VQFN	RGY	20	250	210.0	185.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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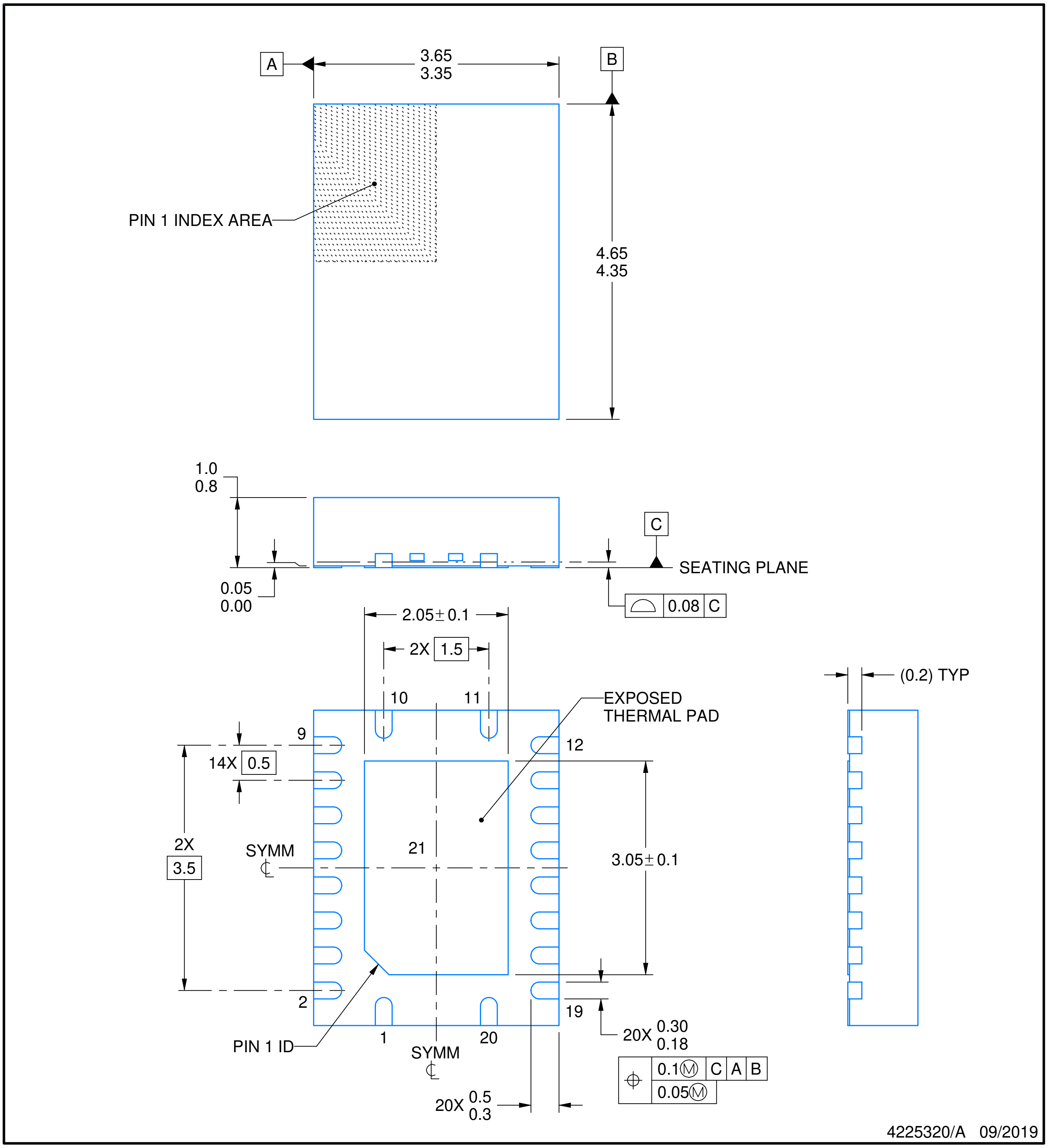
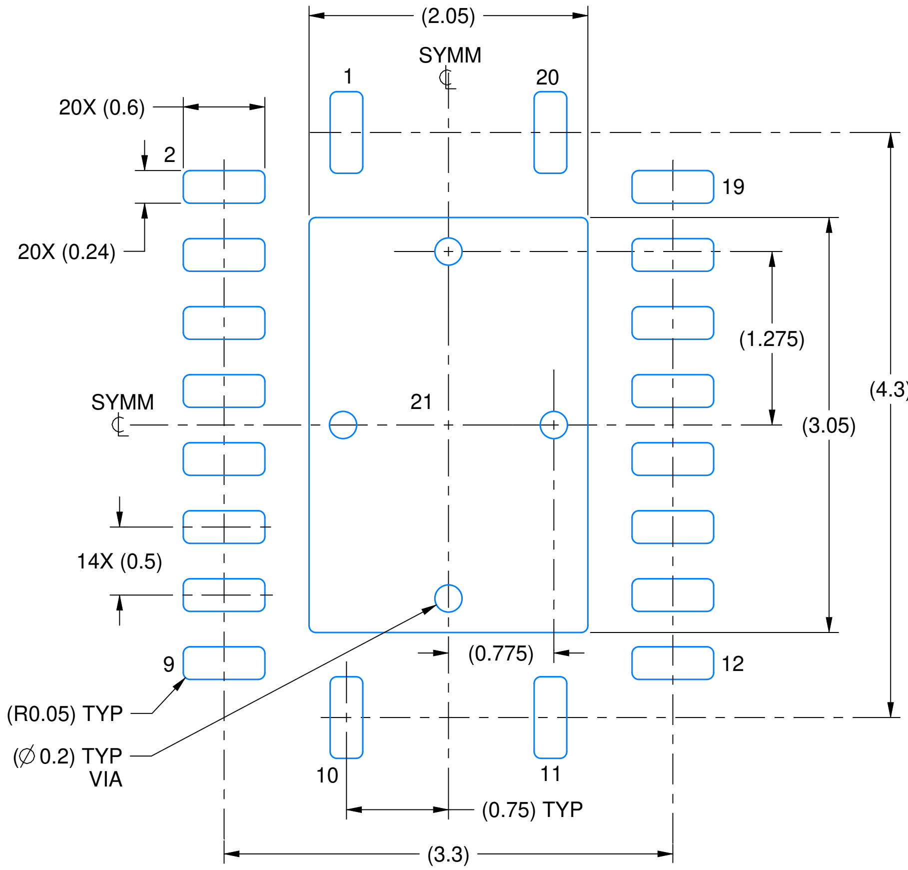
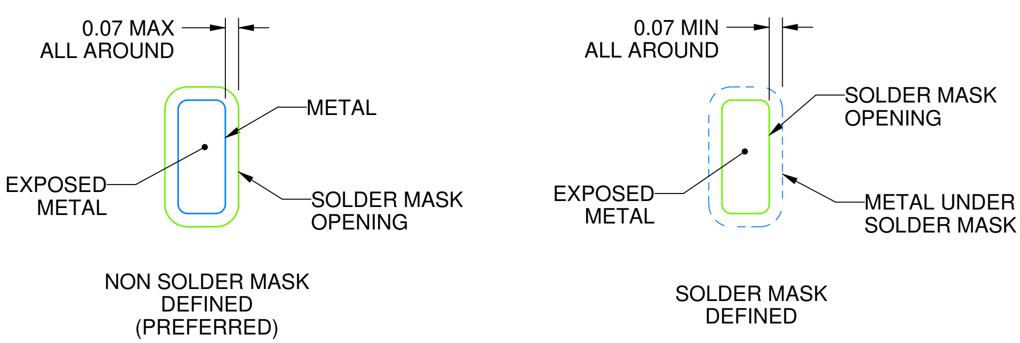


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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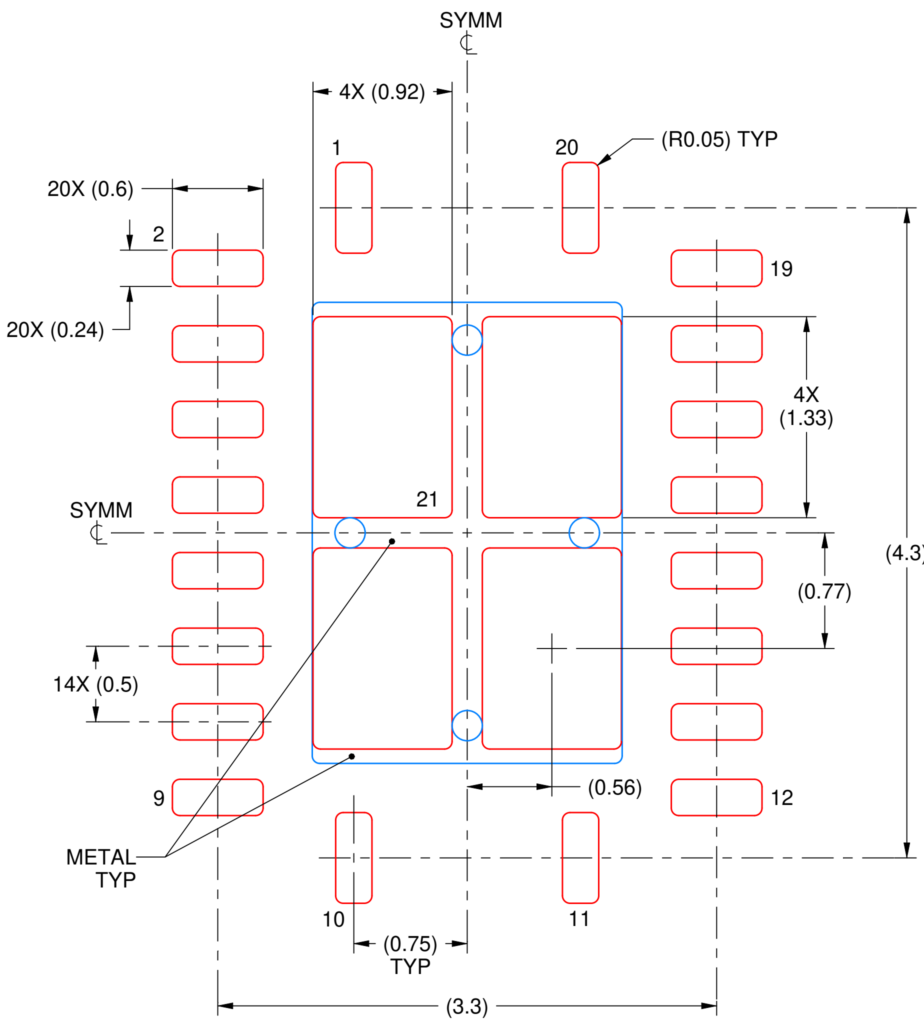
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.