





DUAL COMPLEMENTARY PRE-BIASED TRANSISTORS

Features

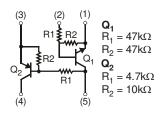
- Epitaxial Planar Die Construction
- Surface Mount Package Suited for Automated Assembly
- Simplifies Circuit Design and Reduces Board Space
- Lead Free, RoHS Compliant (Note 1)
- Halogen and Antimony Free "Green" Device (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SOT353
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed Over Alloy 42 Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.006 grams (approximate)



Bottom View
Package Pin Out
Configuration



Device Schematic

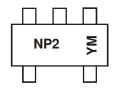
Ordering Information (Note 3)

Part Number	Case	Packaging		
UMC5N-7	SOT353	3000/Tape & Reel		

Notes:

- 1. No purposefully added lead.
- 2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com.
- 3. For packaging details, go to our website at http://www.diodes.com.

Marking Information



NP2 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: U = 2007) M = Month (ex: 9 = September)

Date Code Key

Year	2007	20	08	2009	2010	20	11	2012	2013	20	14	2015
Code	U	\	/	W	Х	,	Y	Z	Α	E	3	С
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings, Pre-Biased NPN Transistor, Q₁ @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage	V _{CC}	50	V
Input Voltage	V _{IN}	-10 to +40	V
Output Current	l ₀	30	mA
Collector Current	I _{C(MAX)}	100	mA

Maximum Ratings, Pre-Biased PNP Transistor, Q₂ @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage	Vcc	-50	V
Input Voltage	V_{IN}	-20 to +7	V
Output Current	lo	-100	mA
Collector Current	I _{C(MAX)}	-100	mA

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	P_{D}	150	mW
Thermal Resistance, Junction to Ambient Air (Note 4)	$R_{ heta JA}$	833	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Notes:

Electrical Characteristics, Pre-Biased NPN Transistor, Q₁ @T_A = 25°C unless otherwise specified

Characteristic		Symbol	Min	Тур	Max	Unit	Test Condition
Innut Voltage	(Note 5)	V _{I(OFF)}	0.5	_		V	$V_{CC} = 5V, I_{O} = 100 \mu A$
Input Voltage	(Note 6)	$V_{I(ON)}$	_	_	3	V	$V_O = 0.3V, I_O = 2mA$
Output Voltage		V _{O(ON)}	_	0.1	0.3	V	$I_{O}/I_{I} = 10 \text{mA}/0.5 \text{ mA}$
Input Current		lı	_	_	0.18	mA	$V_I = 5V$
Output Current		I _{O(OFF)}	_	_	0.5	μΑ	$V_{CC} = 50V, V_{I} = 0V$
DC Current Gain		Gı	68	_	_	_	$V_{O} = 5V, I_{O} = 5mA$
Gain-Bandwidth Product (Note 7)		f _T	_	250	_	MHz	$V_{CE} = 10V$, $I_{E} = -5mA$, $f = 100MHz$
Input Resistance		R ₁	32.9	47	61.1	kΩ	_
Resistance Ratio		R ₂ /R ₁	0.8	1	1.2	_	

Notes:

- 5. The device is guaranteed to be in "OFF" state with $V_{I(OFF)}$ up to 0.5V 6. The device is guaranteed to be in "ON" state with $V_{I(ON)}$ starting from 3V
- 7. Characteristic of Transistor for reference only.

Electrical Characteristics, Pre-Biased PNP Transistor, Q₂ @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
Input Voltage	$V_{I(OFF)}$	-0.3	_	_	V	$V_{CC} = -5V$, $I_{O} = -100\mu A$
input voitage	$V_{I(ON)}$	_	_	-2.5	V	$V_O = -0.3V$, $I_O = -20mA$
Output Voltage	V _{O(ON)}	_	-0.1	-0.3	V	$I_{O}/I_{I} = -10 \text{mA}/-0.5 \text{ mA}$
Input Current	lı	_	_	-1.8	mA	V _I = -5V
Output Current	I _{O(OFF)}	_	_	-0.5	μΑ	$V_{CC} = -50V, V_{I} = 0V$
DC Current Gain	Gı	30	_	_	_	$V_O = -5V, I_O = -10mA$
Gain-Bandwidth Product (Note 7)	f _T	_	250	_	MHz	$V_{CE} = -10V$, $I_{E} = 5mA$, $f = 100MHz$
Input Resistance	R ₁	3.29	4.7	6.11	kΩ	_
Resistance Ratio	R ₂ /R ₁	1.7	2.1	2.6	_	_

Notes:

- 8. The device is guaranteed to be in "OFF" state with $V_{\text{I(OFF)}}\,\text{up}$ to -0.3V
- 9. The device is guaranteed to be in "ON" state with V_{I(ON)} starting from -2.5V
- 10. Characteristic of Transistor for reference only.

^{4.} Device mounted on FR-4 PCB; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at



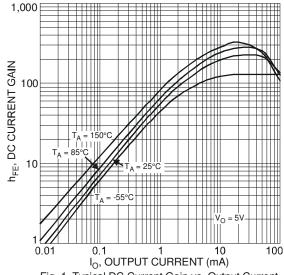


Fig. 1 Typical DC Current Gain vs. Output Current (Q1, NPN)

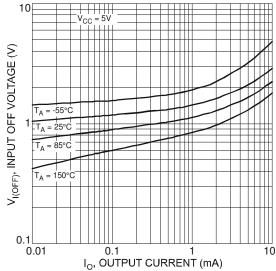


Fig. 3 Typical Input OFF Voltage vs. Output Current (Q1, NPN)

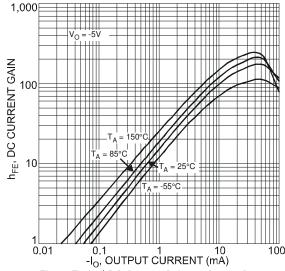


Fig. 5 Typical DC Current Gain vs. Output Current (Q2, PNP)

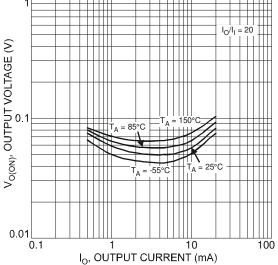


Fig. 2 Typical Output Voltage vs. Output Current (Q1, NPN)

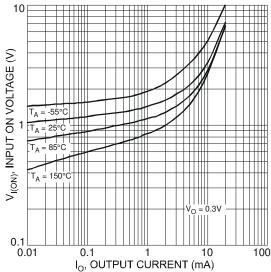
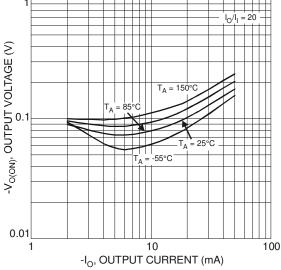
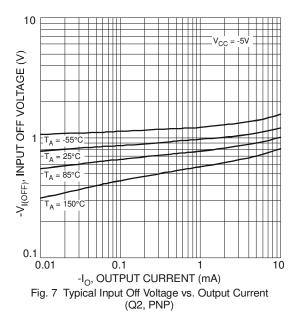


Fig. 4 Typical Input ON Voltage vs. Output Current (Q1, NPN)



-I_O, OUTPUT CURRENT (mA)
Fig. 6 Typical Output Voltage vs. Output Current (Q2, PNP)





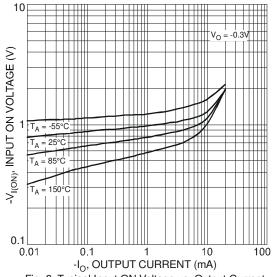
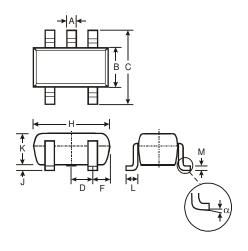


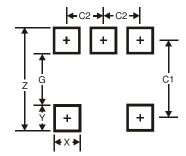
Fig. 8 Typical Input ON Voltage vs. Output Current (Q2, PNP)

Package Outline Dimensions



SOT353						
Dim	Min	Max				
Α	0.10	0.30				
В	1.15	1.35				
С	2.00	2.20				
D	0.65 Typ					
F	0.40	0.45				
Н	1.80	2.20				
J	0	0.10				
K	0.90 1.00					
L	0.25 0.40					
M	0.10 0.22					
α	0° 8°					
All Dimensions in mm						

Suggested Pad Layout



value (in mm)
2.5
1.3
0.42
0.6
1.9
0.65



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