High Output Current, Rail-to-Rail Input/Output Single CMOS Operational Amplifiers

■ GENERAL DESCRIPTION

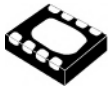
The NJU77903 is CMOS operational amplifier combines full swing input and output with operating up to 36V.

It outputs typically up to 200mA of peak-to-peak current to drive low resistance load including inductance load such as Angle resolver, Lineout cable and Piezo actuator.

In addition, it has enhanced RF noise immunity.

■ PACKAGE OUTLINE

NJU77903DL3
(TO252-5)



NJU77903KW2
(DFN8−W2(ESON8-W2))

■ FEATURES

● High output current	±100mA typ. (200mApp typ.)
● Wide Operating Temperature	Topr = -40ºC to +125ºC
● Rail-to-Rail Input / Output	
● Enhanced RF noise immunity	
● Wide Operating Voltage	6.8V to 36V
● Supply Current	9.5mA typ.
● Open Loop Gain	100dB typ.
● Input Bias Current	1pA typ.
● Slew Rate	3.5V/μs typ.
● Unity Gain Frequency	1.5MHz typ.
● Thermal shutdown	
● Current Limit	
● Package Outline	TO252-5
	DFN8−W2 **(**ESON8-W2/Size: 3mm x 3mm)

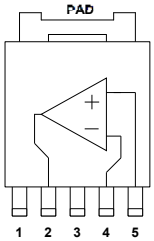
■ APPLICATIONS

- Angle Resolver
- Motor Driver
- Speaker Driver
- 4mA to 20mA Transmitter
- Liner Power Booster

■ PIN CONFIGURATION

NJU77903DL3 (TO252-5)

[TOP VIEW]



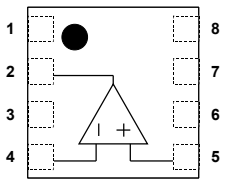
NJU77903DL3 PIN CONFIGURATION

1 V^+
2 OUTPUT
3 V^-
4 −INPUT
5 +INPUT

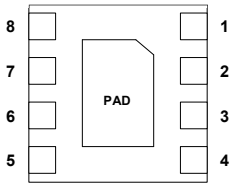
Exposed pad should connect with a V^- terminal.

NJU77903KW2 (DFN8−W2(ESON8-W2)**)**

[TOP VIEW]



[BOTTOM VIEW]



NJU77903KW2 PIN CONFIGURATION

1 NC
2 OUTPUT
3 V^-
4 −INPUT
5 +INPUT
6 LIM2 (Output Sink Current Limit Trim Terminal)
7 LIM1 (Output Source Current Limit Trim Terminal)
8 V^+

Exposed pad should connect with a V^- terminal.

The NC pin and The PAD have to be wired as short as possible to connect with a V^- terminal.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25ºC, unless otherwise noted.)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V^+ - V^-$	40	V
Differential Input Voltage (Note 1)	V_{ID}	±36	V
Input Voltage (Note 2)	V_{IN}	V^- - 0.3 to V^+ + 0.3	V
Input Current	I_{IN}	±10(Note 3)	mA
Output Voltage (Note 4)	V_O	V^- - 0.3 to V^+ + 0.3	V
Power Dissipation (Note 9) TO252-5 DFN8−W2 (ESON8-W2)	P_D	(2-layer / 4-layer) 1190(Note 5) / 3125(Note 6) 640(Note 7) / 2080(Note 8)	mW
Operating Temperature Range	T_{opr}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

(Note1) Differential voltage is the voltage difference between +INPUT and -INPUT.
(Note2) Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V^+. The normal operation will establish when any input is within the Common Mode Input Voltage Range of electrical characteristics.
(Note3) If the input voltage exceeds the supply voltage,the input current must be limited 10 mA or less by using a restriction resistance.
(Note4) Output voltage is the voltage should be allowed to apply to the output terminal independent of the magnitude of V^+.
(Note5) 2-layer: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layers, FR-4) mounting
(Note6) 4-layer: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 4layers, FR-4) mounting
(Note7) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)
(Note8) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(Note9) Power dissipation is the power that can be consumed by the IC at Ta=25ºC, and is the typical measured value based on JEDEC condition. When using the IC over Ta=25ºC subtract the value [mW/ºC] = PD / (Tstg (MAX)-25) per temperature.
(Note10) The NC pin and The PAD have to be wired as short as possible to connect with a V^- terminal.

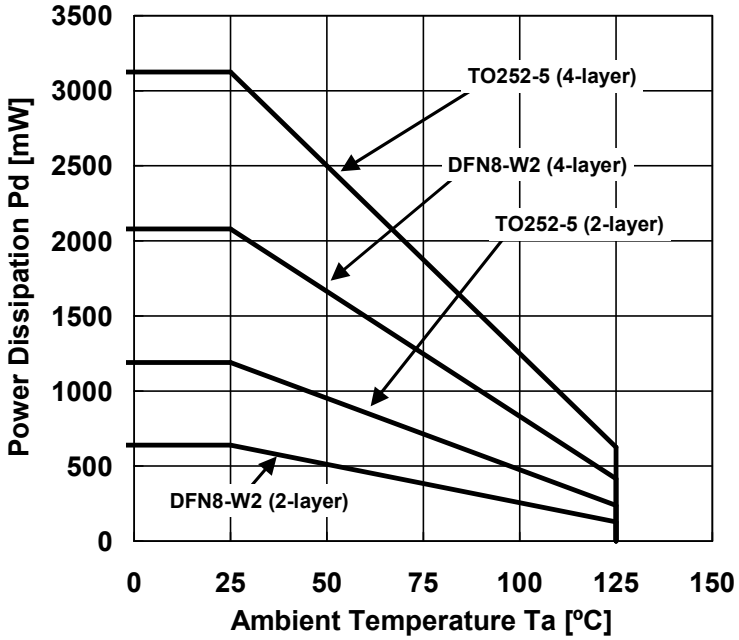


Figure 1 : Power Dissipation Derating Curve

■ RECOMMENDED OPERATING VOLTAGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+-V^-	+6.8 to +36	V

■ ELECTRICAL CHARACTERISTICS

(V^+= +12V, V^-= 0V, V_{IC}= +6V, R_L=10kΩ, Ta=25ºC, unless otherwise noted.)

PARAMETER	PARAMETER	TEST CONDITION	Min.	Typ.	Max.	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}	R_S=50Ω	-	1	6	mV
Input Offset Voltage Drift	ΔVio/ΔT	Ta = -40ºC to 125ºC	-	20	-	μV/ºC
Input Bias Current	I_B		-	1	-	pA
Input Offset Current	I_{IO}		-	1	-	pA
Open Loop Gain	A_V	V_O=1V to 11V, R_L=10kΩ to V^+/2	80	100	-	dB
Common Mode Rejection Ratio	CMR	V_{IC}=0V to 6V, V_{IC}=6V to 12V	55	75	-	dB
Common Mode Input Voltage Range	V_{ICM}	CMR≧55dB	0	-	12	V
OUTPUT CHARACTERISTICS						
Output Voltage	V_{OH}	R_L=10kΩ to V^+/2	11.97	11.99	-	V
		Isource=100mA	11.4	11.65	-	V
	V_{OL}	R_L=10kΩ to V^+/2	-	0.01	0.03	V
		Isink=100mA	-	0.35	0.6	V
Output Source Current Limit1	$I_{SOURCELIM1}$	[NJU77903DL3]	250	375	495	mA
		[NJU77903KW2] : LIM1=OPEN（Figure2-1）				
Output Source Current Limit2	$I_{SOURCELIM2}$	LIM1=V^+（Figure2-1） NJU77903KW2 ONLY	0	50	150	mA
Output Sink Current Limit1	$I_{SINKLIM1}$	[NJU77903DL3]	200	375	545	mA
		[NJU77903KW2] : LIM2=OPEN（Figure2-2）				
Output Sink Current Limit2	$I_{SINKLIM2}$	LIM2=V^-（Figure2-2） NJU77903KW2 ONLY	0	40	120	mA
POWER SUPPLY						
Supply Current	I_{DD}	No Signal, R_L=OPEN	-	9.5	12.5	mA
Supply Voltage Rejection Ratio	SVR	V^+= 6.8V to 36V	70	85	-	dB
DYNAMIC PERFORMANCE						
Unity Gain Frequency	f_T	R_L=10kΩ to V^+/2, C_L=10pF	-	1.5	-	MHz
Phase Margin	ΦM	R_L=10kΩ to V^+/2, C_L=10pF	-	75	-	deg
Slew Rate （Note 11）	SR	G_V=0dB, R_L=10kΩ to V^+/2, C_L=10pF, Vin=4Vpp (4V to 8V)	2.5	3.5	-	V/μs
NOISE PERFORMANCE						
Equivalent Input Noise Voltage	e_n	f=10kHz, R_S=50Ω	-	50	-	nV/√Hz
Total Harmonic Distortion + Noise	THD	G_V=6dB, R_F=10kΩ, R_L=10kΩ, C_L=10pF, Vo=2Vpp, f=10kHz	-	0.03	-	%

(Note 11) Number specified is the slower of the positive and negative slew rates.

■ ELECTRICAL CHARACTERISTICS

(V^+= +15V, V^-= -15V, V_{IC}= 0V, R_L=10kΩ, Ta=25ºC, unless otherwise noted.)

PARAMETER	PARAMETER	TEST CONDITION	Min.	Typ.	Max.	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}	R_S=50Ω	-	2	8	mV
Input Offset Voltage Drift	ΔVio/ΔT	Ta = -40°C to 125°C	-	20	-	μV/°C
Input Bias Current	I_B		-	1	-	pA
Input Offset Current	I_{IO}		-	1	-	pA
Open Loop Gain	A_V	V_O=-14V to +14V, R_L=10kΩ to 0V	80	100	-	dB
Common Mode Rejection Ratio	CMR	V_{IC}=-15V to 0V, V_{IC}=0V to 15V	60	80	-	dB
Common Mode Input Voltage Range	V_{ICM}	CMR≧60dB	-15	-	15	V
OUTPUT CHARACTERISTICS						
Output Voltage	V_{OH}	R_L=10kΩ to V^+/2	14.97	14.99	-	V
		Isource=100mA	14.45	14.70	-	V
	V_{OL}	R_L=10kΩ to V^+/2	-	-14.99	-14.97	V
		Isink=100mA	-	-14.70	-14.45	V
Output Source Currrent Limit1	$I_{SOURCELIM1}$	[NJU77903DL3]	-	400	-	mA
		[NJU77903KW2] : LIM1 terminal = OPEN , (Figure 2-1)				
Output Source Current Limit2	$I_{SOURCELIM2}$	LIM1 terminal=V^+, (Figure 2-1) NJU77903KW2 ONLY	-	60	-	mA
Output Sink Current Limit1	$I_{SINKLIM1}$	[NJU77903DL3] :	-	400	-	mA
		[NJU77903KW2] : LIM2 terminal = OPEN (Figure 2-2)				
Output Sink Current Limit2	$I_{SINKLIM2}$	LIM2 terminal=V^-, (Figure 2-2) NJU77903KW2 ONLY	-	30	-	mA
POWER SUPPLY						
Supply Current	I_{DD}	No Signal, R_L=OPEN	-	12	16	mA
DYNAMIC PERFORMANCE						
Unity Gain Frequency	f_T	R_L=10kΩ to V^+/2, C_L=10pF	-	2	-	MHz
Phase Margin	Φ_M	R_L=10kΩ to V^+/2, C_L=10pF	-	70	-	deg
Slew Rate (Note 12)	SR	G_V=0dB, R_L=10kΩ to V^+/2, C_L=10pF, Vin=4Vpp (-2V to +2V)	-	4	-	V/μs
NOISE PERFORMANCE						
Equivalent Input Noise Voltage	e_n	f=10kHz, R_S=50Ω	-	50	-	nV/√Hz
Total Harmonic Distortion + Noise	THD	G_V=6dB, R_F=10kΩ, R_L=10kΩ, C_L=10pF, Vo=2Vpp, f=10kHz	-	0.03	-	%

(Note 12) Number specified is the slower of the positive and negative slew rates.

■ Output Current Limit Trim Circuit [NJU77903KW2]

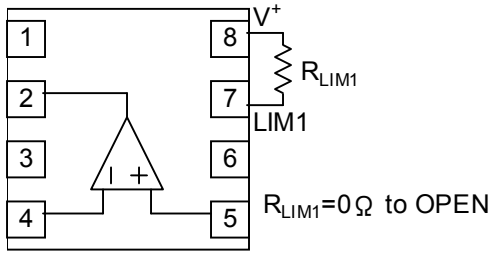


Figure 2-1: Output Source Current Limit Trim

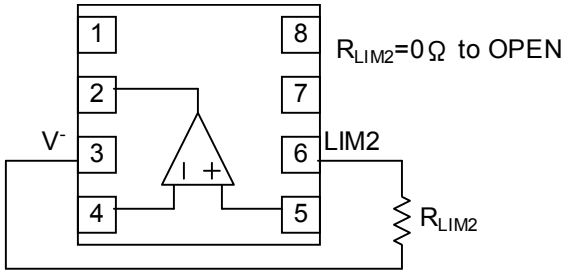
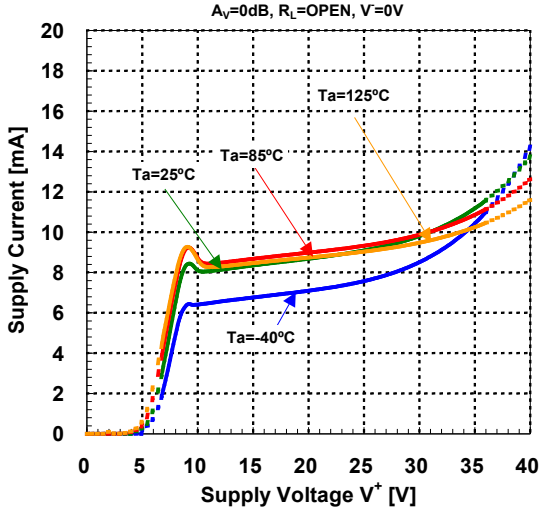


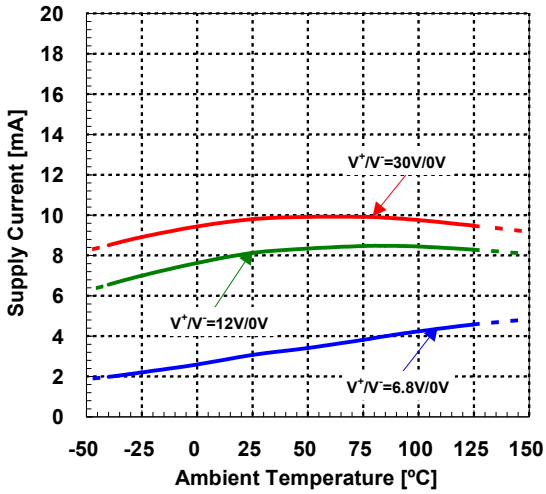
Figure 2-2: Output Sink Current Limit Trim

■ TYPICAL CHARACTERISTICS

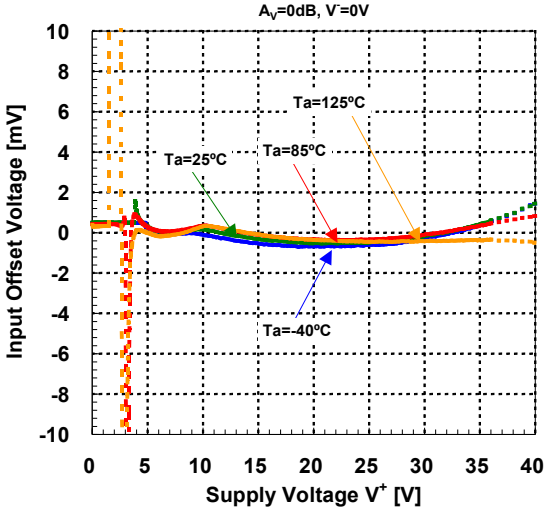
Supply Current vs. Supply Voltage



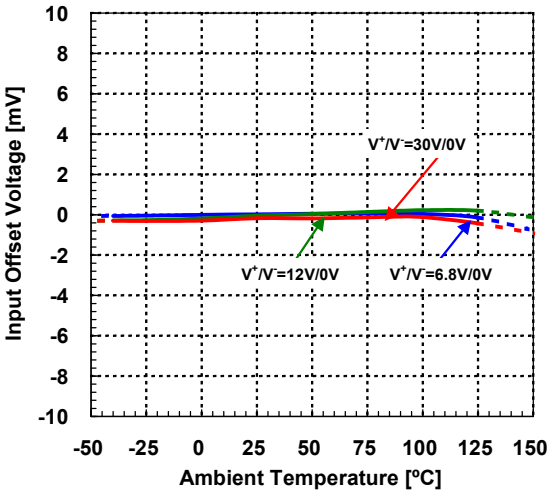
Supply Current vs. Temperature



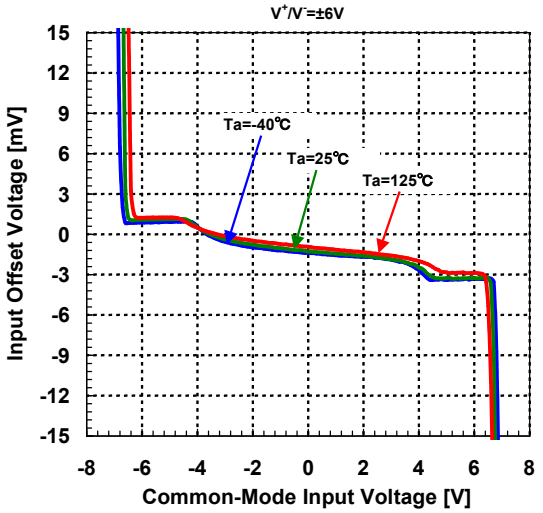
Input Offset Voltage vs. Supply Voltage



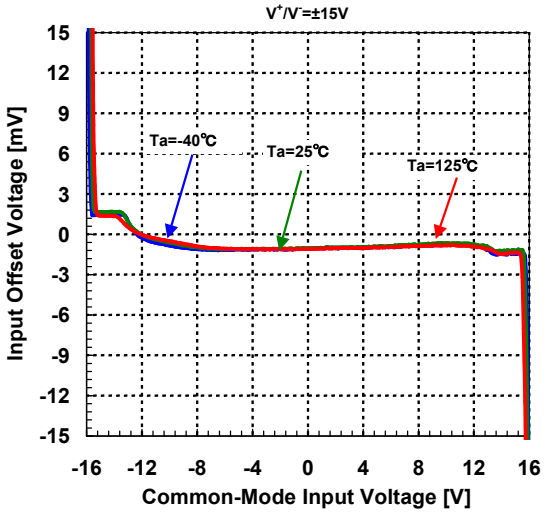
Input Offset Voltage vs. Temperature



Input Offset Voltage vs. Common-Mode Input Voltage

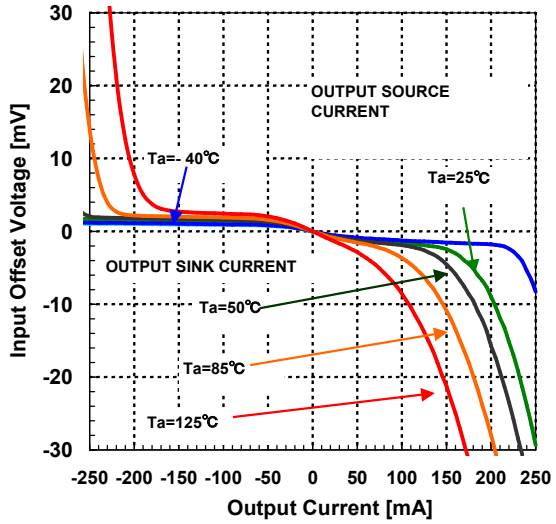


Input Offset Voltage vs. Common-Mode Input Voltage



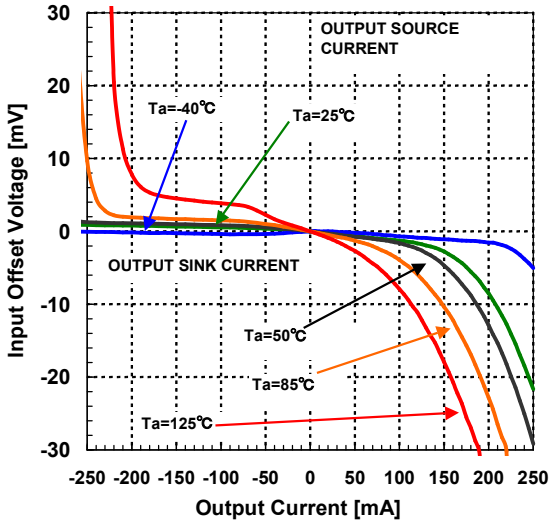
Input Offset Voltage vs. Output Current

V^+/V^-=±6V



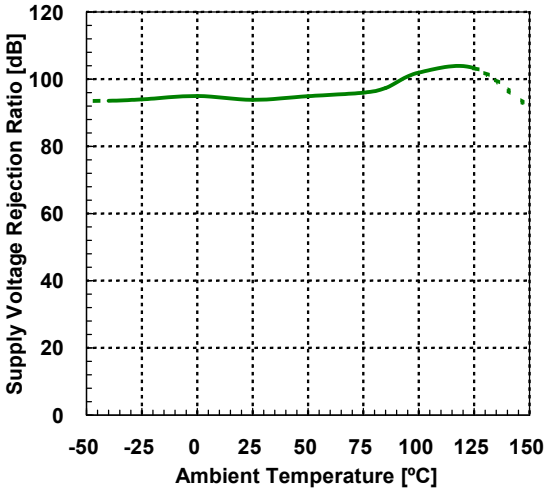
Input Offset Voltage vs. Output Current

V^+/V^-=±15V



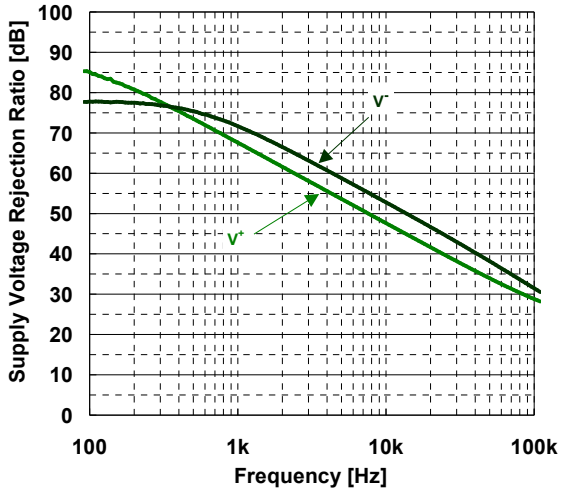
Supply Voltage Rejection Ratio vs. Temperature

V^+=6.8V to 36V , V^-=0V



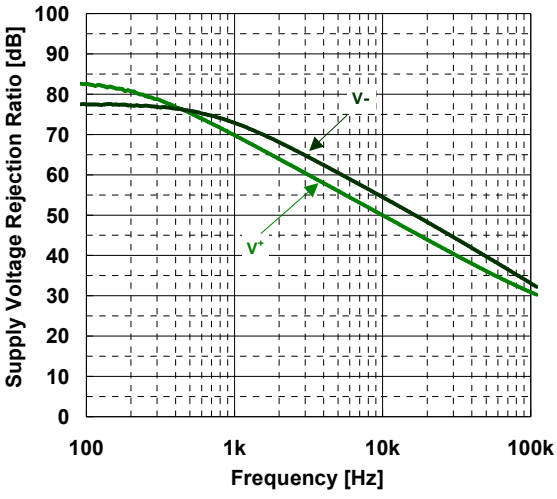
Supply Voltage Rejection Ratio vs. Frequency

V^+/V^-=12V/0V , V_{IN}:2V_{PP}, G_V=40dB, R_S=1kΩ, R_F=100kΩ, Ta=25ºC



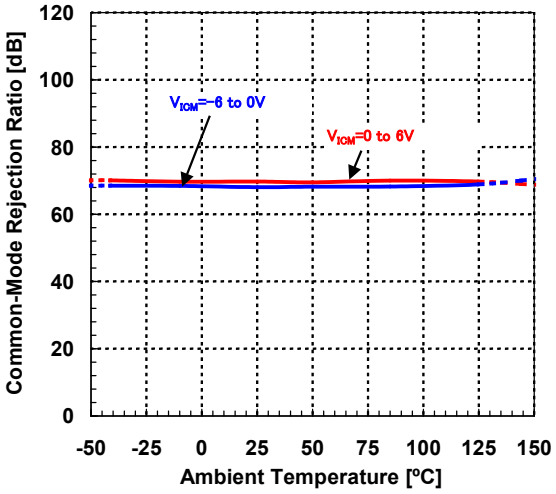
Supply Voltage Rejection Ratio vs. Frequency

V^+/V^-=30V/0V, V_{IN}:2V_{PP}, G_V=40dB, R_S=1kΩ, R_F=100kΩ, Ta=25ºC



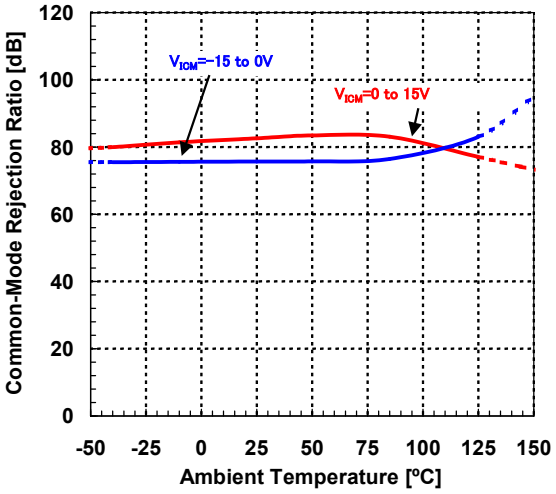
Common-Mode Rejection Ratio vs. Temperature

V^+/V^-=±6V



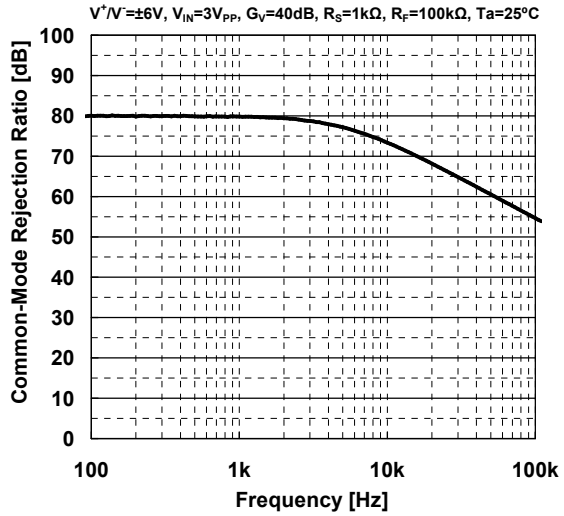
Common-Mode Rejection Ratio vs. Temperature

V^+/V^-=±15V



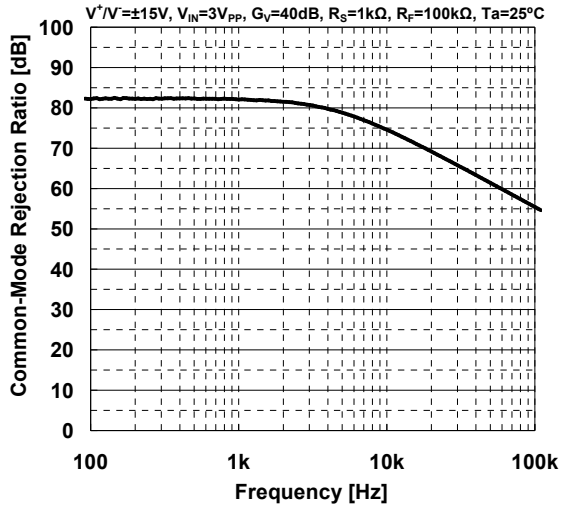
Common-Mode Rejection Ratio vs. Frequency

V^+/V^-=±6V, V_{IN}=3V_{PP}, G_V=40dB, R_S=1kΩ, R_F=100kΩ, Ta=25ºC



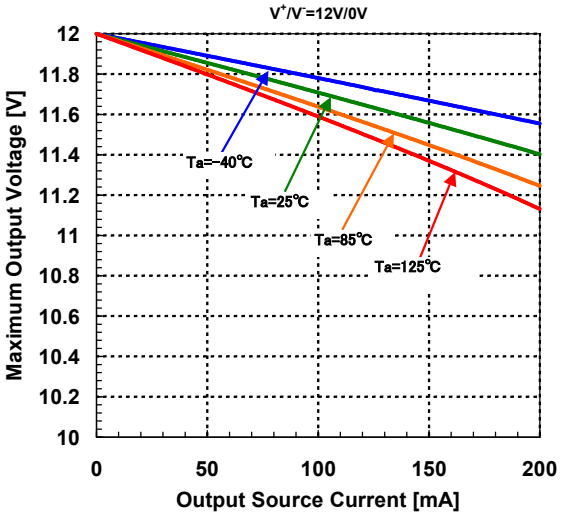
Common-Mode Rejection Ratio vs. Frequency

V^+/V^-=±15V, V_{IN}=3V_{PP}, G_V=40dB, R_S=1kΩ, R_F=100kΩ, Ta=25ºC



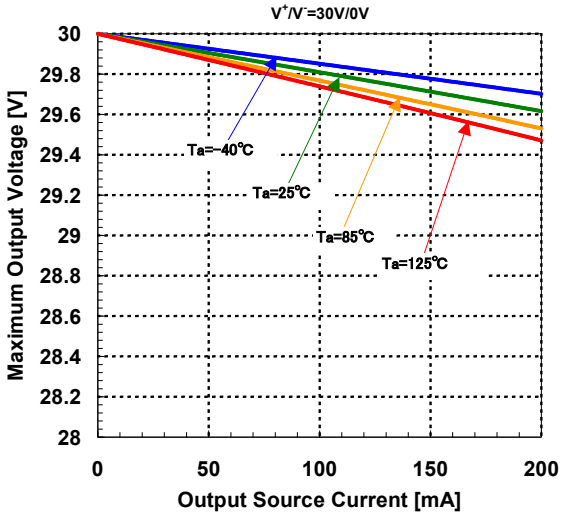
Maximum Output Voltage vs. Output Source Current

V^+/V^-=12V/0V

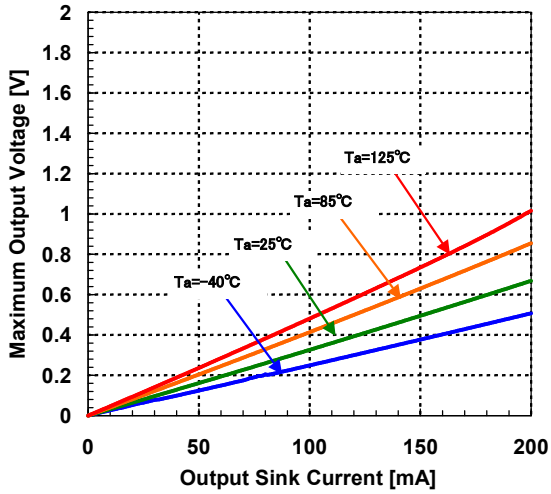


Maximum Output Voltage vs. Output Source Current

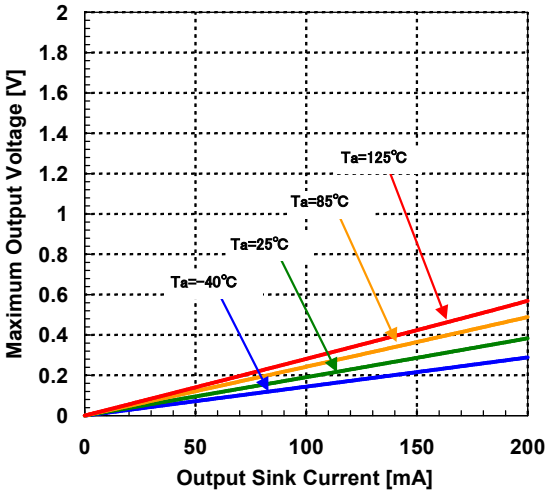
V^+/V^-=30V/0V



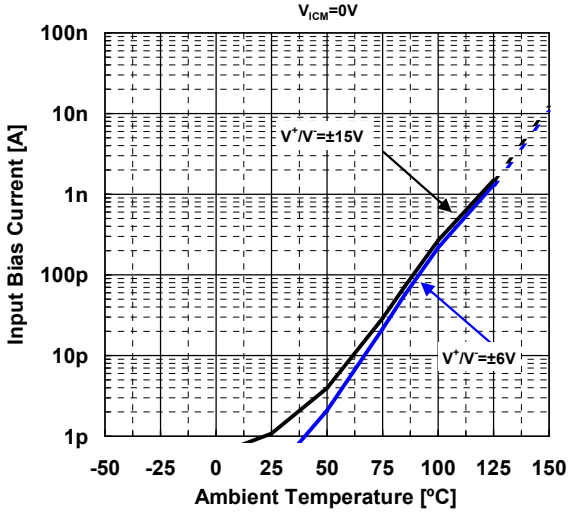
Maximum Output Voltage
vs. Output Sink Current
V^+/V^-=12V/0V



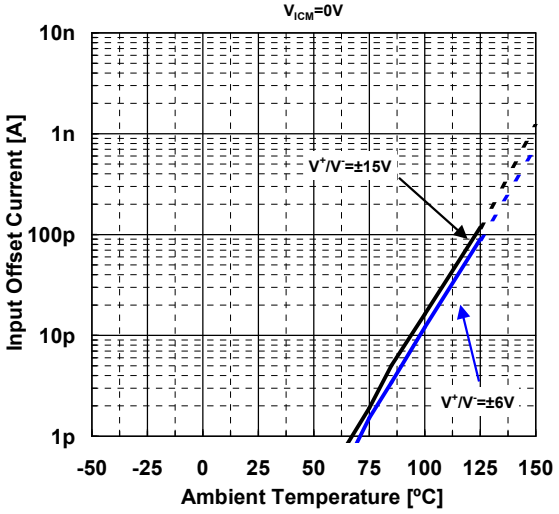
Maximum Output Voltage vs.
Output Sink Current
V^+/V^-=30V/0V



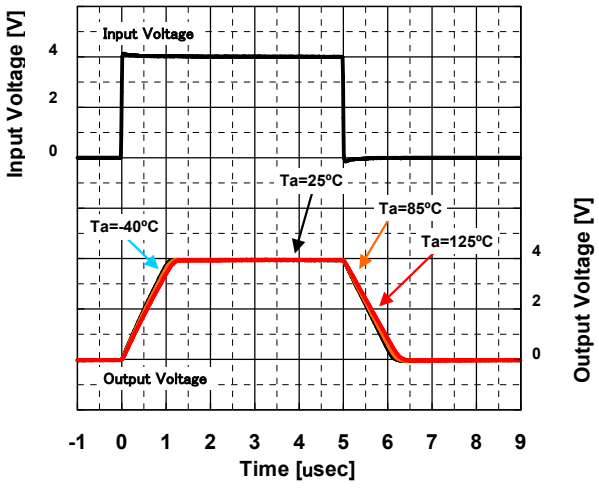
Input Bias Current vs. Temperature
V_{ICM}=0V



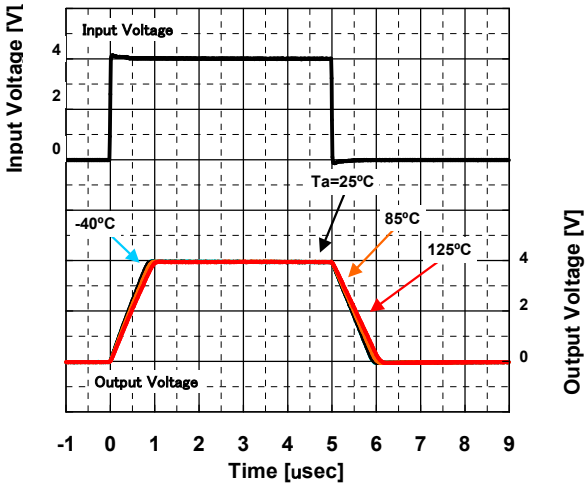
Input Offset Current vs. Temperature
V_{ICM}=0V



Pulse Response
V^+/V^-=±6V, V_{IN}=4V_{P-P}, f=100kHz
PulseEdge=10nsec, Gv=0dB, C_L=10p, R_L=10k

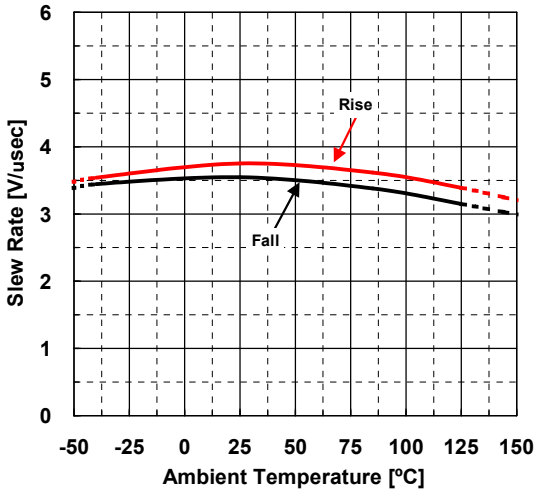


Pulse Response
V^+/V^-=±15V, V_{IN}=4V_{P-P}, f=100kHz
PulseEdge=10nsec, Gv=0dB, C_L=10p, R_L=10k



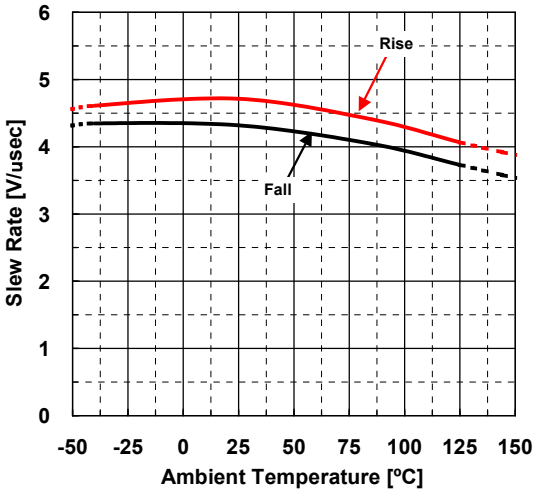
Slew Rate vs. Temperature

V^+/V^-=±6V, V_{IN}=4V_{P-P}, f=100kHz
PulseEdge=10nsec, Gv=0dB, C_L=10p, R_L=10k



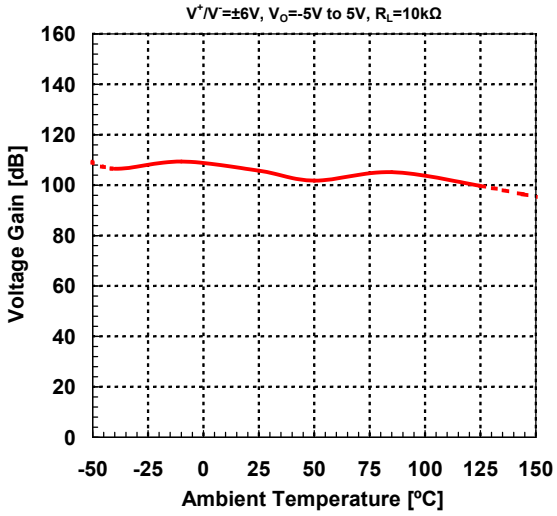
Slew Rate vs. Temperature

V^+/V^-=±15V, V_{IN}=4V_{P-P}, f=100kHz
PulseEdge=10nsec, Gv=0dB, C_L=10p, R_L=10k



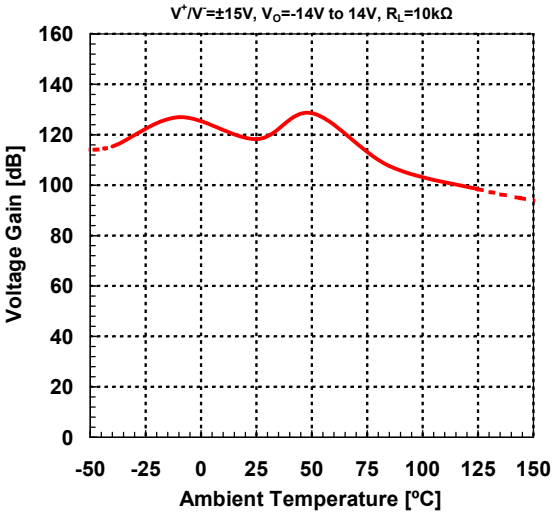
Voltage Gain vs. Temperature

V^+/V^-=±6V, V_O=-5V to 5V, R_L=10kΩ



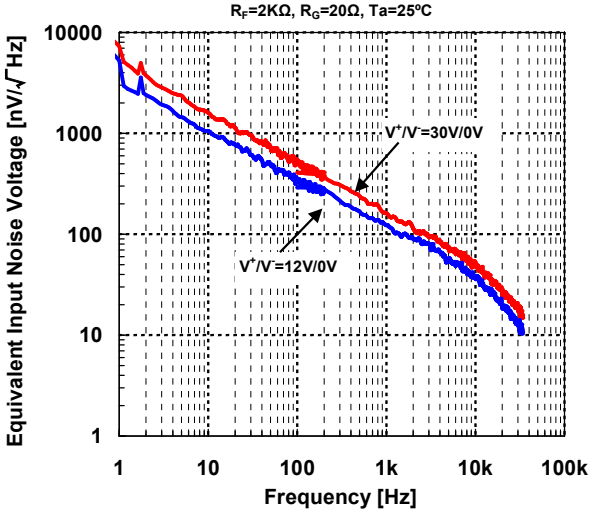
Voltage Gain vs. Temperature

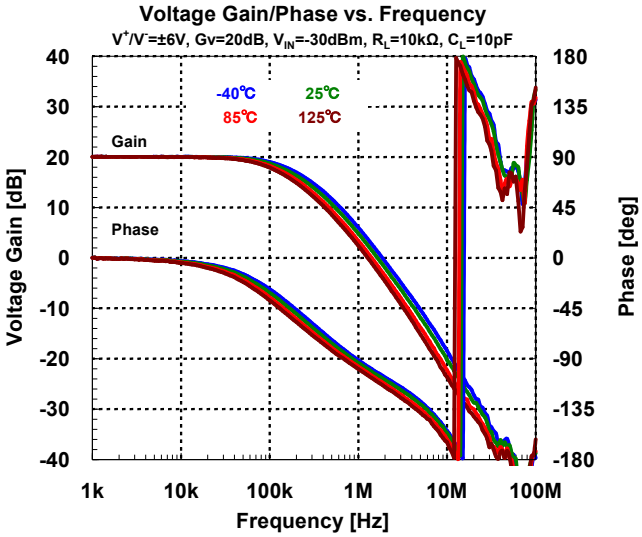
V^+/V^-=±15V, V_O=-14V to 14V, R_L=10kΩ

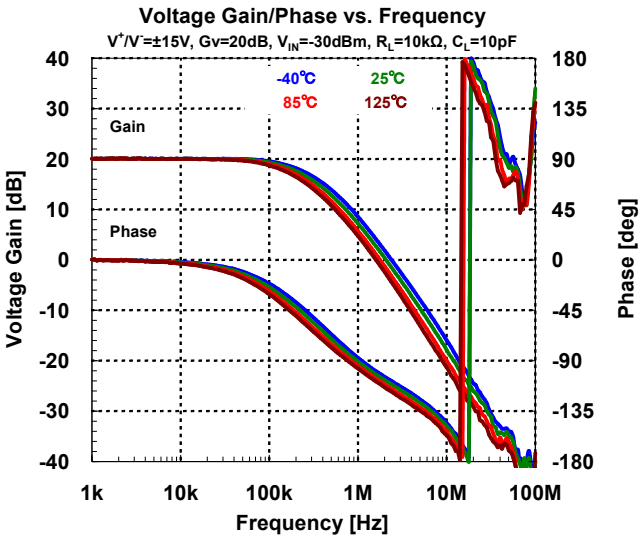


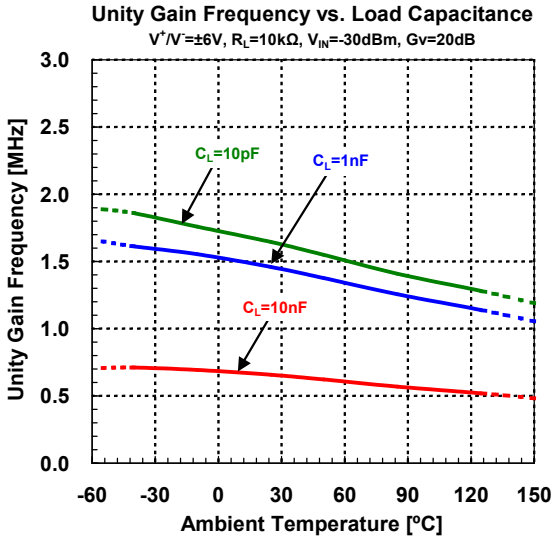
Equivalent Input Noise Voltage vs. Frequency

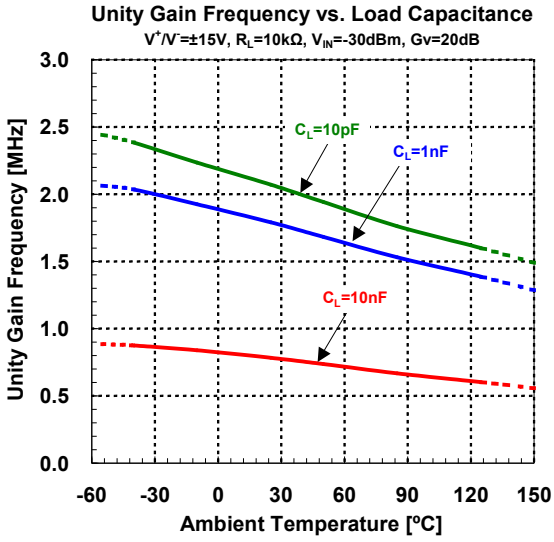
R_F=2KΩ, R_G=20Ω, Ta=25ºC

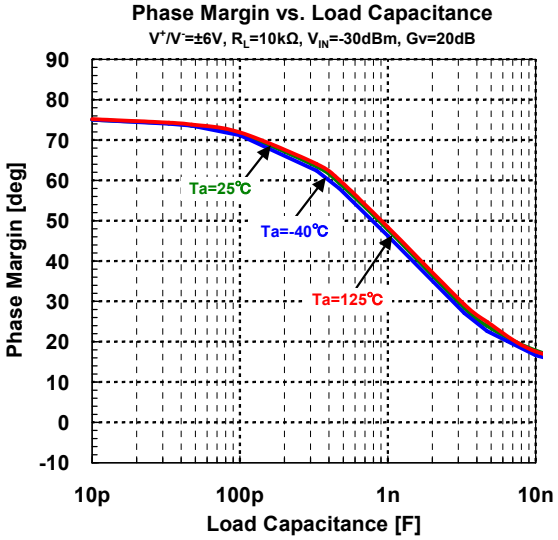


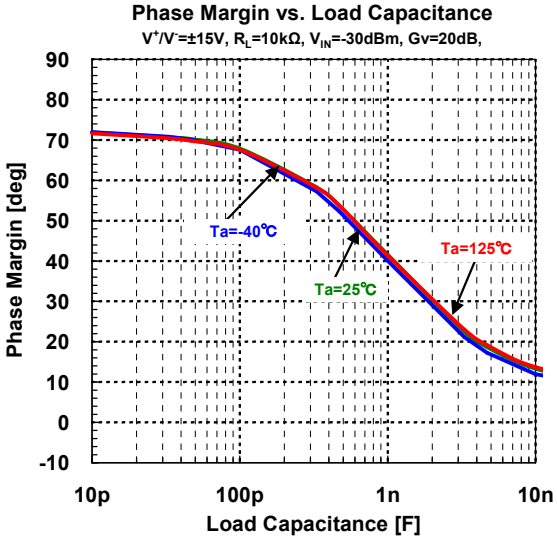

Voltage Gain/Phase vs. Frequency
V+/V-=±6V, Gv=20dB, VIN=-30dBm, RL=10kΩ, CL=10pF
-40℃
25℃
85℃
125℃
Gain
Phase
Voltage Gain [dB]
Phase [deg]
Frequency [Hz]
1k
10k
100k
1M
10M
100M

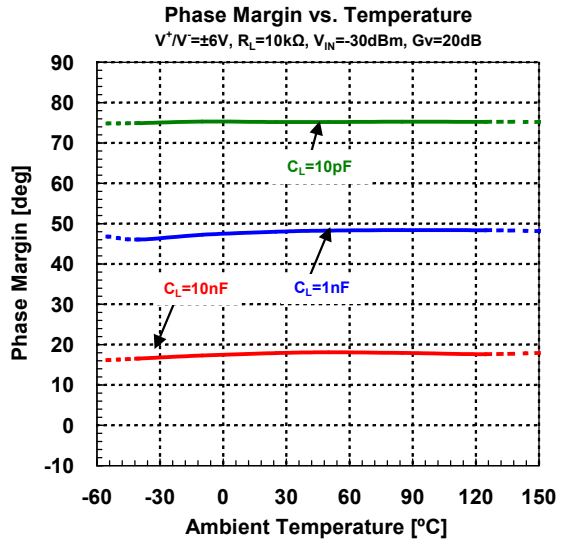

Voltage Gain/Phase vs. Frequency
V+/V-=±15V, Gv=20dB, VIN=-30dBm, RL=10kΩ, CL=10pF
-40℃
25℃
85℃
125℃
Gain
Phase
Voltage Gain [dB]
Phase [deg]
Frequency [Hz]
1k
10k
100k
1M
10M
100M

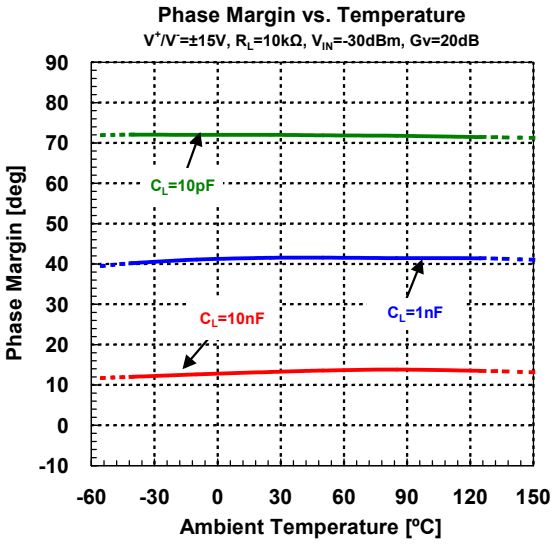

Unity Gain Frequency vs. Load Capacitance
V+/V-=±6V, RL=10kΩ, VIN=-30dBm, Gv=20dB
CL=10pF
CL=1nF
CL=10nF
Unity Gain Frequency [MHz]
Ambient Temperature [ºC]

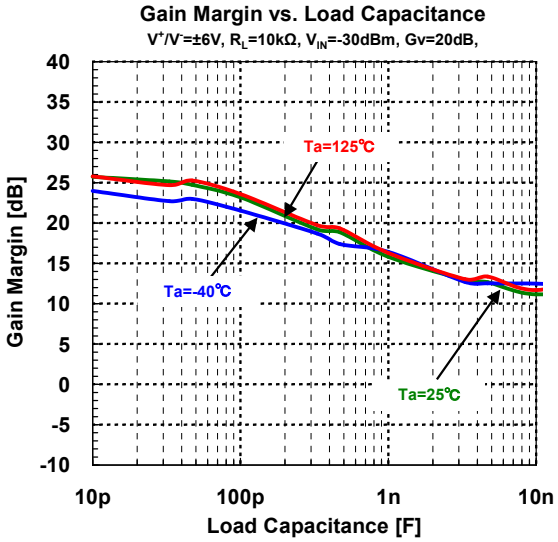

Unity Gain Frequency vs. Load Capacitance
V+/V-=±15V, RL=10kΩ, VIN=-30dBm, Gv=20dB
CL=10pF
CL=1nF
CL=10nF
Unity Gain Frequency [MHz]
Ambient Temperature [ºC]

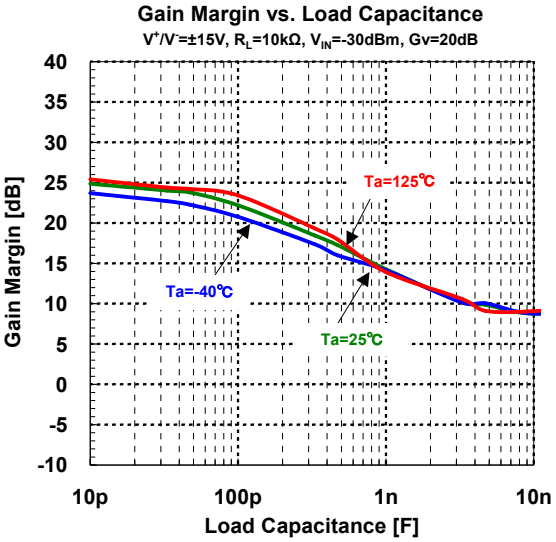

Phase Margin vs. Load Capacitance
V+/V-=±6V, RL=10kΩ, VIN=-30dBm, Gv=20dB
Ta=25℃
Ta=-40℃
Ta=125℃
Phase Margin [deg]
Load Capacitance [F]

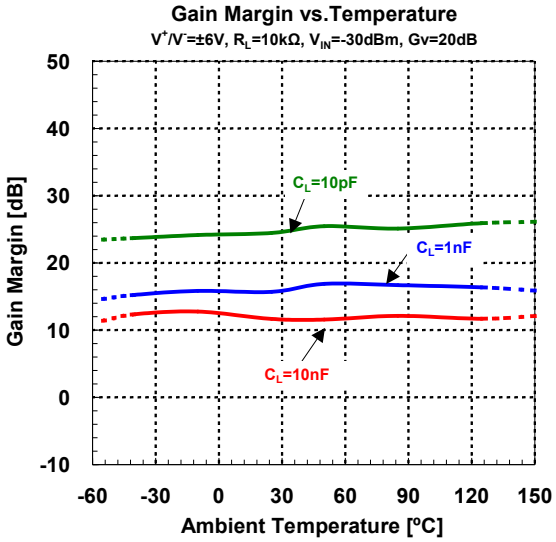

Phase Margin vs. Load Capacitance
V+/V-=±15V, RL=10kΩ, VIN=-30dBm, Gv=20dB,
Ta=-40℃
Ta=25℃
Ta=125℃
Phase Margin [deg]
Load Capacitance [F]

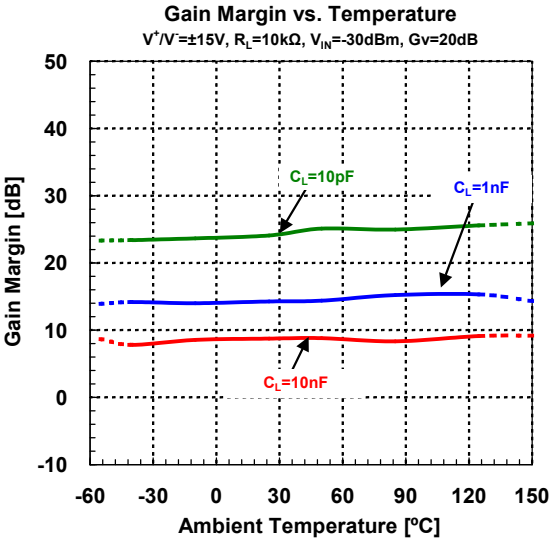

Phase Margin vs. Temperature
V+/V-=±6V, RL=10kΩ, VIN=-30dBm, Gv=20dB
Phase Margin [deg]
Ambient Temperature [ºC]
CL=10pF
CL=10nF
CL=1nF


Phase Margin vs. Temperature
V+/V-=±15V, RL=10kΩ, VIN=-30dBm, Gv=20dB
Phase Margin [deg]
Ambient Temperature [ºC]
CL=10pF
CL=10nF
CL=1nF


Gain Margin vs. Load Capacitance
V+/V-=±6V, RL=10kΩ, VIN=-30dBm, Gv=20dB,
Gain Margin [dB]
Load Capacitance [F]
Ta=125℃
Ta=-40℃
Ta=25℃

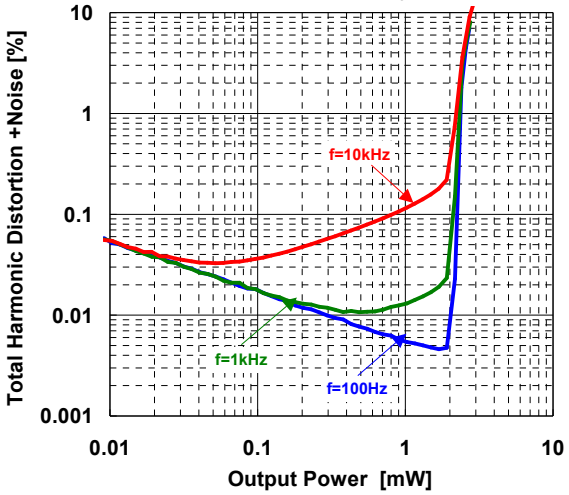

Gain Margin vs. Load Capacitance
V+/V-=±15V, RL=10kΩ, VIN=-30dBm, Gv=20dB
Gain Margin [dB]
Load Capacitance [F]
Ta=125℃
Ta=-40℃
Ta=25℃


Gain Margin vs.Temperature
V+/V-=±6V, RL=10kΩ, VIN=-30dBm, Gv=20dB
Gain Margin [dB]
Ambient Temperature [ºC]
CL=10pF
CL=1nF
CL=10nF


Gain Margin vs. Temperature
V+/V-=±15V, RL=10kΩ, VIN=-30dBm, Gv=20dB
Gain Margin [dB]
Ambient Temperature [ºC]
CL=10pF
CL=1nF
CL=10nF

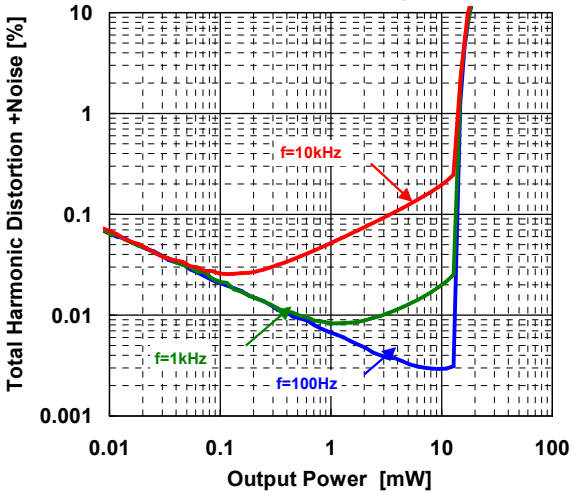
THD + Noise vs. Output Power

V^+/V^-=±6V, G_V=20dB, R_F=9.1kΩ, R_S=1kΩ, Ta=25°C



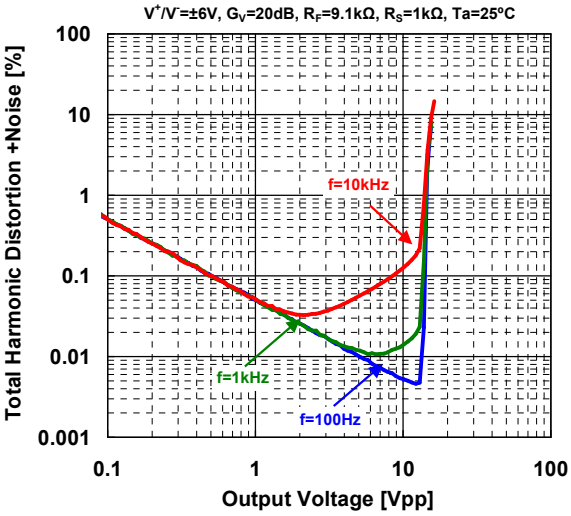
THD + Noise vs. Output Power

V^+/V^-=±15V, G_V=20dB, R_F=9.1kΩ, R_S=1kΩ, Ta=25°C



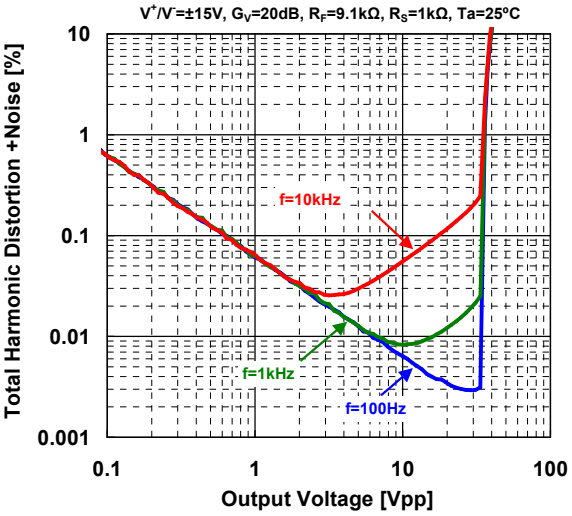
THD + Noise vs. Output Voltage

V^+/V^-=±6V, G_V=20dB, R_F=9.1kΩ, R_S=1kΩ, Ta=25°C



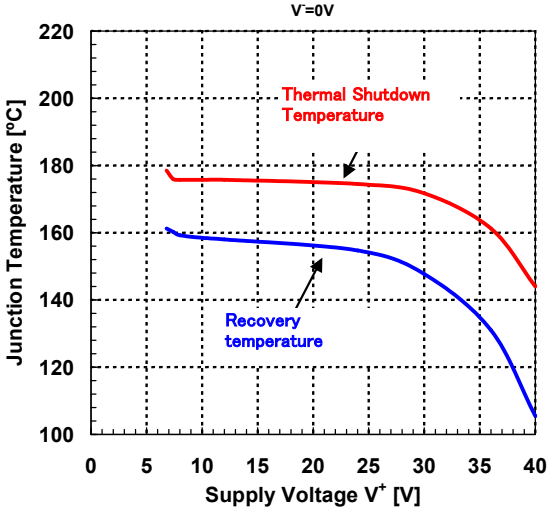
THD + Noise vs. Output Voltage

V^+/V^-=±15V, G_V=20dB, R_F=9.1kΩ, R_S=1kΩ, Ta=25°C



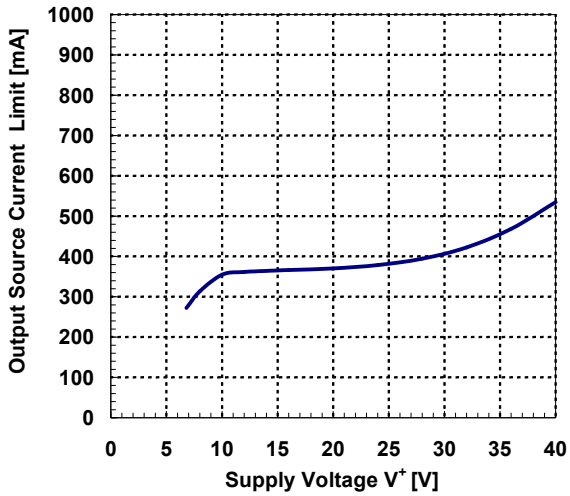
Thermal Shutdown Temperature vs. Supply Voltage

V^-=0V



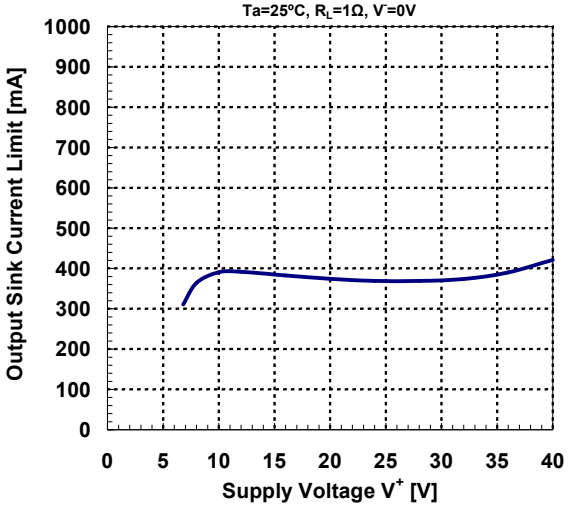
Output Source Current Limit vs. Supply Voltage

Ta=25ºC, R_L=1Ω,V^-=0V



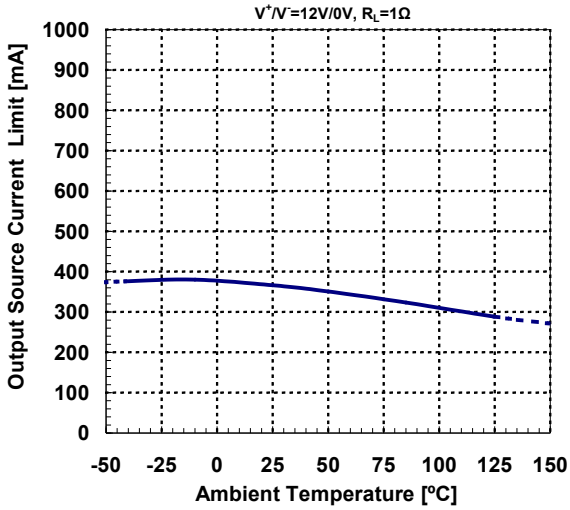
Output Sink Current Limit vs. Supply Voltage

Ta=25ºC, R_L=1Ω, V^-=0V



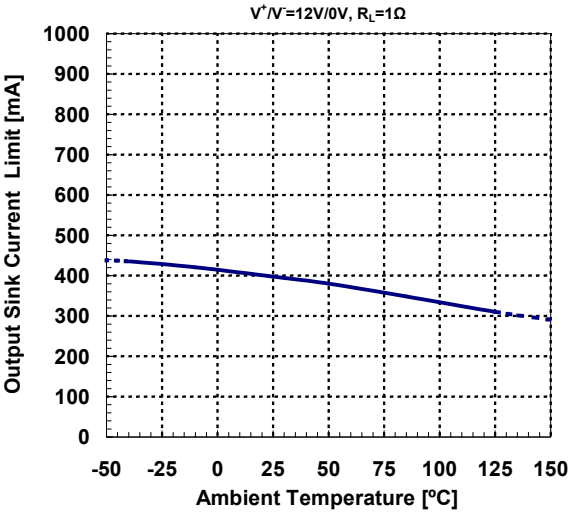
Output Source Current Limit vs. Temperature

V^+/V^-=12V/0V, R_L=1Ω



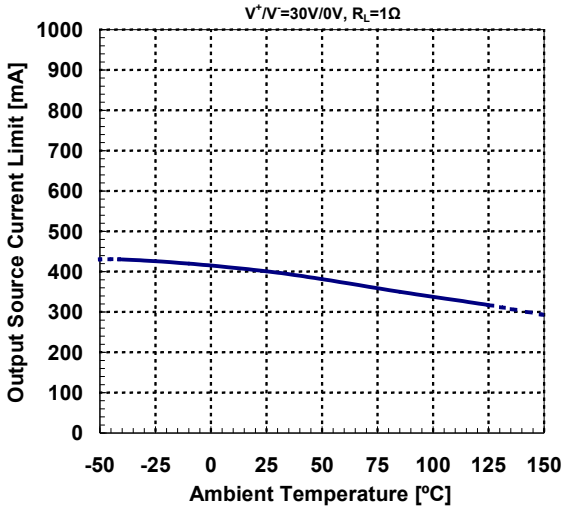
Output Sink Current Limit vs. Temperature

V^+/V^-=12V/0V, R_L=1Ω



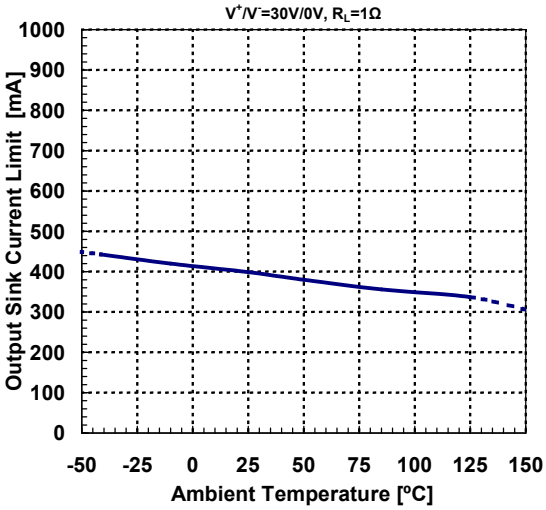
Output Source Current Limit vs. Temperature

V^+/V^-=30V/0V, R_L=1Ω



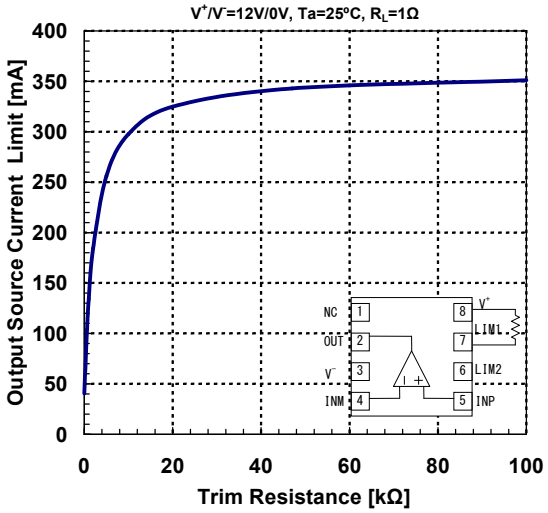
Output Sink Current Limit vs. Temperature

V^+/V^-=30V/0V, R_L=1Ω



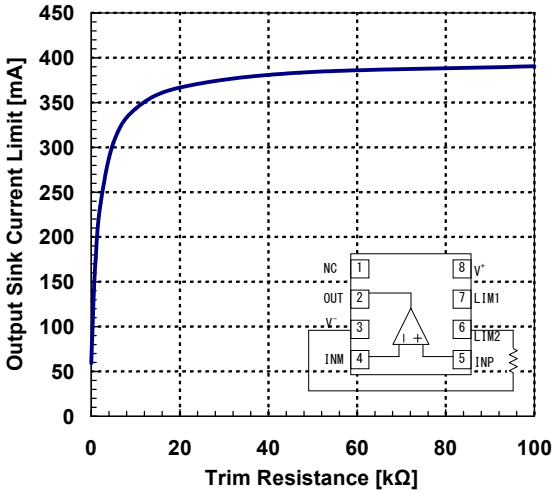
Output Source Current Limit vs. Current Limit Trim Resistance

V^+/V^-=12V/0V, Ta=25°C, R_L=1Ω



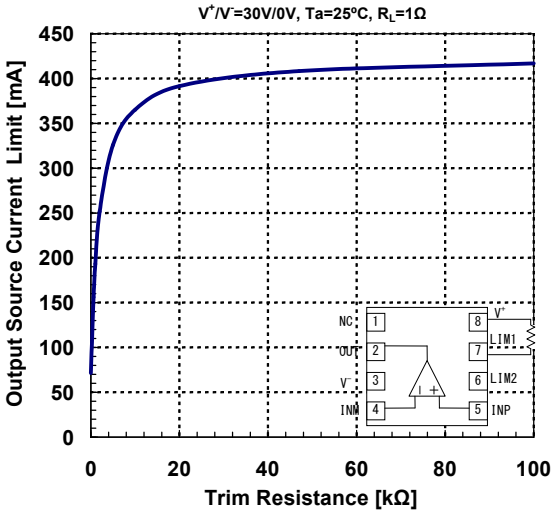
Output Sink Current Limit vs. Current Limit Trim Resistance

V^+/V^-=12V/0V, Ta=25°C, R_L=1Ω



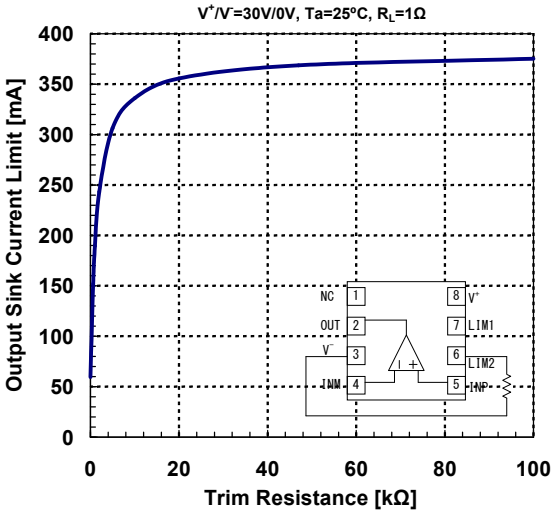
Output Source Current Limit vs. Current Limit Trim Resistance

V^+/V^-=30V/0V, Ta=25°C, R_L=1Ω



Output Sink Current Limit vs. Current Limit Trim Resistance

V^+/V^-=30V/0V, Ta=25°C, R_L=1Ω



■Application Note

The NJU77903 is CMOS operational amplifier that combines rail−to−rail input and output with operating up to 36V. It is able to output high current without the power booster. Therefore, the NJU77903 is suitable for the application requires high operating voltage and high output current.

This application note is one of effectual measures for understanding the dissipation power, thermal shutdown and behavior of current limit, to avoiding unexpected trebles. This application note consists of following matter.

1. Calculation of dissipation power
2. Thermal shutdown
3. Current limit
4. Resolver Excitation Circuit
5. Input Overvoltage Protection

This description does not assure the actual behavior. The performance of the NJU77903 should be conducted trials using actual equipment.

1. Calculation of dissipation power

The dissipation power is determined by the type of loads. It in case of resistance load and inductance load are shown respectively on this note. The symbols of supply voltage are defined as V_{DD} and V_{SS} instead of V^+ and V^-.

1.1 Calculation of dissipation power with resistance load

The dissipation power from the time 0 to π and it from π to 2π are calculated separately.

■ t=0 to π

Fig. 1.1 shows the internal current from 0 to π, Fig. 1.2 shows the Output current and the Output voltage from 0 to π. Io is the Output current and I_A is the current with the exception of the Output current. The dissipation power from 0 to π is expressed by the following equation.

$$P_{R1} = (V_{DD} - V_{SS})I_A + \frac{1}{\pi}\int_0^{\pi}(V_{DD} - V_O \sin\theta)I_O \sin\theta d\theta$$

$$= (V_{DD} - V_{SS})I_A + \frac{1}{\pi}\int_0^{\pi}(V_{DD} - V_O \sin\theta)\frac{V_O}{R}\sin\theta d\theta$$

$$= (V_{DD} - V_{SS})I_A + \frac{2V_{DD}V_O}{\pi R} - \frac{{V_O}^2}{2R}$$

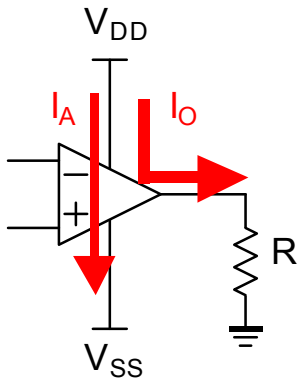


Fig. 1.1 the internal current from 0 to π

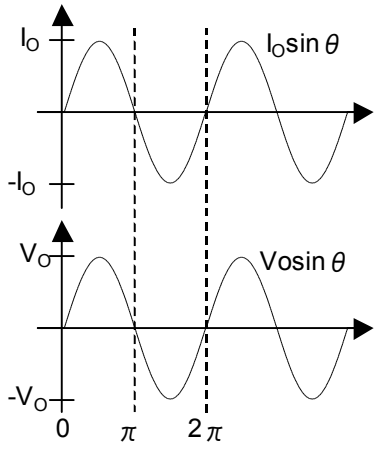


Fig. 1.2 the Output current and Voltage with resistance load

■ t=π to 2π

Fig. 1.3 shows the internal current from π to 2π, the dissipation power from π to 2π is expressed by the following equation.

$$P_{R2} = (V_{DD} - V_{SS})I_A + \frac{1}{\pi}\int_{\pi}^{2\pi}(V_O \sin\theta - V_{SS})I_O \sin\theta d\theta$$

$$= (V_{DD} - V_{SS})I_A + \frac{1}{\pi}\int_{\pi}^{2\pi}(V_O \sin\theta - V_{SS})\frac{V_O}{R}\sin\theta d\theta$$

$$= (V_{DD} - V_{SS})I_A - \frac{2V_{SS}V_O}{\pi R} - \frac{{V_O}^2}{2R}$$

In the case of $V_{DD} = -V_{SS}$, the internal loss P_R is the following result.

$$P_R = (V_{DD} - V_{SS})I_A + \frac{2V_{DD}V_O}{\pi R} - \frac{{V_O}^2}{2R}$$

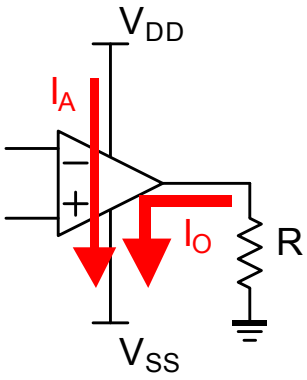


Fig. 1.3 the internal current from π to 2π

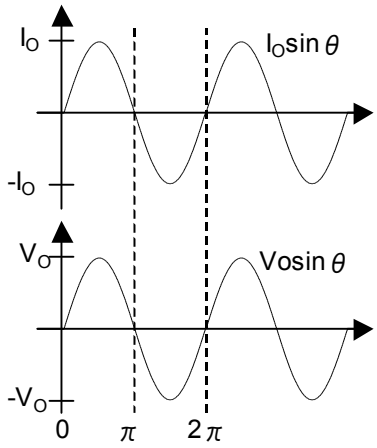


Fig.1.4 the Output current and Voltage with resistance

■ example for use

The dissipation power is calculated on the following condition.

Condition:

V_{DD}/V_{SS}= +6V/-6V

V_o=1Vpk

R=20Ω（Io=1Vpk/20Ω=50mApk=100mApp）

I_A=1.5mA

$$P_R = (V_{DD} - V_{SS})I_A + \frac{2V_{DD}V_O}{\pi R} - \frac{{V_O}^2}{2R}$$

$$= (6V + 6V)\times 1.5mA + \frac{2\times 6V\times 1V}{\pi\times 20\Omega} - \frac{(1V)^2}{2\times 20\Omega} = 184mW$$

On the single power supply operation (V_{DD}/V_{SS}= +12V/0V) with the load resistance(R=20Ωwhich is the middle point Voltage), the dissipation power is 187 mW. It is same as previous one.

1.2 Calculation of dissipation power with inductance load

The dissipation power from the time 0 to π and it from π to 2π are calculated separately.

■t=0 to π

Fig. 1.5 shows the internal current from 0 to π and Fig. 1.7 shows the Output current and the Output Voltage from 0 to π. Since it is an inductance load, the Output Current and the Output Voltage make 90-degree phase difference. Io is the Output Current and I_A is the current with the exception of the output current.

The loss by output current from 0 to π is expressed by the following equation.

$$P_{LO1} = (V_{DD} - V_O \cos\theta) I_O \sin\theta = V_{DD} I_O \sin\theta - \frac{1}{2} V_O I_O \sin 2\theta$$

The loss by output current from 0 to π is expressed by the following equation.

$$P_{L1} = (V_{DD} - V_{SS}) I_A + \frac{1}{\pi}\int_0^{\pi} V_{DD} I_O \sin\theta d\theta - \frac{1}{\pi}\int_0^{\pi} \frac{1}{2} V_O I_O \sin 2\theta d\theta$$

$$= (V_{DD} - V_{SS}) I_A + \frac{2 V_{DD} I_O}{\pi}$$

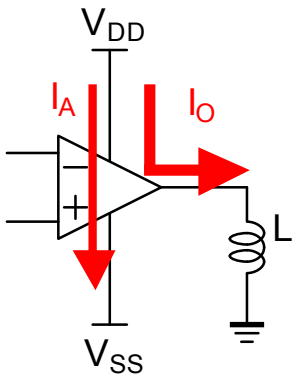


Fig. 1.5 the internal current from 0 to π

■t=π to 2π

Fig. 1.6 shows the internal current from π to 2π.The loss by output current from π to 2π is expressed by the following equation.

$$P_{LO2} = (V_O \cos\theta - V_{SS}) I_O \sin\theta = -V_{ee} I_O \sin\theta + \frac{1}{2} V_O I_O \sin 2\theta$$

The Dissipation power from π to 2π is expressed by the following equation.

$$P_{L2} = (V_{DD} - V_{SS}) I_A + \frac{1}{\pi}\int_{\pi}^{2\pi} -V_{ee} I_O \sin\theta d\theta + \frac{1}{\pi}\int_{\pi}^{2\pi} \frac{1}{2} V_O I_O \sin 2\theta d\theta = (V_{DD} - V_{SS}) I_A - \frac{2 V_{SS} I_O}{\pi}$$

In the case of V_{DD}=-V_{SS}, the dissipation power is the following result.

$$P_L = (V_{DD} - V_{SS}) I_A + \frac{2 V_{DD} I_O}{\pi}$$

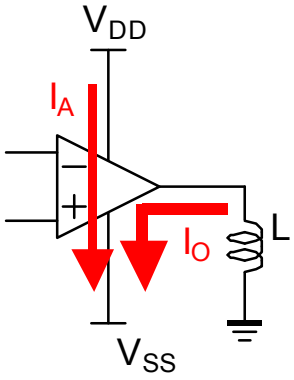


Fig.1.6 the internal current from π to 2π.

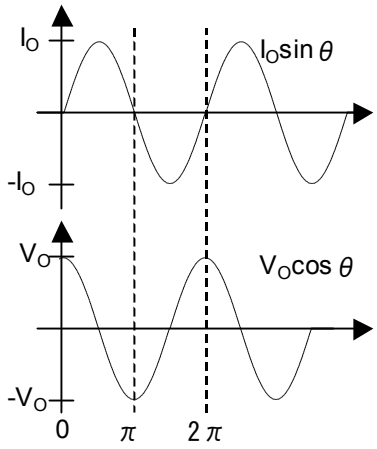


Fig.1.7 the Output current and Output Voltage with inductance load

■ example for use

The dissipation power is calculated on the following condition.

Condition:

V_{DD}/V_{SS}= +6V/-6V

I_o=50mApk(100mApp)

I_A=1.5mA

$$P_L = (V_{DD} - V_{SS})I_A + \frac{2V_{DD}I_O}{\pi} = (6V + 6V) \times 1.5mA + \frac{2 \times 6V \times 50mA}{\pi} = 209mW$$

On the Single power supply operation whose equivalent circuit is Fig1.8, the dissipation power is as follows.

Condition:

V_{DD}/V_{SS}= +12V/0V

I_o=50mApk(100mApp)

I_A=1.5mA

$$P_L = (V_{DD} - V_{SS})I_A + \frac{2V_{DD}I_O}{\pi} = (6V + 6V) \times 1.5mA + \frac{2 \times (12V/2) \times 50mA}{\pi} = 209mW$$

Fig1.9 is the supply-voltage dependency of the dissipation power on inductance load. The NJU77903 should be operated in lower than package power (P_D).

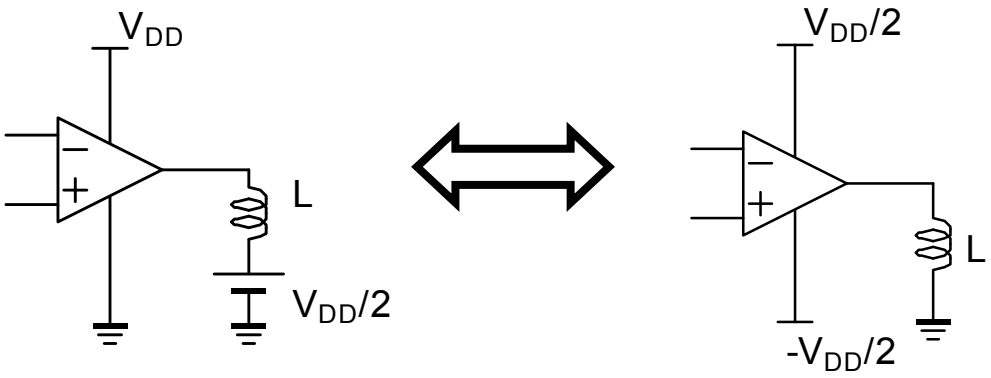


Fig1.8. Equivalent circuit (Single Supply

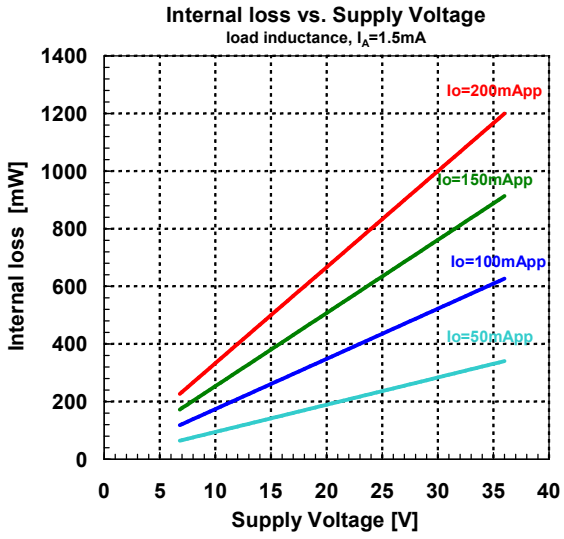


Fig1.9 the supply-voltage dependency of the dissipation power by inductance load. (Single−Supply)

1.3 the current with the exception of the Output current

Fig1.10 shows the Evaluation circuit of the current with the exception of the Output current. This result shows Fig1.11 and Fig1.12.

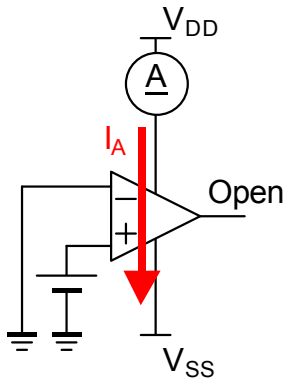


Fig1.10 the current with the exception of the Output current

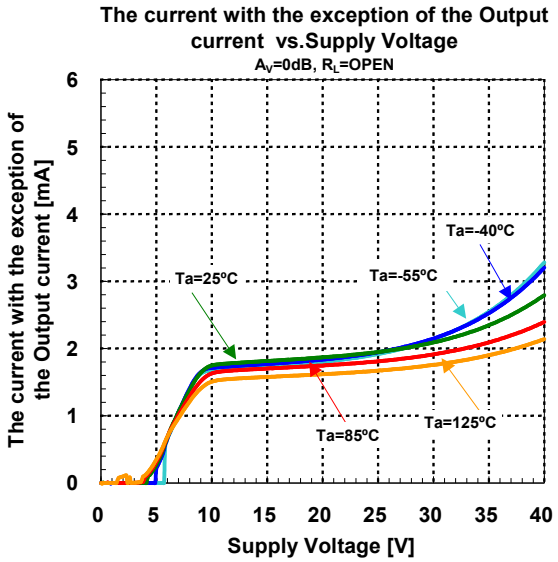


Fig1.11 the current with the exception of the Output current vs. Supply Voltage

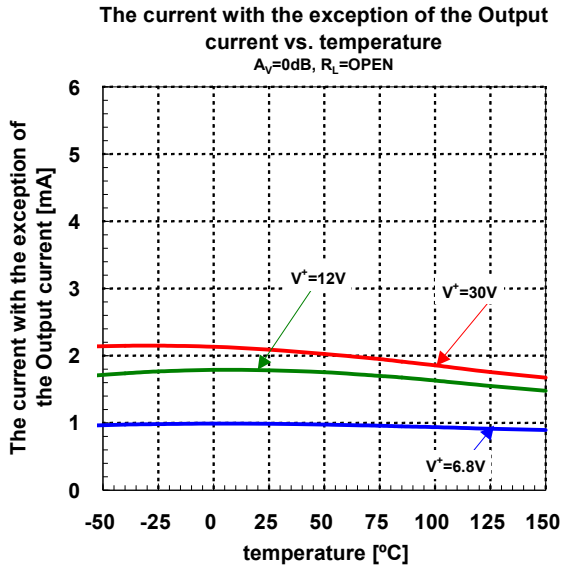


Fig1.12 the current with the exception of the Output current vs. temperature

2. Thermal Shutdown

The NJU77903 has thermal shutdown (TSD) function in case that dissipation power exceeds Package Power P_D. Fig 2.1 shows Thermal Shutdown Temperature vs. Supply Voltage. When the junction temperature exceeds the shutdown temperature approximately 175°C on the Supply Voltage 12V, the TSD function operates and disables the output current. Under the TSD operation, the output terminal is regarded as high impedance terminal. If the output voltage is necessarily GND Voltage, the output terminal should be connected to GND via resistance.

When the junction temperature cools to recovery temperature approximately 160°C on the Supply Voltage 12V, the NJU77903 automatically recover from the TSD operation and output current is re-enabled.

The TSD function is not intended to replace proper heat sinking. The NJU77903 should be operated in lower than 150°C the maximum junction temperature.

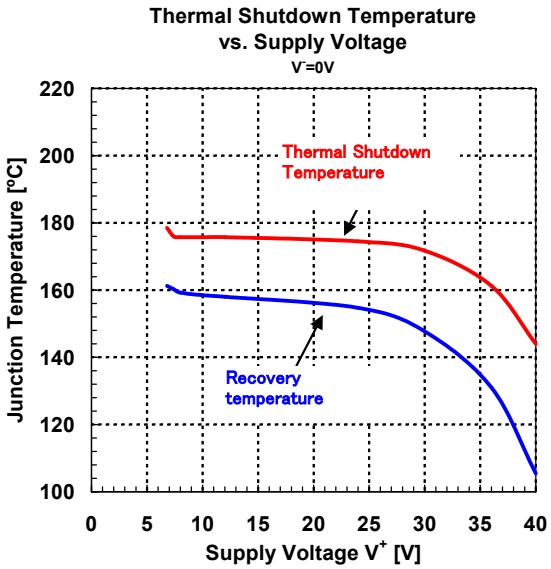


Fig 2.1 Thermal Shutdown Temperature vs. Supply Voltage

3. Current Limit

The NJU77903 is designed with internal current limit in case of overload condition. Fig. 3.1 shows the Output Source Current Limit vs. temperature and Fig. 3.2 shows the Output Sink Current Limit vs. temperature respectively. With the increasing in temperature, the limits are reduced.

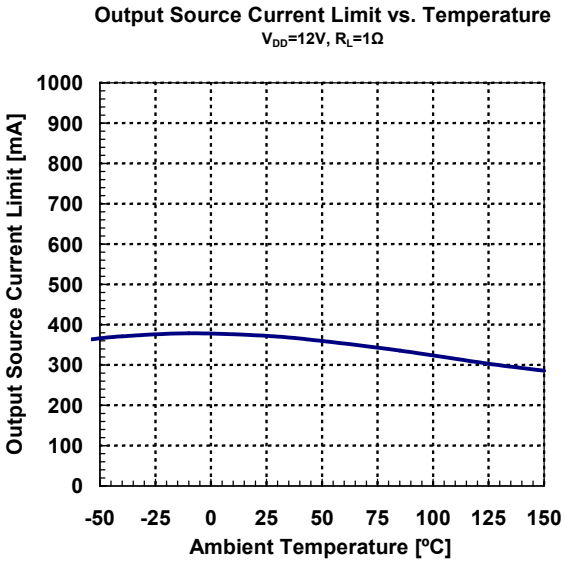


Fig3.1 Output Source Current Limit vs. temperature

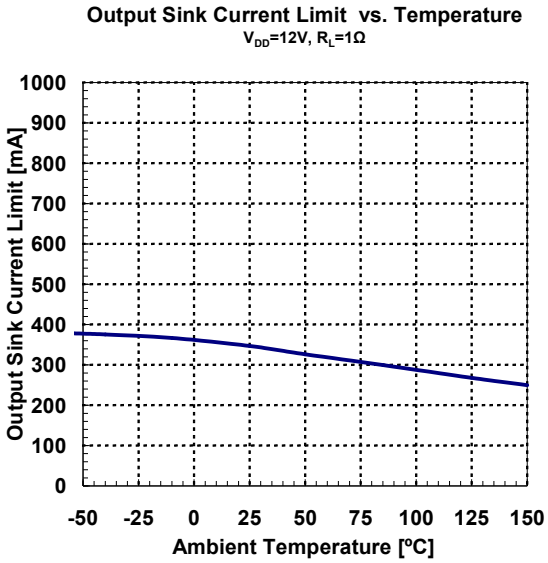


Fig3.2 Output Sink Current Limit vs. temperature

Fig. 3.3 shows Output Source Current vs. time. Output Source Current Limit decreases gradually since junction temperature rises. The output current is temporarily disabled due to TSD operation in Ta=160°C line of Fig. 3.3 (time = 55msec to 75msec). When the junction temperature falls, the output current is automatically recovered (time = 75msec). In order to prevent from damage the NJU77903 should be running under maximum junction temperature.

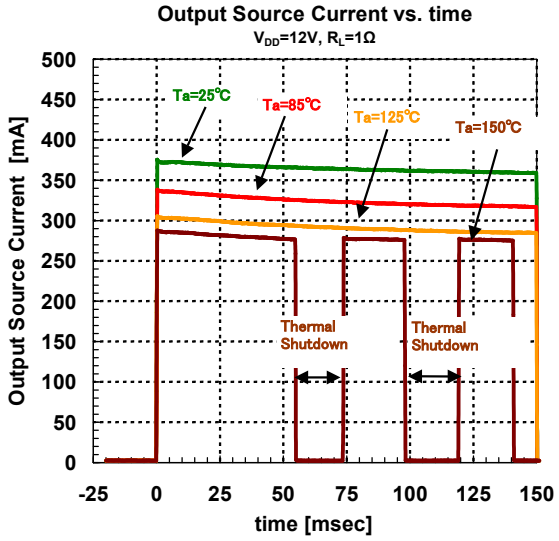


Fig3.3 Output Source Current Limit vs. Time

4. Resolver Excitation Circuit

Fig4.1 shows the Typical Resolver Excitation Circuit using the NJU77903 and the NJM2904. The NJM2904 (A) makes midpoint voltage and the NJM2904 (B) makes signal phase inversion. Fig4.2 is the circuit without NJM2904 (A), its dominant voltage is given by resistance voltage divider. Fig4.3 is the circuit omitted NJM2904 (A) and NJM2904 (B), it is available under the condition using the input signals which have phase difference one another.

Fig 4.4 shows output voltage and current. The output voltage (Vout) is the voltage drop on the inductance load, the output current (Iout) is defined as positive side according Fig 4.4. The inductance load makes phase difference between Vout and Iout. However, it is not just 90° because of internal resistance on inductance. The performance of resolver excitation should be conducted trials using actual equipment.

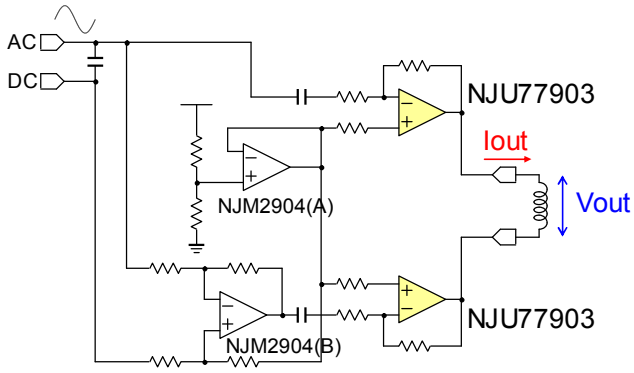


Fig4.1 Resolver Excitation Circuit

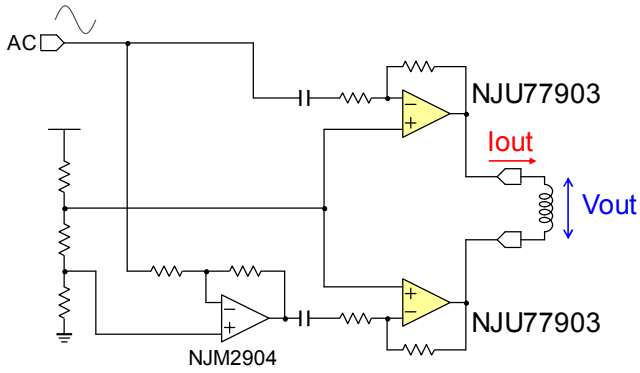


Fig4.2 Resolver Excitation Circuit
（This version omitted NJM2904(A)）

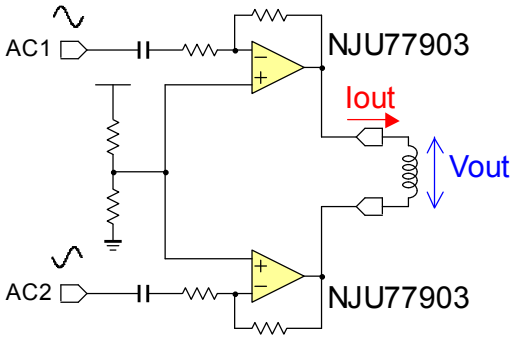


Fig4.3 Resolver Excitation Circuit
（This version omitted NJM2904）

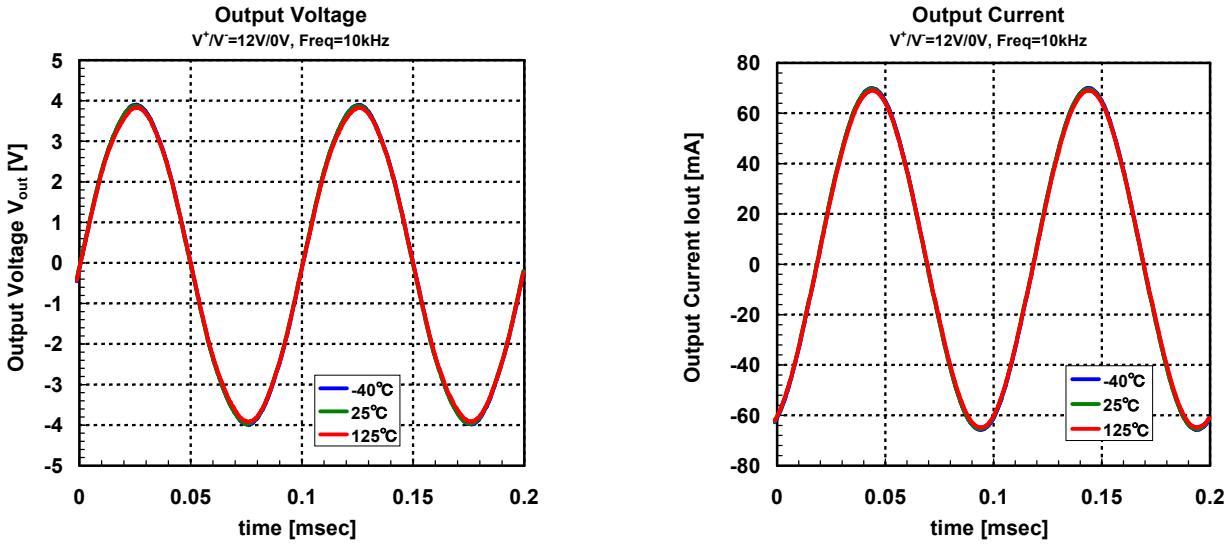
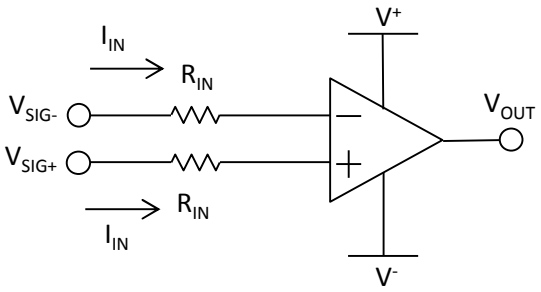


Fig 4.4 Output Voltage and Output Current of Resolver Excitation Circuit

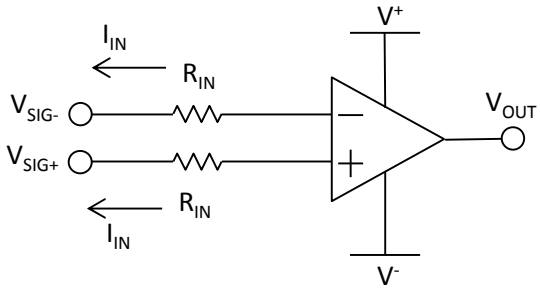
5. Input Overvoltage Protection

If the input voltage exceeds the supply rail, You must use a limiting resistor as shown in Fig5.1, because you must be limited to less than the input current of absolute maximum ratings. Resistance value of the current limiting and can be calculated by the following equation.



$$I_{IN} = \frac{V_{SIG} - V^+}{R_{IN}} \leqq 10mA, (V_{SIG} \geqq V^+)$$

Fig5.1a Input Overvoltage ($V_{SIG} \geqq V^+$)

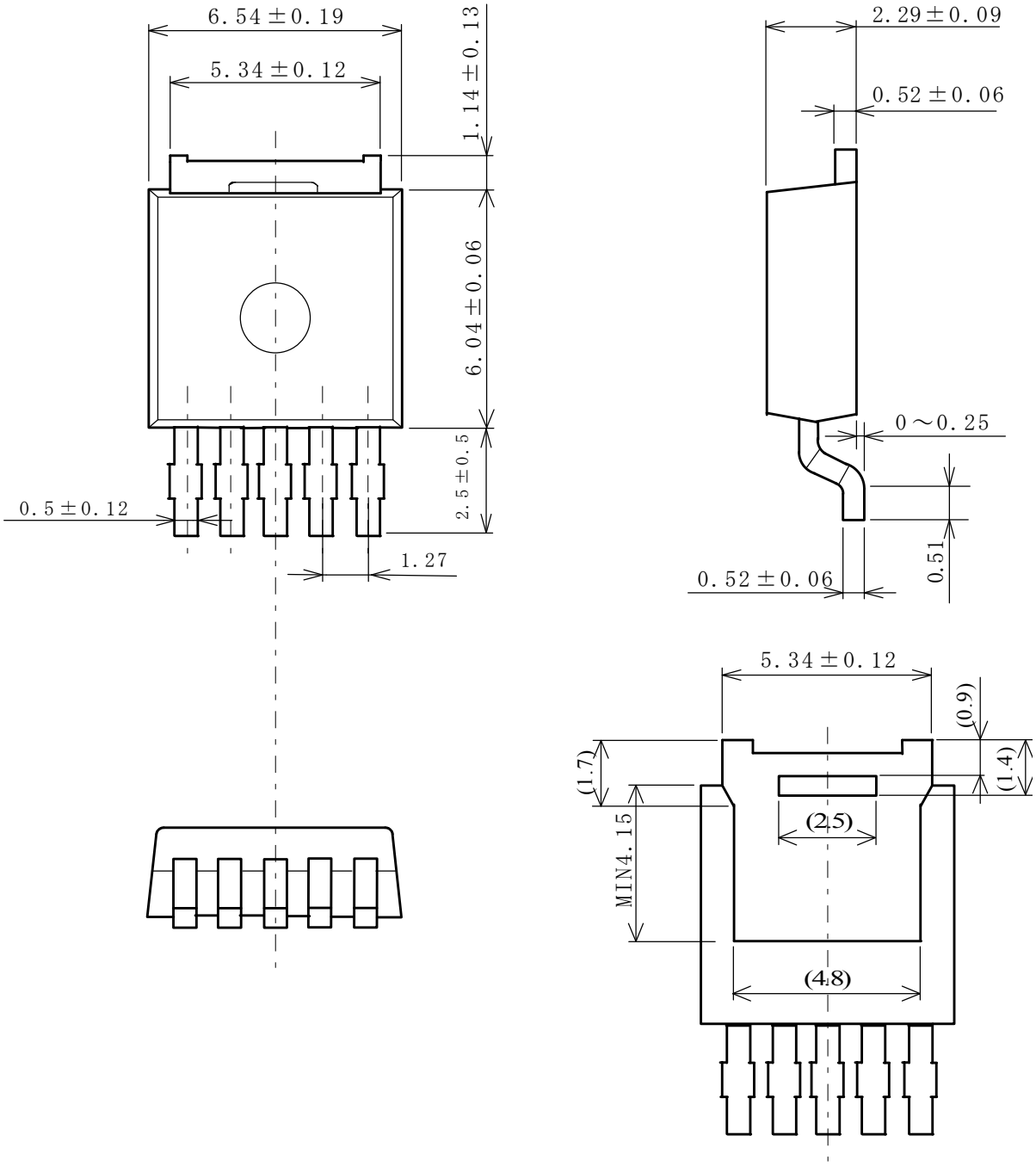


$$I_{IN} = \frac{V^- - V_{SIG}}{R_{IN}} \leqq 10mA, (V_{SIG} \leqq V^-)$$

Fig5.1b Input Overvoltage ($V_{SIG} \leqq V^-$)

TO252-5

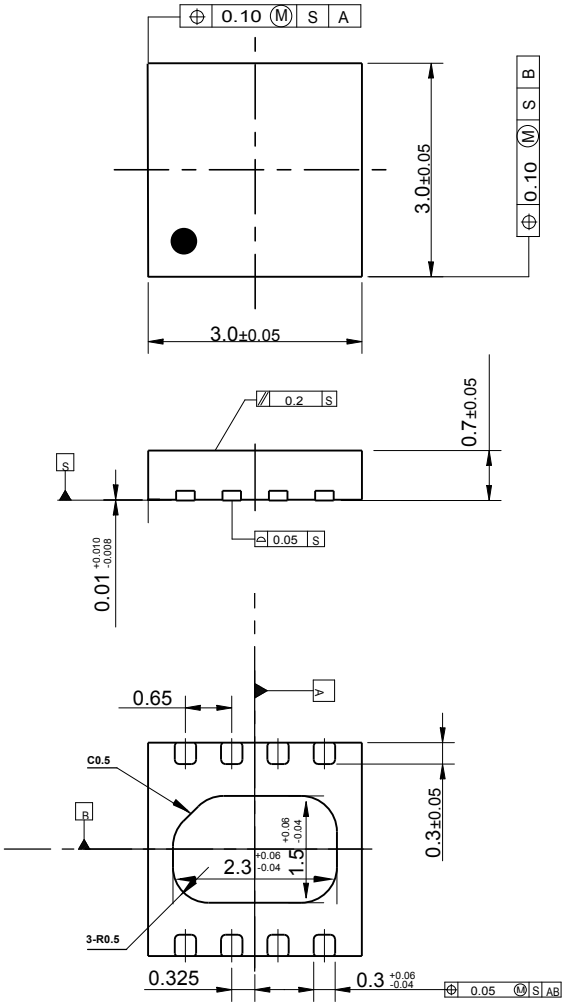
■ **PACKAGE DIMENSIONS**



Unit : mm

DFN8-W2 (ESON8-W2)

■ PACKAGE DIMENSIONS



Unit : mm