ALPHA & OMEGA SEMICONDUCTOR

# AON7403

## 30V P-Channel MOSFET

### General Description

The AON7403 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications.

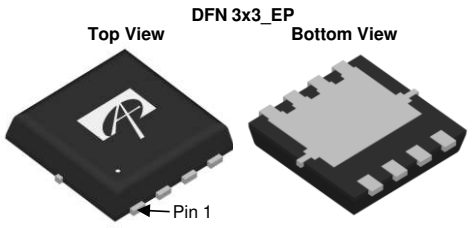
### Product Summary

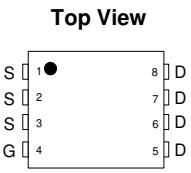
| | |
|---|---|
| $V_{DS}$ | -30V |
| $I_D$ (at $V_{GS}$=-10V) | -29A |
| $R_{DS(ON)}$ (at $V_{GS}$=-10V) | < 18mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$=-5V) | < 36mΩ |

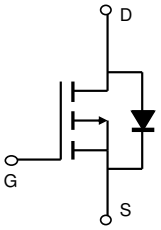
100% UIS Tested

Green Product

DFN 3x3_EP




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±25 | V |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | -29 | A |
| | $T_C$=100°C | | -18 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | -80 | |
| Continuous Drain Current | $T_A$=25°C | $I_{DSM}$ | -11 | A |
| | $T_A$=70°C | | -8.5 | |
| Avalanche Current [C] | | $I_{AR}$ | 24 | A |
| Repetitive avalanche energy L=0.1mH [C] | | $E_{AR}$ | 29 | mJ |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 25 | W |
| | $T_C$=100°C | | 10 | |
| Power Dissipation [A] | $T_A$=25°C | $P_{DSM}$ | 4.1 | W |
| | $T_A$=70°C | | 2.6 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 22 | 30 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 47 | 60 | °C/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JC}$ | 4.2 | 5 | °C/W |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=-250µA, $V_{GS}$=0V | -30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-30V, $V_{GS}$=0V | | | -1 | µA |
| | | $T_J$=55°C | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±25V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=-250µA | -1.7 | -2.2 | -3 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=-10V, $V_{DS}$=-5V | -80 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-10V, $I_D$=-8A | | 14 | 18 | mΩ |
| | | $T_J$=125°C | | 20 | 25 | |
| | | $V_{GS}$=-5V, $I_D$=-5A | | 26 | 36 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-8A | | 20 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A,$V_{GS}$=0V | | -0.7 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | -22 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-15V, f=1MHz | | 1130 | 1400 | pF |
| $C_{oss}$ | Output Capacitance | | | 240 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 155 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 5.8 | 8 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=-10V, $V_{DS}$=-15V, $I_D$=-8A | | 18 | 24 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 5.5 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 3.3 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=-10V, $V_{DS}$=-15V, $R_L$=1.8Ω, $R_{GEN}$=3Ω | | 8.7 | | ns |
| $t_r$ | Turn-On Rise Time | | | 8.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 18 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 7 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-8A, dI/dt=500A/µs | | 12 | 16 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-8A, dI/dt=500A/µs | | 26 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

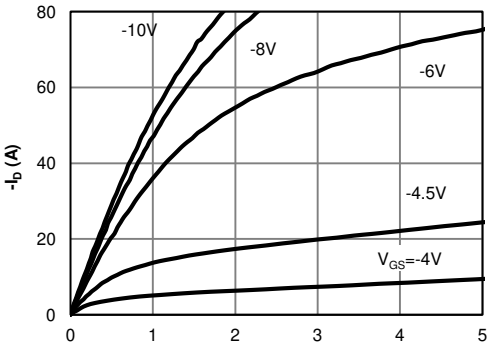



**Fig 1: On-Region Characteristics (Note E)**

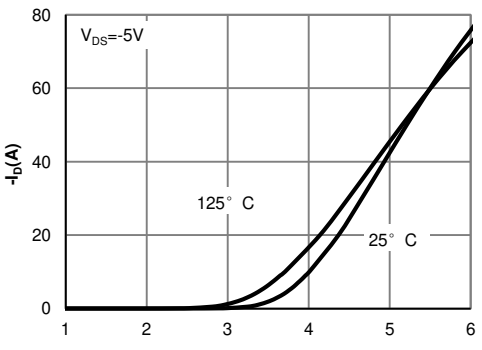



**Figure 2: Transfer Characteristics (Note E)**

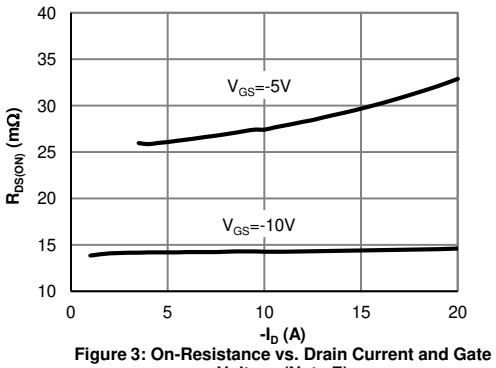



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

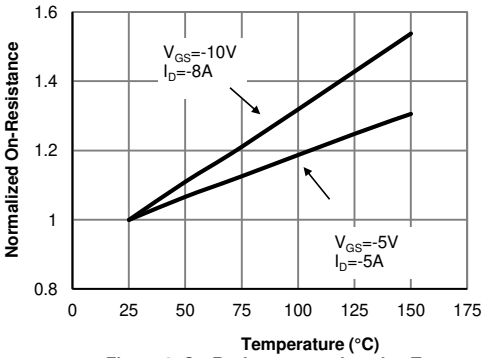



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

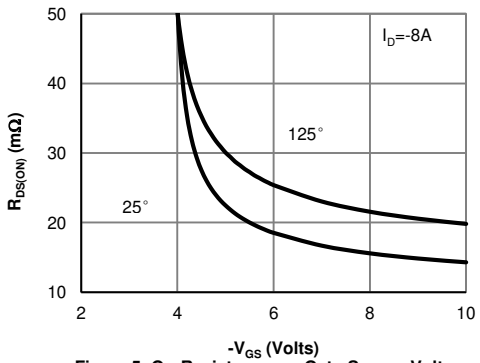



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

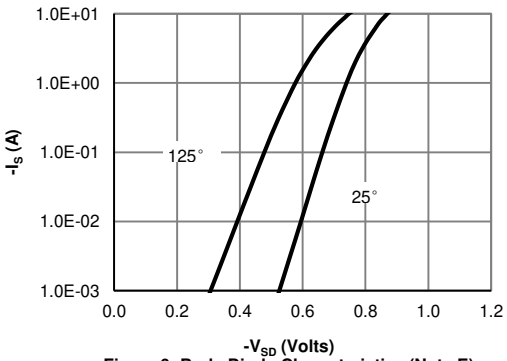



**Figure 6: Body-Diode Characteristics (Note E)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

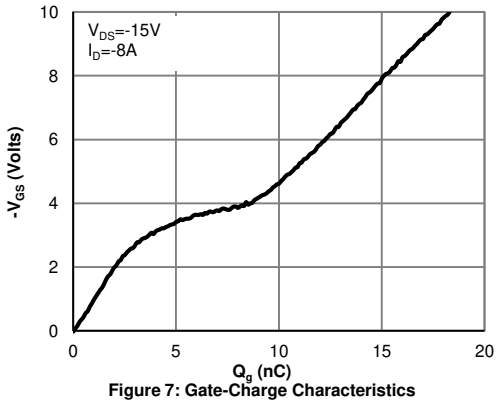



**Figure 7: Gate-Charge Characteristics**

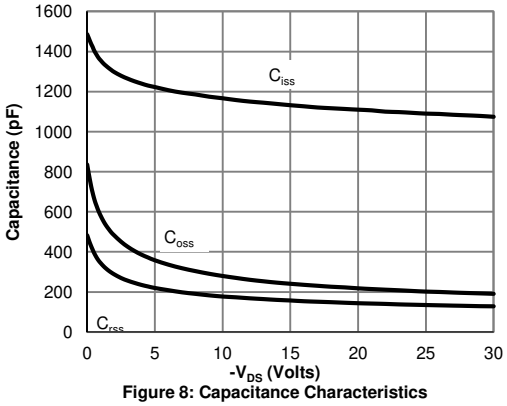



**Figure 8: Capacitance Characteristics**

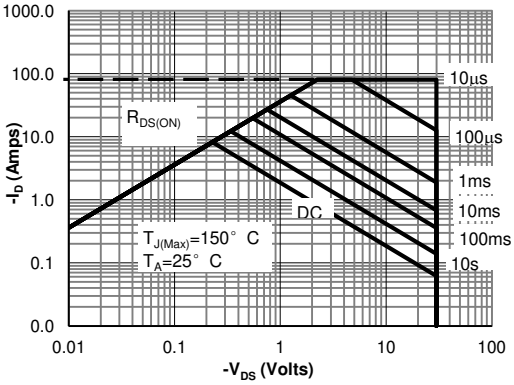



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

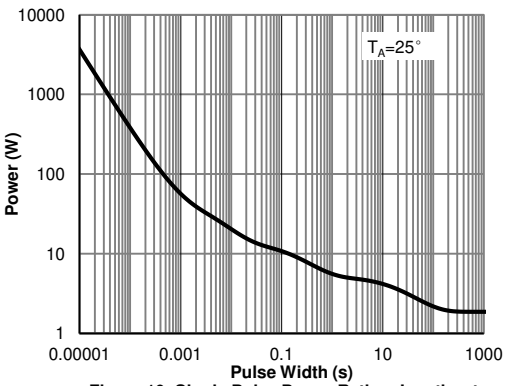



**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

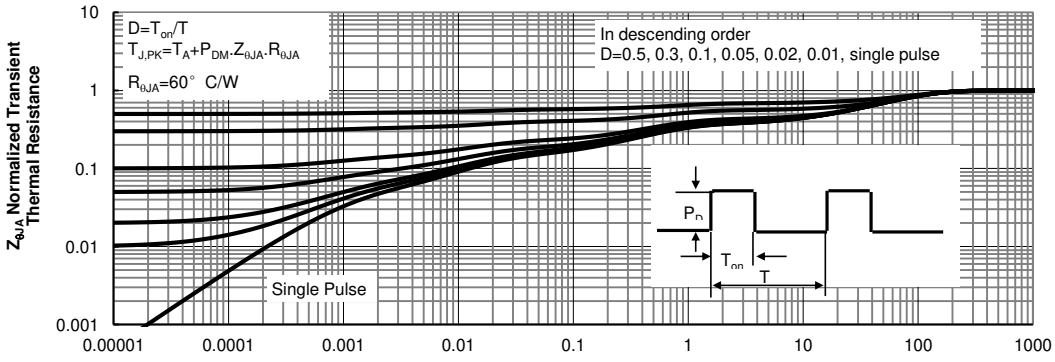
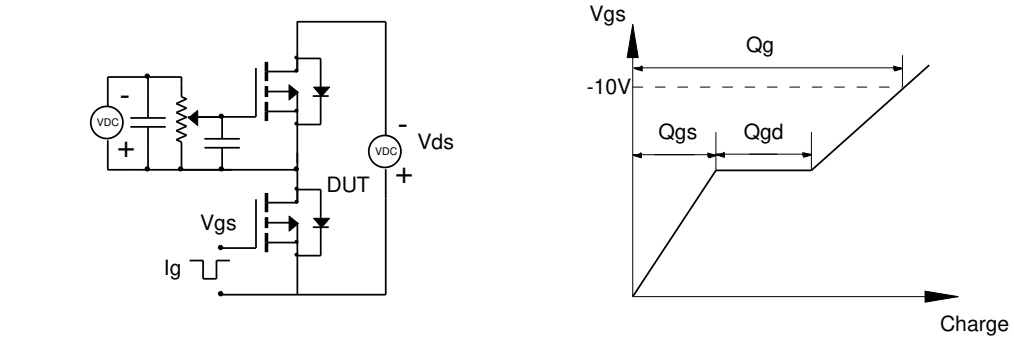
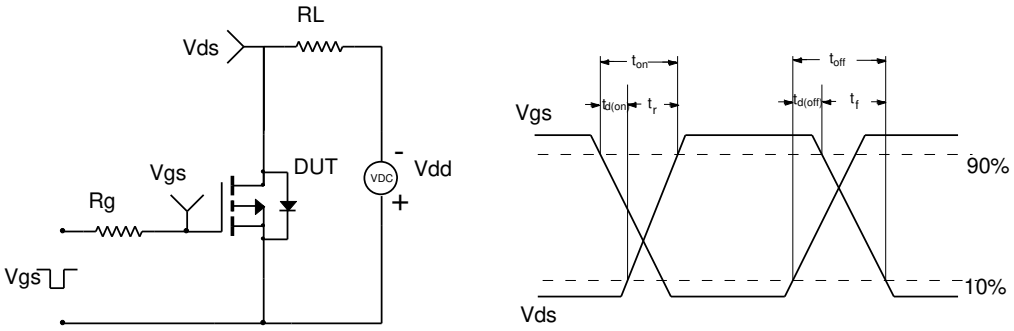



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

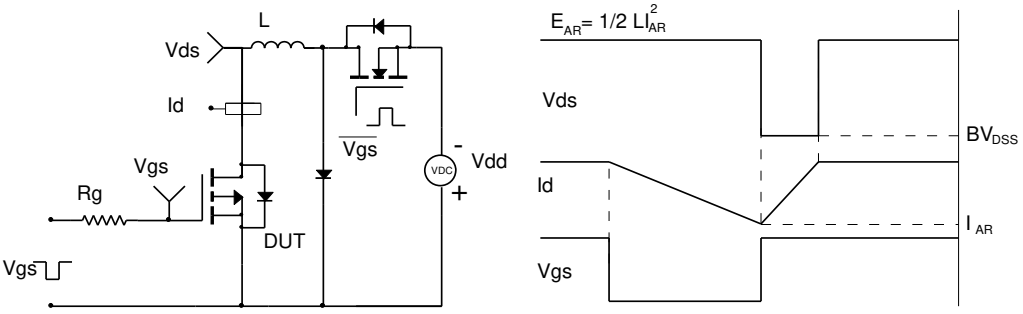
## Gate Charge Test Circuit & Waveform




## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms