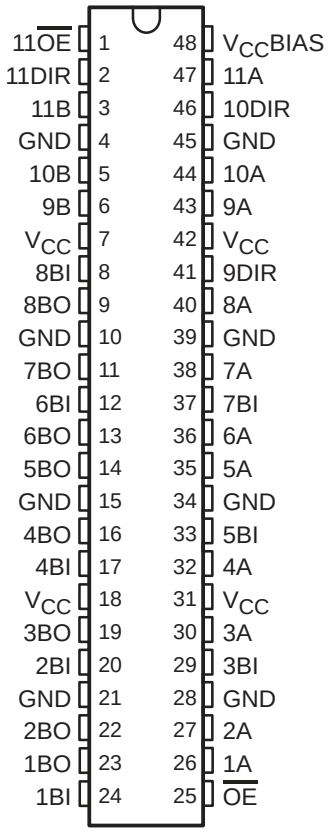
- **Member of the Texas Instruments Widebus™ Family**
- **Supports the VME64 ETL Specification**
- **Reduced TTL-Compatible Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support Equivalent 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Equivalent 25-Ω Series Damping Resistor on B Port**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The SN74ABTE16246 is an 11-bit noninverting transceiver designed for asynchronous two-way communication between buses. This device has open-collector and 3-state outputs. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has an equivalent 25-Ω series output resistor to reduce ringing. Active bus-hold inputs on the B port hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ABTE16246DL	ABTE16246
		Tape and reel	SN74ABTE16246DLR	
	TSSOP – DGG	Tape and reel	SN74ABTE16246DGGR	ABTE16246

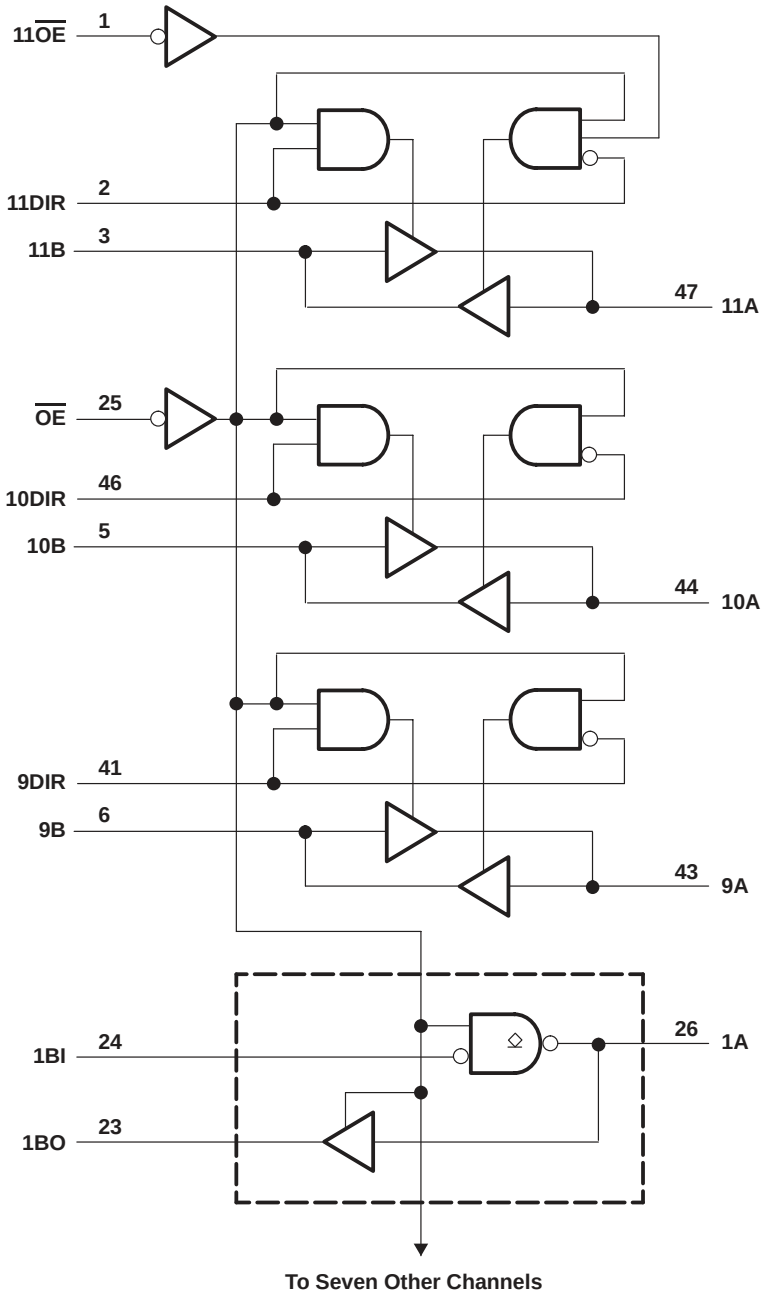
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS					OPERATION
$\overline{OE}$	9DIR	10DIR	11DIR	11$\overline{OE}$	
H	X	X	X	X	Isolation
L	X	X	X	X	1BI–8BI data to 1A–8A bus (OC†), 1A–8A data to 1BO–8BO bus
L	L	X	X	X	9A data to 9B bus
L	H	X	X	X	9B data to 9A bus
L	X	L	X	X	10A data to 10B bus
L	X	H	X	X	10B data to 10A bus
L	X	X	L	L	11A data to 11B bus
L	X	X	L	H	11A, 11B isolation
L	X	X	H	X	11B data to 11A bus

† OC = Open-collector outputs

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and V_{CC}BIAS . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 70°C/W
DL package . . . . . 63°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}, V_{CC}BIAS	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			V
		Except $\overline{OE}$	1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8	V
		Except $\overline{OE}$			1.4	
V_{OH}	High-level output voltage	1A–8A	0		5.5	V
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	B bus			–12	mA
		9A–11A			–64	
I_{OL}	Low-level output current	B bus			12	mA
		A bus			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = –100 µA			V_{CC}–0.2	V
		V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4			
			I_{OH} = –12 mA	2			
	9A–11A	V_{CC} = 5.5 V,	I_{OH} = –1 mA			4.5	
		V_{CC} = 4.5 V	I_{OH} = –32 mA	2.4			
			I_{OH} = –64 mA	2			
I_{OH}	1A–8A	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			20	µA
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA			0.4	V
			I_{OL} = 12 mA			0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA			0.55	
			I_{OL} = 90 mA			0.9	
V_{hys}					100		mV
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V	100			µA
			V_I = 2 V	–100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V			±500	
I_I	Control inputs	V_{CC} = 5.5 V	V_I = V_{CC} or GND			±1	µA
	A or B ports	V_{CC} = 5.5 V, $\overline{OE}$ = V_{CC}				±20	
I_{OZH}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 2.7 V			10	µA
I_{OZL}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 0.5 V			–10	µA
I_O	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–50		–180	mA
	B port			–25		–90	
I_{off}		V_{CC} = 0, V_I or V_O ≤ 4.5 V,	V_{CC}BIAS = 0			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		28	36	mA
			Outputs low		38	48	
			Outputs disabled		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V, C_L = 50 pF	$\overline{OE}$ high		0.02		mA/ MHz
			$\overline{OE}$ low		0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V			2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V			4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V,	V_{CC}BIAS = 4.5 V to 5.5 V,	$I_{O(DC)}$ = 0		250	700	μA
		V_{CC} = 4.5 V to 5.5 V‡,	V_{CC}BIAS = 4.5 V to 5.5 V,	$I_{O(DC)}$ = 0			20	
V_O	A port	V_{CC} = 0	V_{CC}BIAS = 4.5 V to 5.5 V		1.1	1.5	1.9	V
			V_{CC}BIAS = 4.75 V to 5.25 V		1.3	1.5	1.7	
I_O	A port	V_{CC} = 0,	V_{CC}BIAS = 4.5 V	V_O = 0	–20		–100	μA
				V_O = 3 V	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	B	1.5	3.1	4.2	1.5	5.2	ns
t_{PHL}			1.5	3.5	4.6	1.5	5.2	
t_{PLH}	9B–11B	9A–11A	1.5	3	3.8	1.5	4.5	ns
t_{PHL}			1.5	3.2	4	1.5	4.5	
t_{PLH}§	1B–8B	1A–8A	1.5	3.2	4	1.5	4.5	ns
t_{PLH}¶			7.5	8.9	9.7	7.5	10.3	
t_{PHL}			1.5	3.2	4	1.5	4.5	
t_{PZH}	$\overline{OE}$	9A–11A	2	4.3	5.3	2	6.2	ns
t_{PZL}		1A–11A	2	4.4	5.4	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.3	6	2	7.1	ns
t_{PZL}			2	4.5	6.4	2	7.3	
t_{PHZ}	$\overline{OE}$	9A–11A	2	4.2	5.9	2	6.7	ns
t_{PLZ}		1A–11A	2	3.5	4.6	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2.5	4.3	6.2	2.5	7	ns
t_{PLZ}			2	3.6	5	2	5.5	

§ Measurement point is V_{OL} + 0.3 V.
¶ Measurement point is V_{OL} + 1.5 V.

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

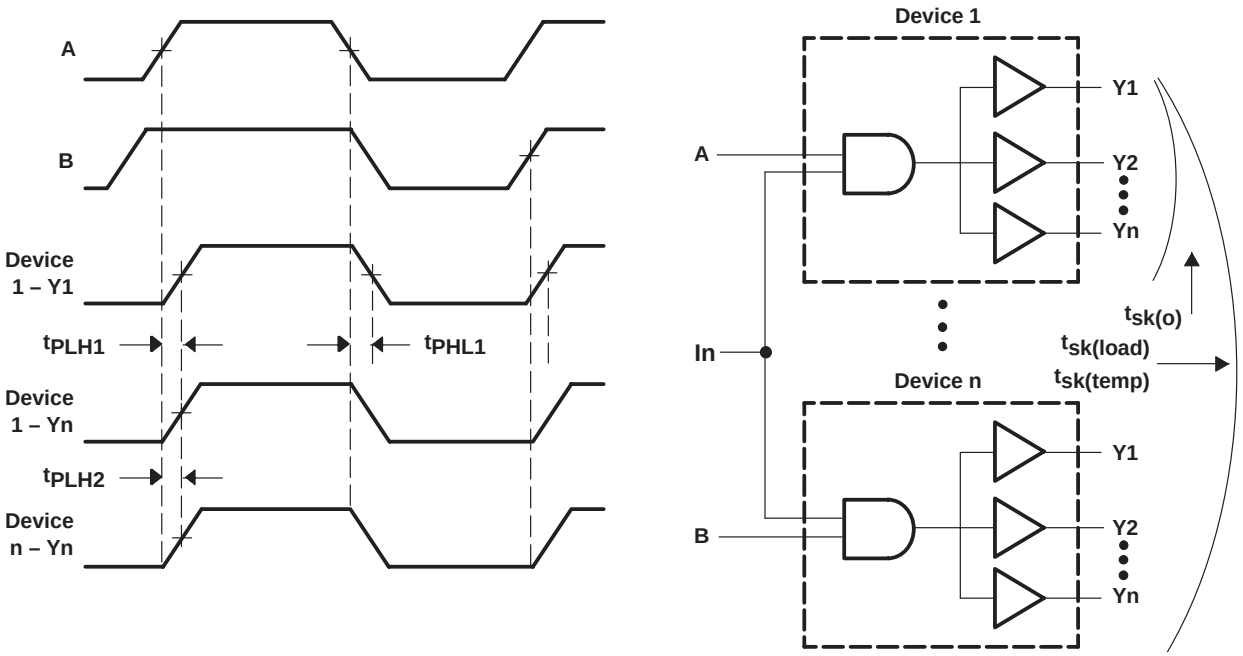
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	9B–11B	9A–11A	R_X = 13 Ω	1.5	3.2	4	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.6	
t_{PHL}	1B–8B	1A–8A	R_X = 13 Ω	1.5	3.3	4.2	1.5	4.8	ns
t_{PLH}	9B–11B	9A–11A	R_X = 26 Ω	1.5	3.1	4	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	4.9	
t_{PHL}	1B–8B	1A–8A	R_X = 26 Ω	1.5	3.1	4	1.5	4.4	ns
t_{PLH}	9B–11B	1A–8A	R_X = 56 Ω	1.5	3	3.8	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	4.7	
t_{PHL}	1B–8B	1A–8A	R_X = 56 Ω	1.5	3	4	1.5	4.4	ns
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2	ns
	A	B	R_X = Open		0.4	0.8		2	
	B	A	R_X = 26 Ω		0.3	0.8		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3	ns
	A	B	R_X = Open		0.7	1.1		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	ns
t_t‡	A	B	R_X = Open	3.5	5.5	7.3	3.5	7.9	ns

† t_t is measured between 1 V and 2 V of the output waveform.
‡ t_t is measured between 10% and 90% of the output waveform.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	MIN	MAX	UNIT
$t_{sk(temp)}$	A	B	V_{CC} = constant, ΔT_A = 20°C			2.5	ns
	B	A		R_X = 56 Ω		4	
$t_{sk(load)}$	B	A	V_{CC} = constant, Temperature = constant	R_X = 13, 26, or 56 Ω		4	ns

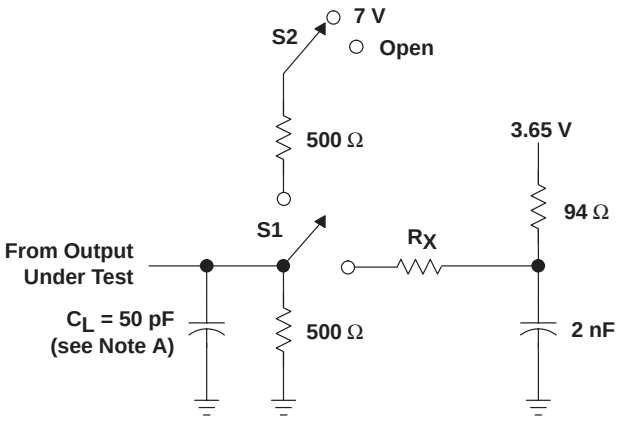
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation-delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of any two outputs of the same device switching in the same direction (e.g., $|t_{PLH1} - t_{PLH2}|$) .
C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of $V_{CC} \pm 1\%$ and with package temperature differences of 20°C.
D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

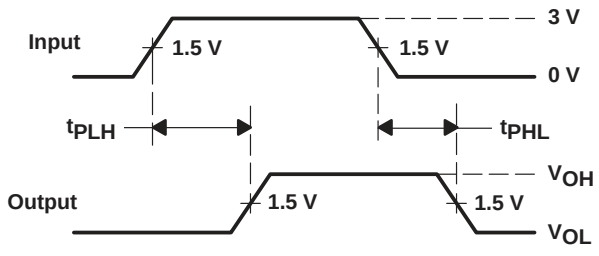


R_X = 13, 26, or 56 Ω

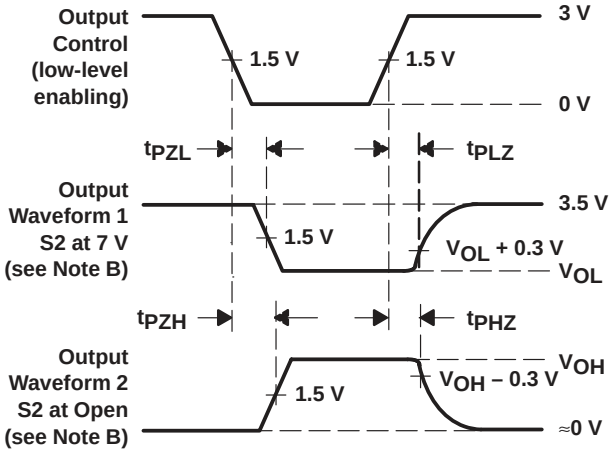
LOAD CIRCUIT

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (9A–11A and B port)	Up	Open
t_{PLH}/t_{PHL} (1A–8A)	Up	7 V
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH} (except 1A–8A)	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured between 1 V and 2 V of the output waveform.
F. t_t is measured between 10% and 90% of the output waveform.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABTE16246DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTE16246	Samples
SN74ABTE16246DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTE16246	Samples
SN74ABTE16246DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTE16246	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

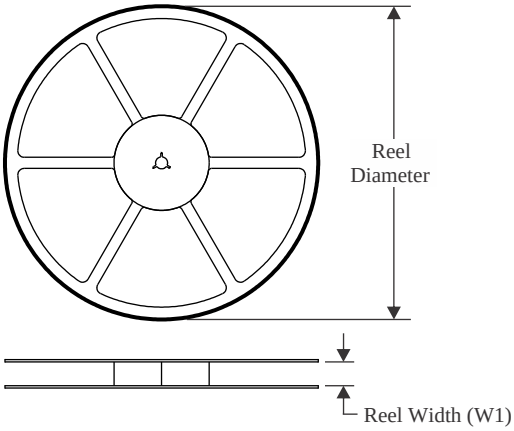
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

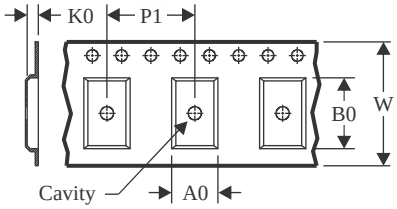
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

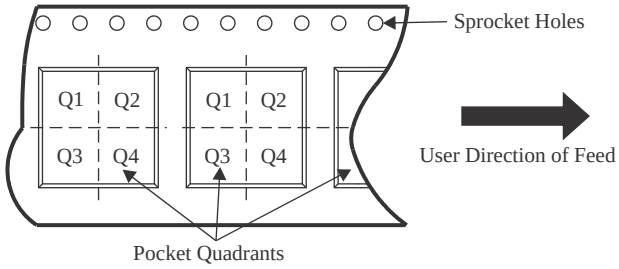


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

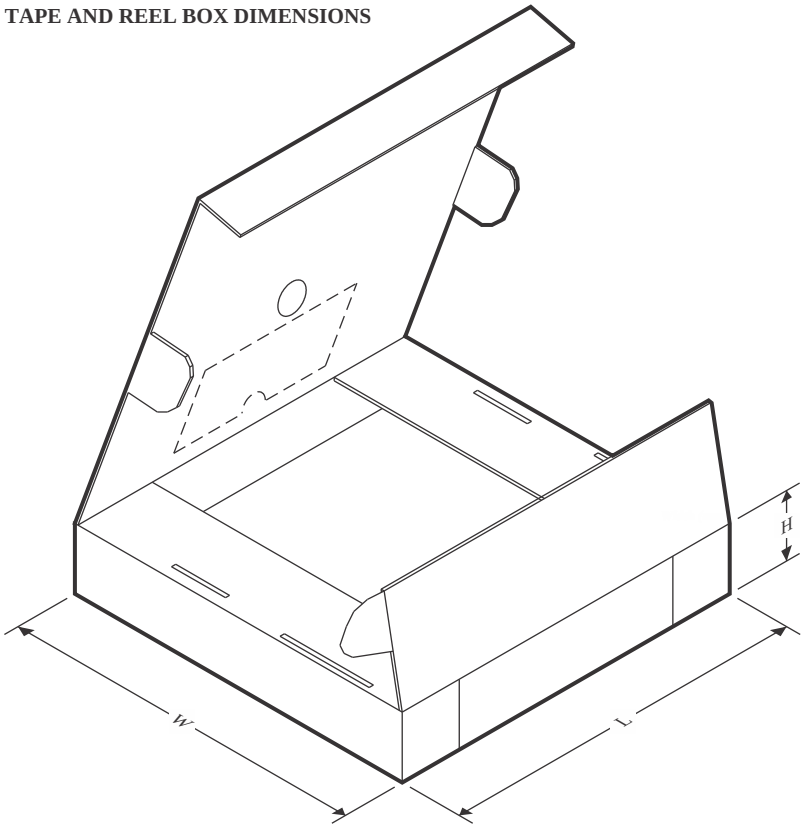
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTE16246DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABTE16246DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

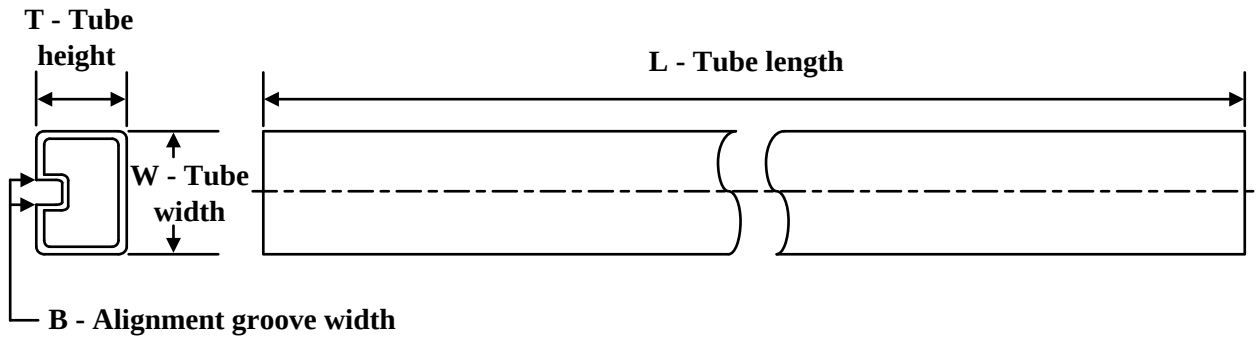
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTE16246DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABTE16246DLR	SSOP	DL	48	1000	367.0	367.0	55.0

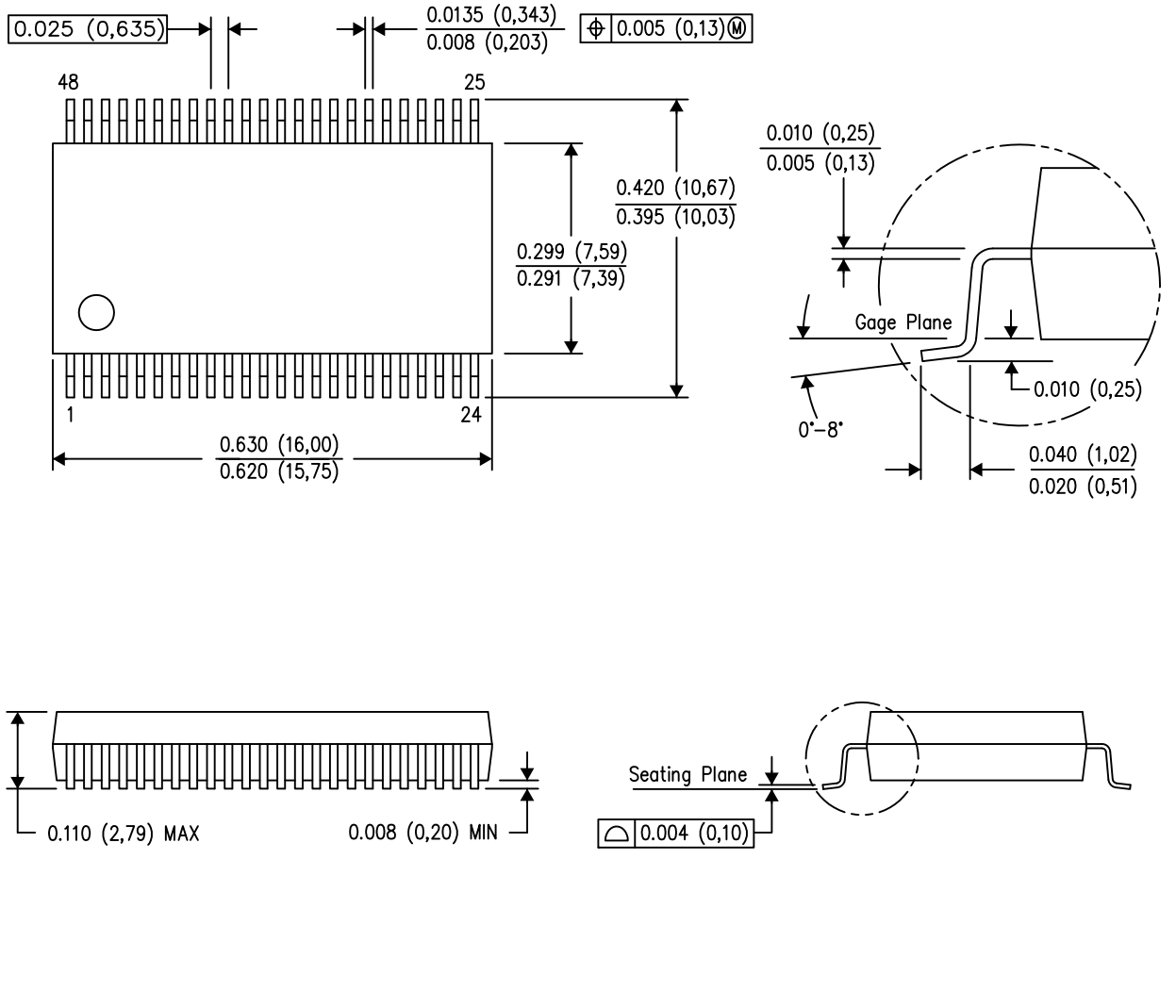
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABTE16246DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

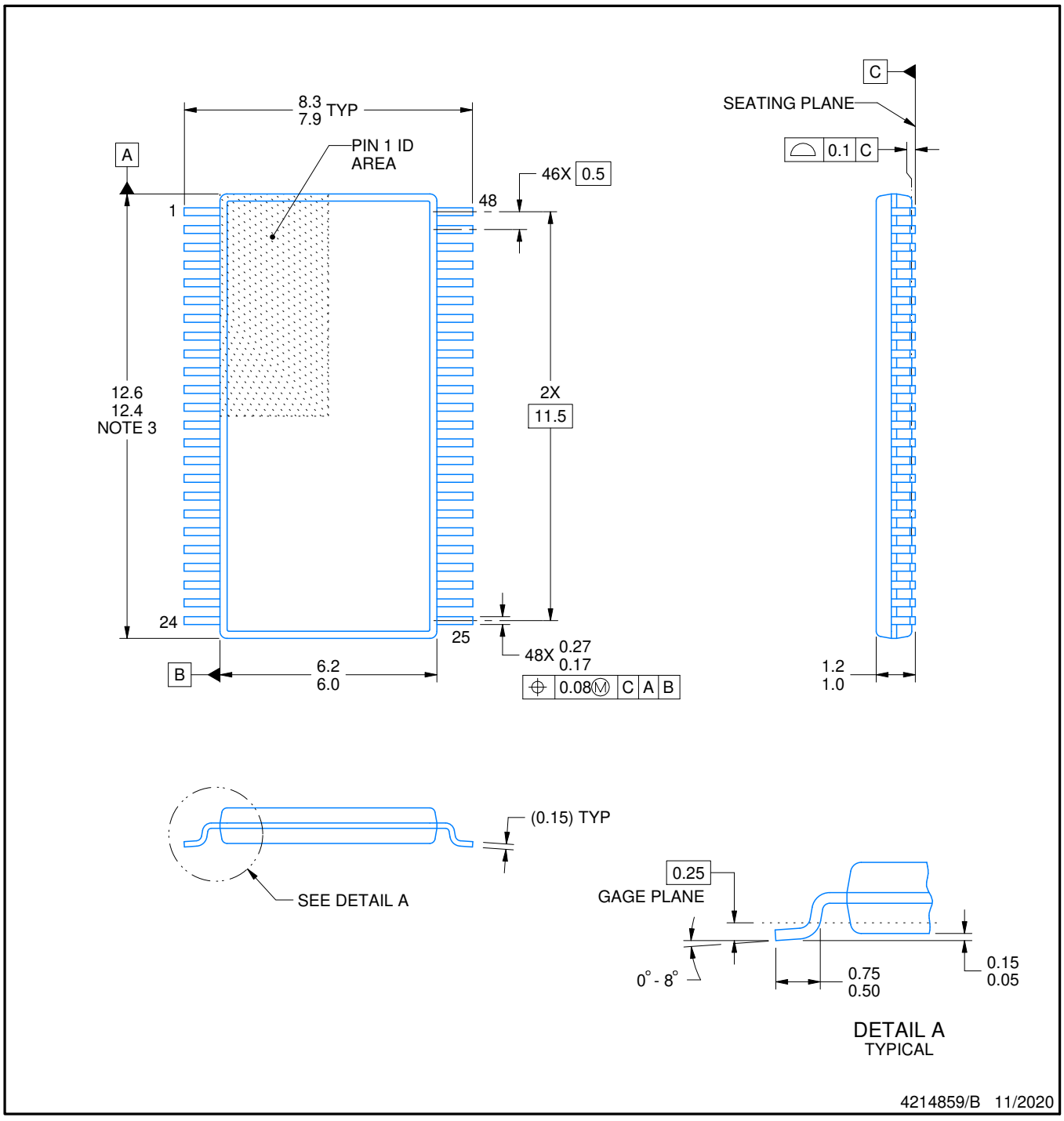
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0048A

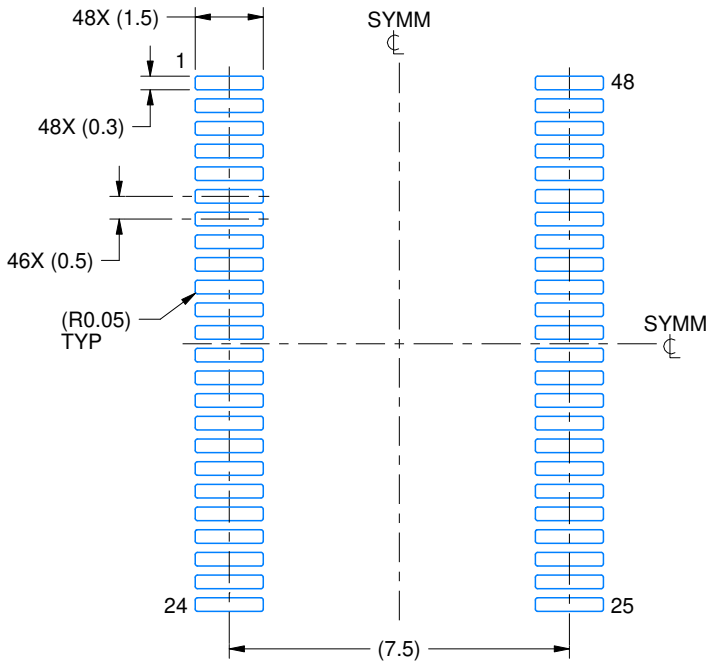
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

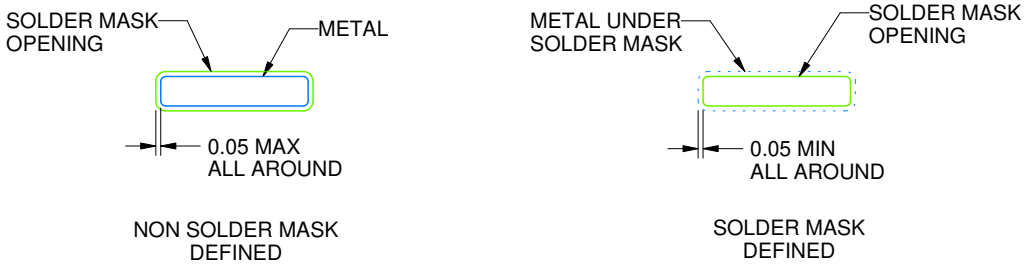


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

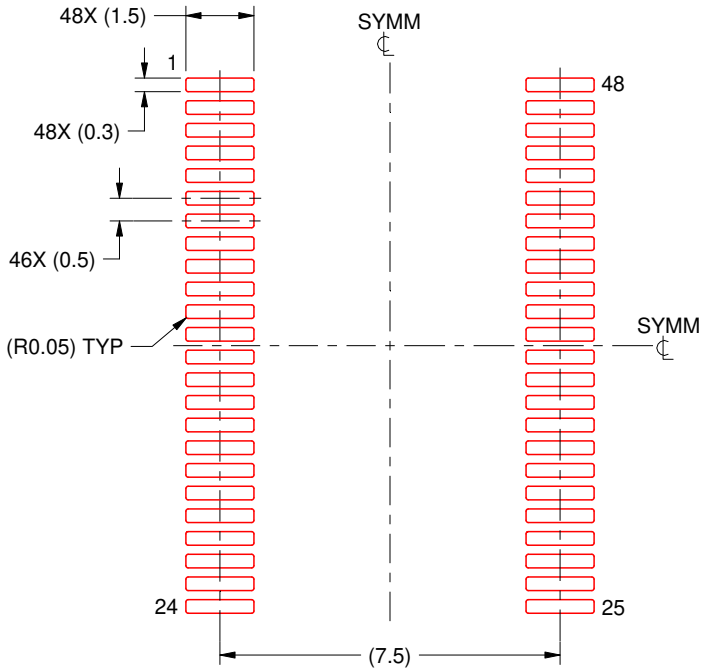


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

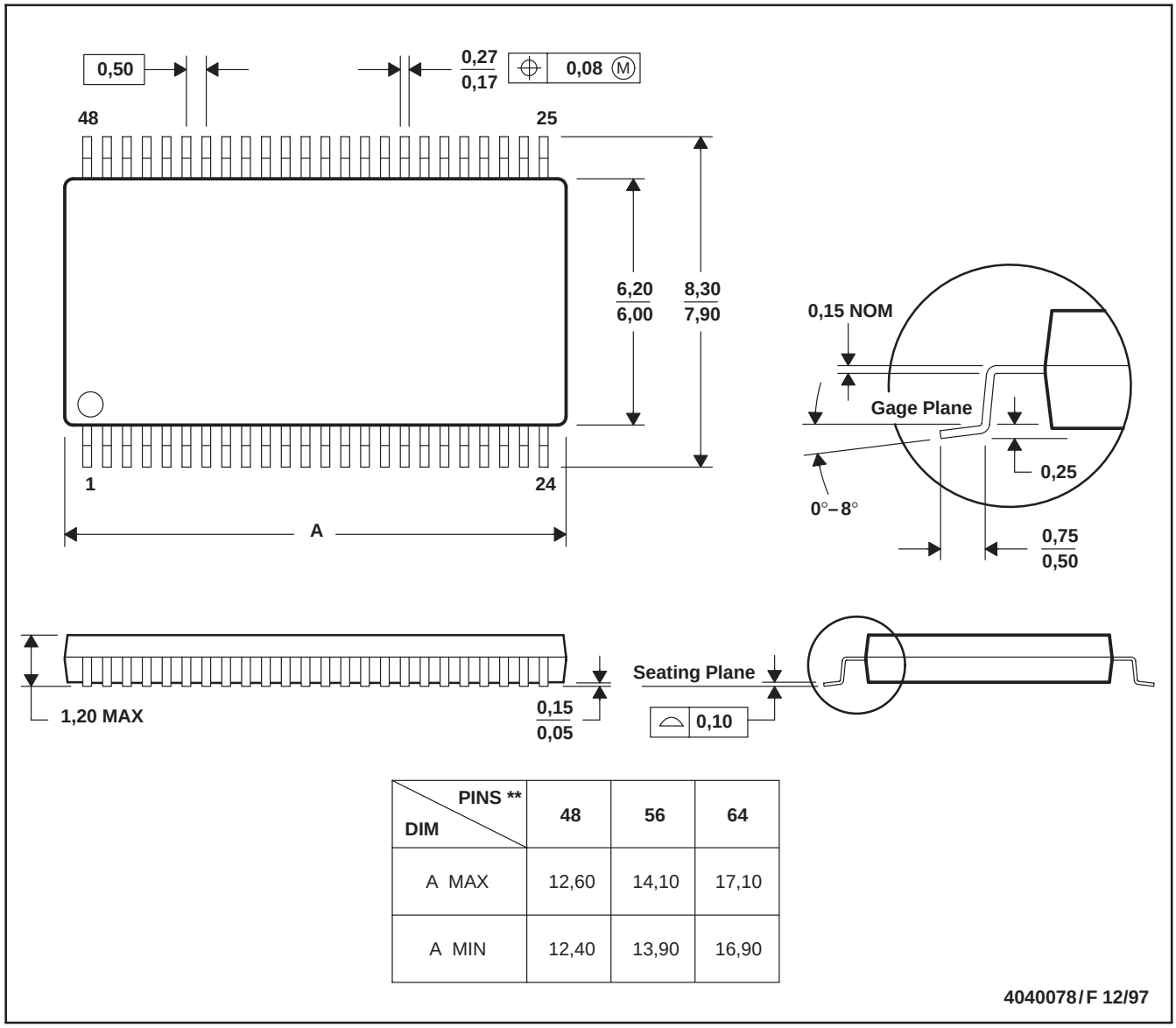
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265