SC2446A
Dual-Phase, Single or Dual Output Synchronous Step-Down Controller

Description

The SC2446A is a high-frequency dual synchronous step-down switching power supply controller. It provides out-of-phase output gate signals. The SC2446A operates in synchronous continuous-conduction mode. Both phases are capable of maintaining regulation with sourcing or sinking load currents, making the SC2446A suitable for generating both V_{DDQ} and the tracking V_{TT} for DDR applications.

The SC2446A employs fixed frequency peak current-mode control for the ease of frequency compensation and fast transient response.

The dual-phase step-down controllers of the SC2446A can be configured to provide two individually controlled and regulated outputs or a single output with shared current in each phase. The Step-down controllers operate from an input of at least 4.7V and are capable of regulating outputs as low as 0.5V

The step-down controllers in the SC2446A have the provision to sense inductor R_{DC} voltage drop for current-mode control. This sensing scheme eliminates the need of the current-sense resistor and is more noise-immune than direct sensing of the high-side or the low-side MOSFET voltage. Precise current-sensing with sense resistor is optional.

Individual soft-start and overload shutdown timer is included in each step-down controller. The SC2446A implements hiccup overload protection. In two-phase single-output configuration, the master timer controls the soft-start and overload shutdown functions of both controllers.

Features

- 2-Phase synchronous continuous conduction mode for high efficiency step-down converters
- Out of phase operation for low input current ripples
- Output source and sink currents
- Fixed frequency peak current-mode control
- 50mV/-75mV maximum current sense voltage
- Inductive current-sensing for low-cost applications
- Optional resistor current-sensing for precise current-limit
- Dual outputs or 2-phase single output operation
- Excellent current sharing between individual phases
- Wide input voltage range: 4.7V to 16V
- Individual soft-start, overload shutdown and enable
- Duty cycle up to 88%
- 0.5V feedback voltage for low-voltage outputs
- External reference input for DDR applications
- Programmable frequency up to 1MHz per phase
- External synchronization
- Industrial temperature range
- 28-lead TSSOP lead free package. This product is fully WEEE and RoHS compliant

Applications

- Telecommunication power supplies
- DDR memory power supplies
- Graphic power supplies
- Servers and base stations

Typical Application Circuit

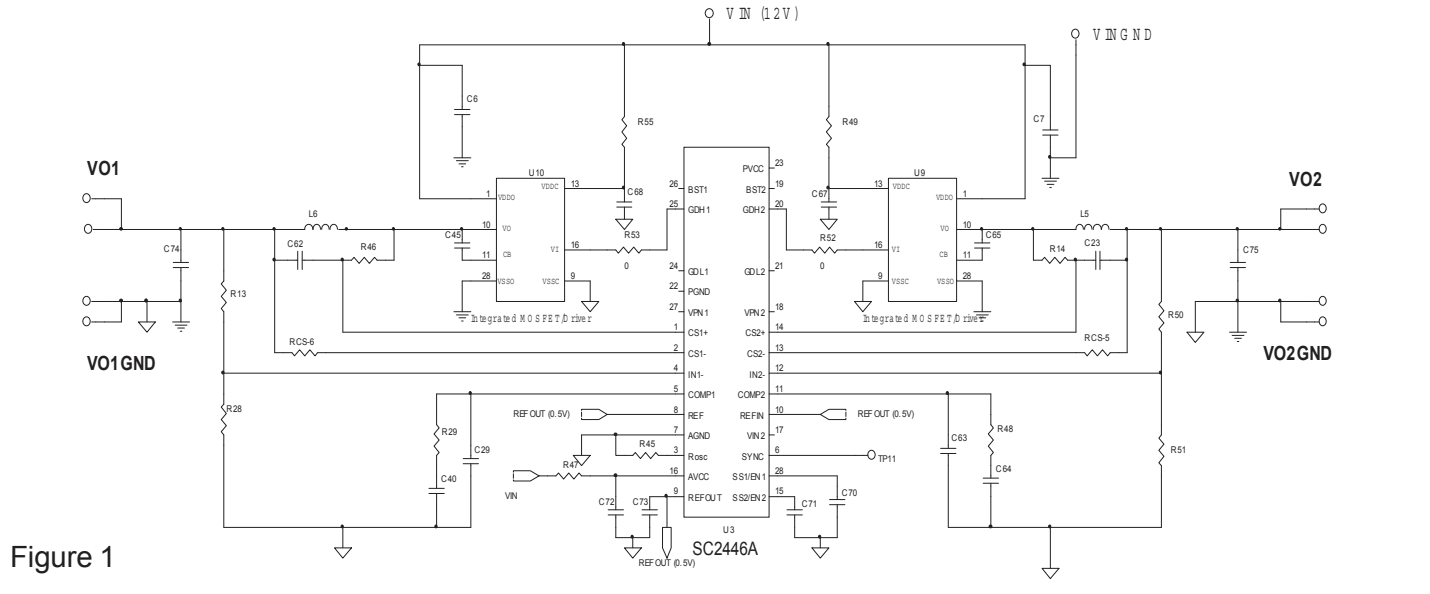


Figure 1

Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum Ratings	Units
Supply Voltage	AVCC	-0.3 to 16	V
Gate Outputs GDH1, GDH2, GDL1, GDL2 voltages	V_{GDH1}, V_{GDH2},V_{GDL1}, V_{GDL2}	-0.3 to 6	V
IN1-, IN2- Voltages	V_{IN1-},V_{IN2-}	-0.3 to AVCC+0.3	V
REF_{OUT} Voltages	V_{REF} ,V_{REFOUT}	-0.3 to 6	V
REF, REF_{IN} Voltage	V_{REFIN}	-0.3 to AVCC+0.3	V
COMP1, COMP2 Voltages	$V_{COMP1,}V_{COMP2}$	-0.3 to AVCC+0.3	V
CS1+, CS1-, CS2+ and CS2- Voltages	$V_{CS1+,}V_{CS1-,}V_{CS2+,}V_{CS2-}$	-0.3 to AVCC+0.3	V
SYNC Voltage	V_{SYNC}	-0.3 to AVCC+0.3	V
SS1/EN1 AND SS2/EN2 Voltages	$V_{SS1,}V_{SS2}$	-0.3 to 6	V
Ambient Temperature Range	T_A	-40 to 125	°C
Thermal Resistance Junction to Case (TSSOP-28)	θ_{JC}	13	°C/W
Thermal Resistance Junction to Ambient (TSSOP-28)	θ_{JA}	84	°C/W
Storage Temperature Range	T_{STG}	-60 to 150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	260	°C
Maximum Junction Temperature	T_J	150	°C

Electrical Characteristics

Unless specified: AVCC = 12V, SYNC = 0, R_{osc} = 51.1kΩ, -40°C < T_A = T_J < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Undervoltage Lockout						
AVCC Start Threshold	$AVCC_{TH}$	AVCC Increasing		4.5	4.7	V
AVCC Start Hysteresis	$AVCC_{HYST}$			0.2		V
AVCC Operating Current	I_{CC}	AVCC= 12V		8	15	mA
AVCC Quiescent Current in UVLO		AVCC = $AVCC_{TH}$ - 0.2V		2.5		mA
Channel 1 Error Amplifier						
Input Common-Mode Voltage Range		(Note 1)	0		3	V
Inverting Input Voltage Range		(Note 1)	0		AVCC	V
Input Offset Voltage		0 ~ 70° C		1	±3	mV
Non-Inverting Input Bias Current	I_{REF}			-100	-250	nA
Inverting Input Bias Current	I_{IN1-}			-100	-250	nA
Amplifier Transconductance	G_{M1}			260		$\mu\Omega^{-1}$
Amplifier Open-Loop Gain	a_{OL1}			65		dB
Amplifier Unity Gain Bandwidth				5		MHz
Minimum COMP1 Switching Threshold		V_{CS1+} = V_{CS1-} = 0 V_{SS1} Increasing		2.2		V

Electrical Characteristics (Cont.)

Unless specified: AVCC = 12V, SYNC = 0, R_{OSC} = 51.1kΩ, -40°C < T_A = T_J < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Amplifier Output Sink Current		V_{IN1-} = 1V, V_{COMP1} = 2.5V		16		µA
Amplifier Output Source Current		V_{IN1-} = 0, V_{COMP1} = 2.5V		12		µA
Channel 2 Error Amplifier						
Input Common-mode Voltage Range		(Note 1)	0		3	V
Inverting Input Voltage Range		(Note 1)	0		AVCC	V
Input Offset Voltage		0 ~ 70° C		1.5	±3	mV
Non-inverting Input Bias Current	I_{IN2+}			-150	-380	nA
Inverting Input Bias Current	I_{IN2-}			-100	-250	nA
Inverting Input Voltage for 2-Phase Single Output Operation			2.5			V
Amplifier Transconductance	G_{M2}			260		$\mu\Omega^{-1}$
Amplifier Open-Loop Gain	a_{OL2}			65		dB
Amplifier Unity Gain Bandwidth				5		MHz
Minimum COMP2 Switching Threshold		V_{CS2+} = V_{CS2-} = 0 V_{SS2} Increasing		2.2		V
Amplifier Output Sink Current		V_{COMP2} = 2.5V		16		µA
Amplifier Output Source Current		V_{COMP2} = 2.5V		12		µA
Oscillator						
Channel Frequency	f_{CH1}, f_{CH2}	0 ~ 70° C	450	500	550	KHz
Synchronizing Frequency		(Note 1)	$2.1f_{CH}$			KHz
SYNC Input High Voltage			1.5			V
SYNC Input Low Voltage					0.5	V
SYNC Input Current	I_{SYNC}	V_{SYNC} = 0.2V V_{SYNC} = 2V			1 50	µA
Channel Maximum Duty Cycle	D_{MAX1}, D_{MAX2}			88		%
Channel Minimum Duty Cycle	D_{MIN1}, D_{MIN2}				0	%
Current-limit Comparators						
Input Common-Mode Range			0		AVCC - 1	V
Cycle-by-cycle Peak Current Limit	V_{ILIM1+}, V_{ILIM2+}	V_{CS1-} = V_{CS2-} = 0.5V, Sourcing Mode, 0 ~ 70° C	40	50	60	mV
Valley Current Overload Shutdown Threshold	V_{ILIM1-}, V_{ILIM2-}	V_{CS1-} = V_{CS2-} = 0.5V, Sinking Mode, 0 ~ 70° C	-60	-75	-90	mV
Positive Current-Sense Input Bias Current	I_{CS1+}, I_{CS2+}	V_{CS1+} = V_{CS1-} = 0 V_{CS2-} = V_{CS2-} = 0		-0.7	-2	µA
Negative Current-Sense Input Bias Current	I_{CS1-}, I_{CS2-}	V_{CS1+} = V_{CS1-} = 0 V_{CS2+} = V_{CS2-} = 0		-0.7	-2	µA

Electrical Characteristics (Cont.)

Unless specified: AVCC = 12V, SYNC = 0, R_{OSC} = 51.1kΩ, -40°C < T_A = T_J < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PWM Outputs						
Peak Source Current	G_{DL1}, G_{DL2}, G_{DH1}, G_{DH2}	AVCC = 12V		4		mA
Peak Sink Current	G_{DL1}, G_{DL2}, G_{DH1}, G_{DH2}	AVCC = 12V		3		mA
Output High Voltage		Source I_O = 1.2mA, 0 ~ 70° C	3.95		5	V
Output Low Voltage		Sink I_O = 1mA	0		0.4	V
Minimum On-Time		T_A = 25°C		120		ns
Soft-Start, Overload Latchoff and Enable						
Soft-Start Charging Current	I_{SS1}, I_{SS2}	V_{SS1} = V_{SS2} = 1.5V		1.8		µA
Overload Latchoff Enabling Soft-Start Voltage		V_{SS1} and V_{SS2} Increasing		3.2		V
Overload Latchoff IN1- Threshold		V_{SS1} = 3.8V, V_{IN1-} Decreasing		0.5V_{REF}		V
Overload Latchoff IN2- Threshold		V_{SS2} = 3.8V, V_{IN2-} Decreasing		0.5 X V_{REFIN}		V
Soft-Start Discharge Current	$I_{SS1(DIS)}$, $I_{SS2(DIS)}$	V_{IN1-} = 0.5V_{REF}, V_{IN2-} = 0.5V_{REFIN}, V_{SS1} = V_{SS2} = 3.8V		1.2		µA
Overload Latchoff Recovery Soft-Start Voltage	V_{SSRCV1}, V_{SSRCV2}	V_{SS1} and V_{SS2} Decreasing	0.3	0.5	0.7	V
PWM Output Disable SS/EN Voltage			0.7	0.8		V
PWM Output Enable SS/EN Voltage				1.2	1.5	V
Internal 0.5V Reference Buffer						
Output Voltage	V_{REFOUT}	I_{REFOUT} = -1mA, 0°C < T_A = T_J < 70°C	495	500	505	mV
Load Regulation		0 < I_{REFOUT} < -5mA		0.05		%/mA
Line Regulation		$AVCC_{TH}$ < AVCC < 15V, I_{REFOUT} = -1mA			0.02%	%V

Notes:
(1) Guaranteed by design not tested in production.
(2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configurations

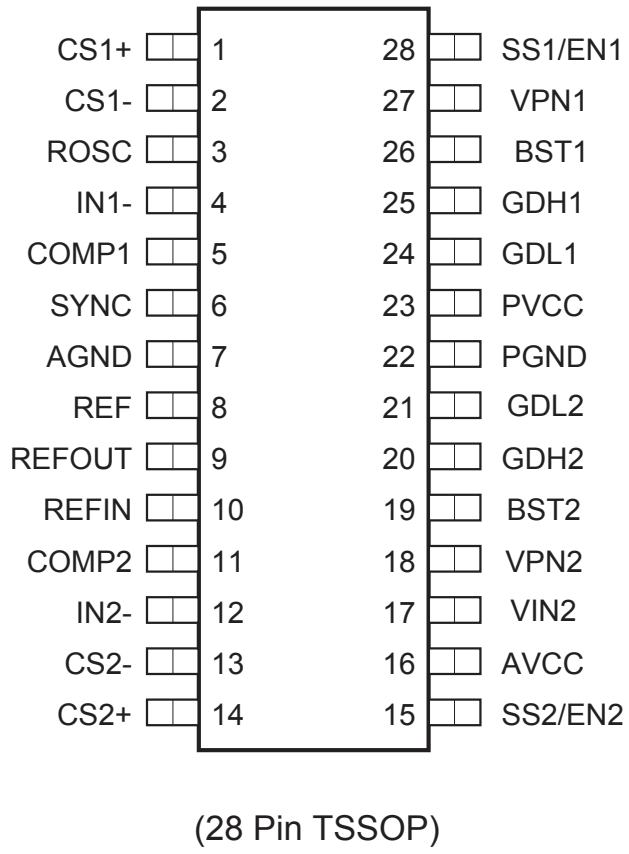


Figure 2

Ordering Information

Device	Package	Temp. Range(T_A)
SC2446AITSTRT(1)(2)	TSSOP-28	-40 to 125°C
SC2446AEVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices for TSSOP package.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

TSSOP Package

Pin	Pin Name	Pin Function
1	CS1+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Controller 1.
2	CS1-	The Inverting Input of the Current-sense Amplifier/Comparator for the Controller 1. Normally tied to the output of the converter.
3	ROSC	An external resistor connected from this pin to GND sets the oscillator frequency.
4	IN1-	Inverting Input of the Error Amplifier for the Step-down Controller 1. Tie an external resistive divider between OUTPUT1 and the ground for output voltage sensing.
5	COMP1	The Error Amplifier Output for Step-down Controller 1. This pin is used for loop compensation.
6	SYNC	Edge-triggered Synchronization Input. When not synchronized, tie this pin to a voltage above 1.5V or the ground. An external clock (frequency > frequency set with ROSC) at this pin synchronizes the controllers.
7	AGND	Analog Signal Ground.
8	REF	The non-inverting input of the error amplifier for the step down converter 1.
9	REFOUT	Buffered output of the internal reference voltage 0.5V.
10	REFIN	An external Reference voltage is applied to this pin.The non-inverting input of the error amplifier for the step-down converter 2 is internally connected to this pin.
11	COMP2	The Error Amplifier Output for Step-down Controller 2. This pin is used for loop compensation.
12	IN2-	Inverting Input of the Error Amplifier for the Step-down Controller 2. Tie an external resistive divider between output2 and the ground for output voltage sensing. Tie to AVCC for two-phase single output applications
13	CS2-	The Inverting Input of the Current-sense Amplifier/Comparator for the Controller 2. Normally tied to the output of the converter.
14	CS2+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Controller 2
15	SS2/EN2	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for step-down converter 2. Pulling this pin below 0.7V shuts off the gate drivers for the second controller. Leave open for two-phase single output applications.
16	AVCC	Power Supply Voltage for the Analog Portion of the Controllers.
17	VIN2	No connection.
18	VPN2	No connection.
19	BST2	No connection.
20	GDH2	PWM Output for the High-side N-channel MOSFET of Output 2.

Pin Descriptions

Pin	Pin Name	Pin Function
21	GDL2	Logic Enable gate drive signal for Output 2.
22	PGND	No connection.
23	PVCC	No connection.
24	GDL1	Logic Enable gate drive signal for Output 1.
25	GDH1	PWM Output for the High-side N-channel MOSFET of Output 1.
26	BST1	No connection.
27	VPN1	No connection.
28	SS1/EN1	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for buck converter 1. Pulling this pin below 0.7V shuts off the gate drivers for the first controller.

Block Diagram

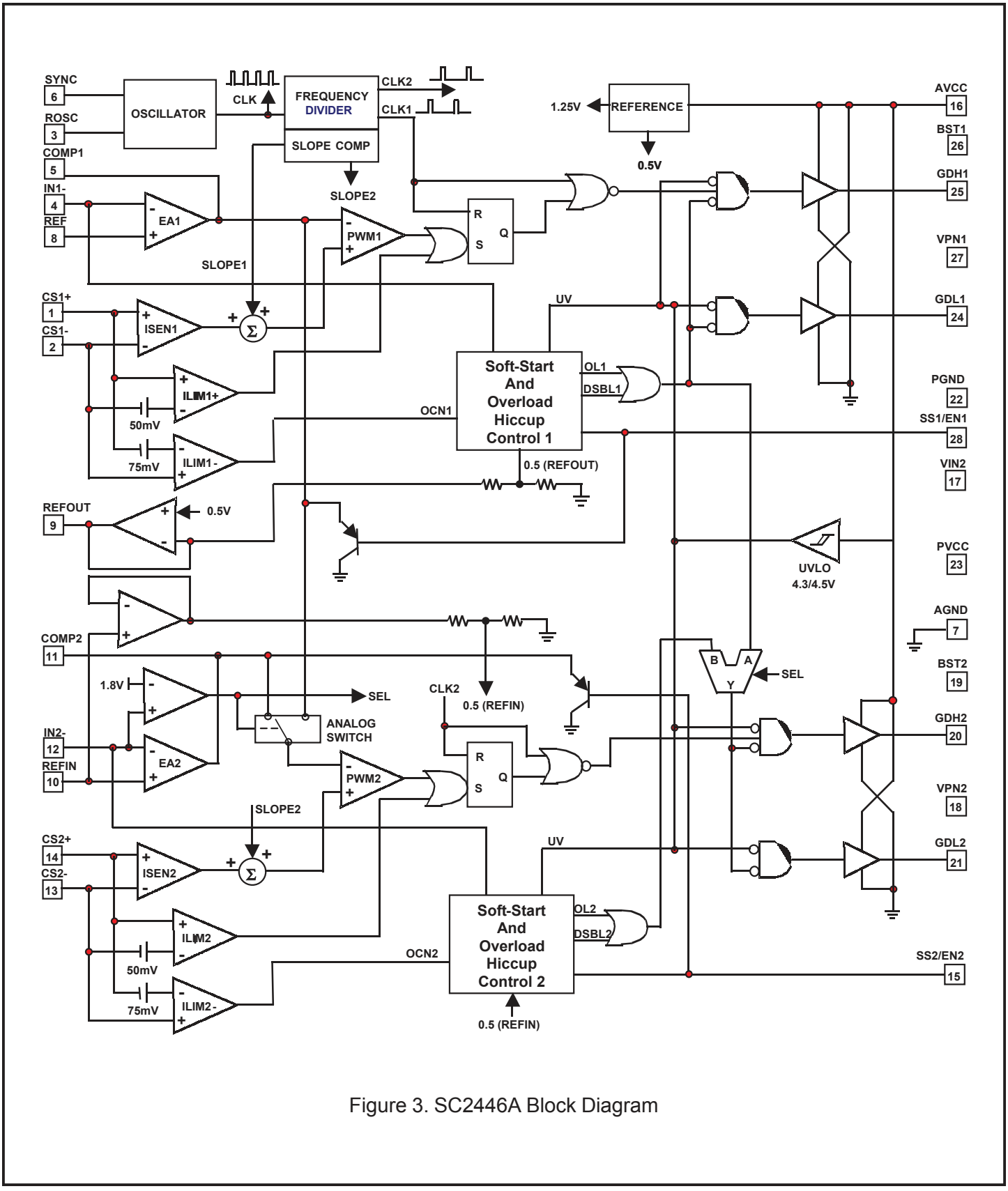


Figure 3. SC2446A Block Diagram

Block Diagram

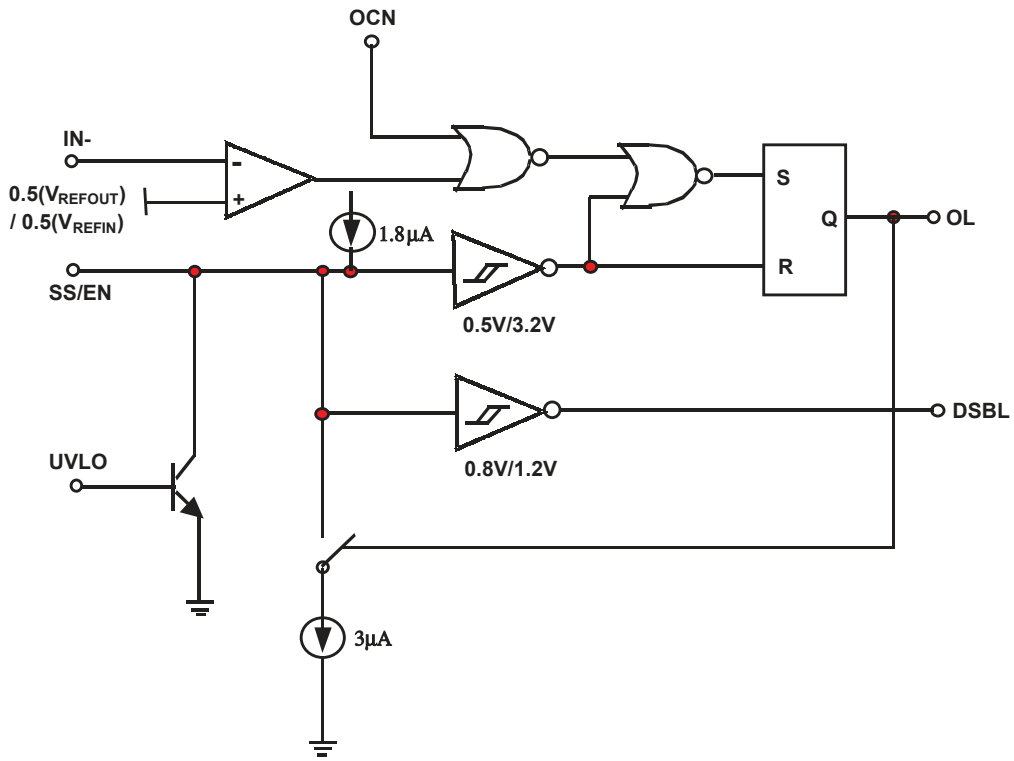


Figure 4. Soft-Start and Overload Hiccup Control Circuit

Application Information

SC2446A consists of two current-mode synchronous buck controllers with many integrated functions. By proper application circuitry configuration, SC2446A can be used to generate
1) two independent outputs from a common input or two different inputs or
2) dual phase output with current sharing,
3) current sourcing/sinking from common or separate inputs as in DDR (I and II) memory application.
The application information related to the converter design using SC2446A is described in the following.

Step-down Converter

Starting from the following step-down converter specifications,

Input voltage range: $V_{in} \in [V_{in,min}, V_{in,max}]$
Input voltage ripple (peak-to-peak): ΔV_{in}
Output voltage: V_o
Output voltage accuracy: ε
Output voltage ripple (peak-to-peak): ΔV_o
Nominal output (load) current: I_o
Maximum output current limit: $I_{o,max}$
Output (load) current transient slew rate: dI_o (A/s)
Circuit efficiency: η
Selection criteria and design procedures for the following are described.
1) output inductor (L) type and value,
2) output capacitor (C_o) type and value,
3) input capacitor (C_{in}) type and value,
4) power MOSFET's,
5) current sensing and limiting circuit,
6) voltage sensing circuit,
7) loop compensation network.

Operating Frequency (f_s)

The switching frequency in the SC2446A is user-programmable. The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.

1) Passive component size
2) Circuitry efficiency
3) EMI condition
4) Minimum switch on time and
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFETs/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

Minimum Switch On Time Consideration

In the SC2446A the falling edge of the clock turns on the top MOSFET gate. The inductor current and the sensed voltage ramp up. After the sensed voltage crosses a threshold determined by the error amplifier output, the top MOSFET gate is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. The SC2446A has a minimum on time of about 120ns at room temperature. This is the shortest on interval of the controlling FET. The controller either does not turn on the top MOSFET at all or turns it on for at least 120ns.

For a synchronous step-down converter, the operating duty cycle is V_O/V_{IN}. So the required on time for the top MOSFET is $V_O/(V_{IN}fs)$. If the frequency is set such that the required pulse width is less than 120ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at very high switching frequency and very short duty cycle is not practical. If the voltage conversion ratio V_O/V_{IN} and hence the required duty cycle is higher, the switching frequency can be increased to reduce the sizes of passive components.
There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC2446A. For ease of control, we recommend the required pulse width to be at least 1.5 times the minimum on time.

Setting the Switching Frequency

The switching frequency is set with an external resistor connected from Pin 3 to the ground. The set frequency is inversely proportional to the resistor value (Figure 5).

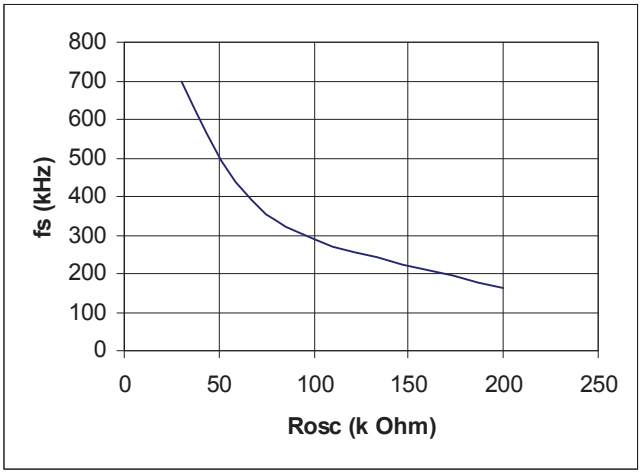


Figure 5. Free running frequency vs. R_{OSC}.

Inductor (L) and Ripple Current

Both step-down controllers in the SC2446A operate in synchronous continuous-conduction mode (CCM) regardless of the output load. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely smaller inductors results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.

Assuming that the inductor current ripple (peak-to-peak) value is $\delta * I_o$, the inductance value will then be

$$L = \frac{V_o(1-D)}{\delta I_o f_s}.$$

The peak current in the inductor becomes (1+δ/2)*Io and the RMS current is

$$I_{L,rms} = I_o\sqrt{1+\frac{\delta^2}{12}}.$$

The followings are to be considered when choosing inductors.

a) Inductor core material: For high efficiency applications above 350KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350KHz but with attendant higher core losses.

b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.

c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (C_o) and V_{out} Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR (R_{esr}) and ESL (L_{esl}) (Figure 6).

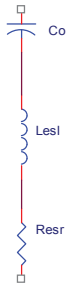


Figure 6. An equivalent circuit of C_o.

If the current through the branch is $i_b(t)$, the voltage across the terminals will then be

$$v_o(t) = V_o + \frac{1}{C_o}\int_0^t i_b(t)dt + L_{esl}\frac{di_b(t)}{dt} + R_{esr}i_b(t).$$

This basic equation illustrates the effect of ESR, ESL and C_o on the output voltage.

The first term is the DC voltage across C_o at time *t=0*. The second term is the voltage variation caused by the

Application Information (Cont.)

charge balance between the load and the converter output. The third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform with peak-to-peak value $\delta * I_o$, the ripple-voltage caused by inductor current ripples is

$$\Delta v_C \approx \frac{\delta I_o}{8 C_o f_s},$$

the ripple-voltage due to ESL is

$$\Delta v_{ESL} = L_{esl} f_s \frac{\delta I_o}{D},$$

and the ESR ripple-voltage is

$$\Delta v_{ESR} = R_{esr} \delta I_o.$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESL's. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage $< \Delta V_o$, the ESR should satisfy

$$R_{esr1} < \frac{\Delta V_o}{\delta I_o}.$$

To limit the dynamic output voltage overshoot/undershoot within α (say 3%) of the steady state output voltage) from no load to full load, the ESR value should satisfy

$$R_{esr2} < \frac{\alpha V_o}{I_o}.$$

Then, the required ESR value of the output capacitors should be

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}.$$

The voltage rating of aluminum capacitors should be at least $1.5V_o$. The RMS current ripple rating should also be greater than

$$\frac{\delta I_o}{2\sqrt{3}}.$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy

$$C_o > \frac{10}{2\pi f_s R_{esr}}.$$

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant.

For example, if a 10µF, 4mΩ ceramic capacitor is connected in parallel with 2x1500µF, 90mΩ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100µF, 2mΩ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100µF, 2mΩ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR's either. Instead they should be calculated using the following formulae.

Application Information (Cont.)

$$C_{eq}(\omega) := \frac{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}{(R_{1a}{}^2 C_{1a}+R_{1b}{}^2 C_{1b})\omega^2 C_{1a}C_{1b}+(C_{1a}+C_{1b})}$$

$$R_{eq}(\omega) := \frac{R_{1a}R_{1b}(R_{1a}+R_{1b})\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (R_{1b}C_{1b}{}^2 + R_{1a}C_{1a}{}^2)}{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}$$

where R_{1a} and C_{1a} are the ESR and capacitance of electrolytic capacitors, and R_{1b} and C_{1b} are the ESR and capacitance of the ceramic capacitors respectively. (Figure 7)

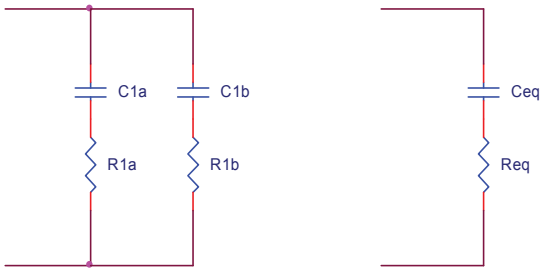


Figure 7. Equivalent RC branch.

Req and Ceq are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If $R_{1a} = R_{1b} = R_1$ and $C_{1a} = C_{1b} = C_1$, then R_{eq} and C_{eq} will be frequency-independent and

$$R_{eq} = 1/2\ R_1 \text{ and } C_{eq} = 2C_1.$$

Input Capacitor (C_{in})

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 8.

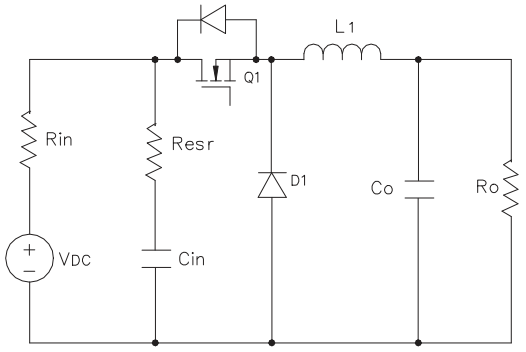


Figure 8. A simple model for the converter input

In Figure 8 the DC input voltage source has an internal impedance R_{in} and the input capacitor C_{in} has an ESR of R_{esr}. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 9.

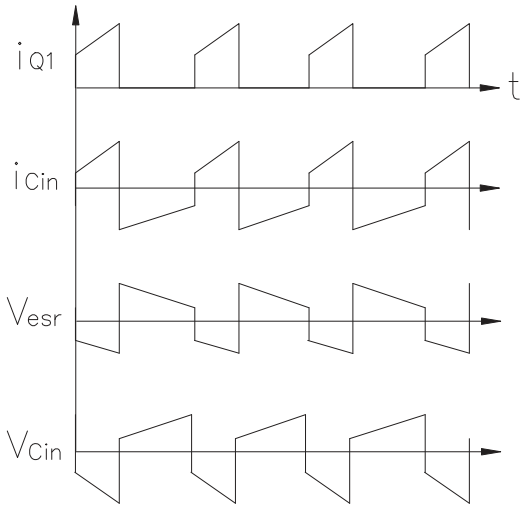


Figure 9. Typical waveforms at converter input.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFETs on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o\sqrt{D[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2 + \frac{D}{\eta^2}(1-D)]}.$$

Application Information (Cont.)

The power dissipated in the input capacitors is then

$$P_{Cin} = I_{Cin}{}^2 R_{esr}.$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is

$$\Delta v_{ESR} = R_{esr}(1+\frac{\delta}{2})I_o.$$

The peak-to-peak input voltage ripple due to the capacitor is

$$\Delta v_C \approx \frac{DI_o}{C_{in} f_s},$$

From these two expressions, C_{IN} can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2446A operate at 180 degrees from each other. If both step-down channels in the SC2446A are connected in parallel, both the input and the output RMS currents will be reduced.

Ripple cancellation effect of interleaving allows the use of smaller input capacitors. When converter outputs are connected in parallel and interleaved, smaller inductors and capacitors can be used for each channel. The total output ripple-voltage remains unchanged. Smaller inductors speeds up output load transient.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the *RMS* value of the ripple current in the input capacitor.

Let the duty ratio and output current of Channel 1 and Channel 2 be D_1, D_2 and I_{o1}, I_{o2}, respectively.

If D_1<0.5 and D_2<0.5, then

$$I_{Cin} \approx \sqrt{D_1 I_{o1}{}^2 + D_2 I_{o2}{}^2}.$$

Choosing Power MOSFETs

The power devices with integrated gate drivers such as PIP212, R2J20601NP, PIP202, PIP201 and IP2001, IP2002 are suitable for SC2446A application.

Current Sensing

Inductor current sensing is required for the current-mode control. Although the inductor current can be sensed with a precision resistor in series with the inductor, the lossless inductive current sense technique is used in the SC2446A. This technique has the advantages of

1) lossless current sensing,
2) lower cost compared to resistive sense
3) more accurate compared to the $R_{DS(ON)}$ sense

The basic arrangement of the inductive current sense is shown in Figure 10.

Where, R_L is the equivalent series resistance of the output inductor. The added R_s and C_s form a RC branch for inductor current sensing.

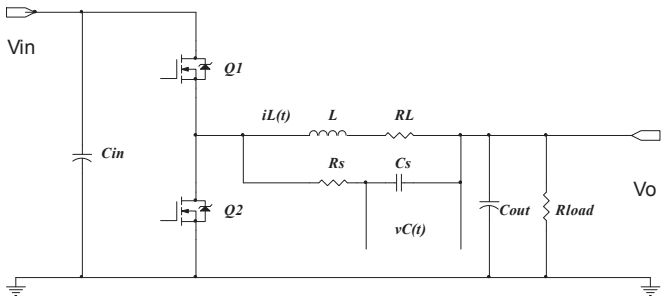


Figure 10. The basic structure of inductive current sense.

In steady state, the DC value,

$$V_{CS} = R_L I_O$$

Application Information (Cont.)

It is noted that the DC value of V_{Cs} is independent of the value of L, R_s and C_s. This means that, if only the average load current information is needed (such as in average current mode control), this current sensing method is effective without time constant matching requirement. In the current mode control as implemented in SC2446A, the voltage ripple on C_s is critical for PWM operation. In fact, the AC voltage ripple peak-to-peak value of V_{Cs} (denoted as ΔV_{Cs}) directly effects the signal-to-noise ratio of the PWM operation. In general, smaller ΔV_{Cs} leads to lower signal-to-noise ratio and more noise sensitive operation. Larger ΔV_{Cs} leads to more circuit (power stage) parameter sensitive operation. A good engineering compromise is to make

$$\Delta V_{Cs} \sim R_L \ \delta I_o.$$

The pre-requisite for such relation is the so called time constant matching condition

$$\frac{L}{R_L} \approx R_s C_s.$$

For an example of application circuit, L = 1µH, RL = 1.8mΩ, the time constant R_sC_s should be set as 555.6µs. If one selects C_s = 33nF, then R_s = 16.9 kΩ.

Scaling the Current Limit

Over-current is handled differently in the SC2446A depending on the direction of the inductor current. If the differential sense voltage between CS+ and CS- exceeds +50mV, the top MOSFET will be turned off and the bottom MOSFET will be turned on to limit the inductor current. This +50mV is the cycle-by-cycle peak current limit when the load is drawing current from the converter. There is no cycle-by-cycle current limit when the inductor current flows in the reverse direction. If the voltage between CS1+ and CS- falls below -75mV, the controller will undergo overload shutdown and time-out with both the top and the bottom MOSFETs shut off. (See the section Overload Protection and Hiccup).

In the circuit of Figure 11, the equivalent inductor current limits are set according to

$$I_{LMcp} = \frac{50mV}{R_L},$$

when the load is sourcing current from the converter and

$$I_{LMcn} = -\frac{75mV}{R_L},$$

when the load is forcing current back to the input power source. If R_L = 1.8mΩ, then I_{LM} = 27.8 / -41.7A. The circuit in Figure 11 allows the user to scale the equivalent current limit with the same RL.

In the following design steps, the capacitor C_s in the current sensing part is commonly selected in the range of 22nF ~ 100nF.

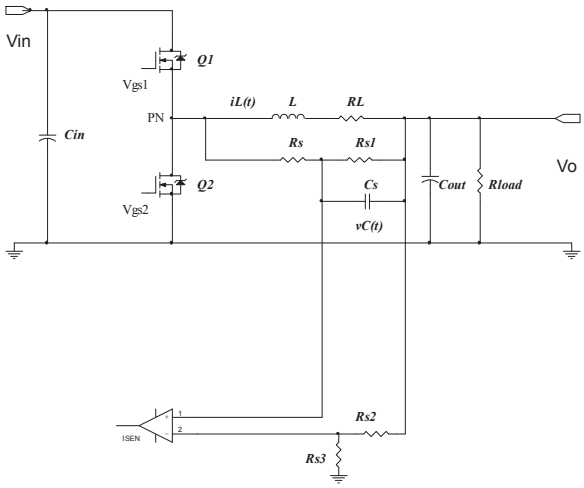


Figure 11. Scaling the equivalent current limit.

a) When the required current limit value I_{LM} is greater than I_{LMcp}, one just needs to remove R_{s3}, and solve the following equations

$$(R_s // R_{s1})\, C_s = \frac{L}{R_L},$$

$$I_{LM} R_L \frac{R_{s1}}{R_s + R_{s1}} = 50mV,$$

and $R_{s2} = R_s // R_{s1}$.

for R_s, R_{s1} and R_{s2}.

Application Information (Cont.)

Note that R_{S2} is selected as $R_S//R_{S1}$ in order to reduce the bias current effect of the current amplifier in SC2446A.

b) When the required current limit I_{LM} is less than I_{LMcp}, one just needs to remove R_{s1} and solve

$$R_s C_s = \frac{L}{R_L},$$

$$I_{LM} R_L + \frac{R_s}{R_{s3}} V_O = 50mV,$$

for R_s and R_{S3}.

R_{s2} is then obtained from

$$R_{s2} = \frac{R_{s3} R_s}{R_{s3} - R_s}.$$

Similar steps and equations apply to the current limit setting and scaling for current sinking mode.

Overload Protection and Hiccup

During start-up, the capacitor from the SS/EN pin to ground functions as a soft-start capacitor. After the converter starts and enters regulation, the same capacitor operates as an overload shutoff timing capacitor. As the load current increases, the cycle-by-cycle current-limit comparator will first limit the inductor current. Further increase in loading will cause the output voltage (hence the feedback voltage) to fall. If the feedback voltage falls to less than (50% for Ch1, 50% for Ch2) of the reference voltage, the controller will shut off both the top and the bottom MOSFETs. Meanwhile an internal net 1.2µA current source discharges the soft-start capacitor $C_{32}(C_{33})$ connected to the SS/EN pin.

When the capacitor is discharged to 0.5V, a 1.8µA current source recharges the SS/EN capacitor and converter restarts. If overload persists, the controller will shut down the converter when the soft start capacitor voltage exceeds 3.2V. The converter will repeatedly start and shut off until it is no longer overloaded. This hiccup mode of overload protection is a form of foldback current limiting. The following calculations estimate the average inductor current when the converter output is shorted to the ground.

a) The time taken to discharge the capacitor from 3.2V to 0.5V

$$t_{ssf} = C_{32} \frac{(3.2 - 0.5)V}{1.2\mu A}.$$

If C_{32} = 0.1µF, t_{ssf} is calculated as 225ms.

b) The soft start time from 0.5V to 3.2V

$$t_{ssr} = C_{32} \frac{(3.2 - 0.5)V}{1.8\mu A}.$$

When C_{32} = 0.1µF, t_{ssr} is calculated as 150ms. Note that during soft start, the converter only starts switching when the voltage at SS/EN exceeds 1.2V.

c) The effective start-up time is

$$t_{sso} = C_{32} \frac{(3.2 - 1.2)V}{1.8\mu A}.$$

The average inductor current is then

$$I_{Leff} = I_{LMcp} \frac{t_{sso}}{t_{ssf} + t_{ssr}}.$$

$I_{Leff} \approx 0.30\ I_{LMcp}$ and is independent of the soft start capacitor value. The converter will not overheat in hiccup.

Setting the Output Voltage

The non-inverting input of the channel-one error amplifier is internally tied the 0.5V voltage reference output (Pin 8). The non-inverting input of the channel-two error amplifier is brought out as a device pin (Pin 10) to which the user can connect Pin 8 or an external voltage reference. A simple voltage divider (R_{o1} at top and R_{o2} at bottom) sets the converter output voltage. The voltage feedback gain $h=0.5/V_o$ is related to the divider resistors value as

$$R_{o2} = \frac{h}{1-h} R_{o1.}$$

Once either R_{o1} or R_{o2} is chosen, the other can be calculated for the desired output voltage V_o. Since the number of standard resistance values is limited, the calculated resistance may not be available as a standard value resistor. As a result, there will be a set error in the

Application Information (Cont.)

converter output voltage. This non-random error is caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.

The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

Vo (V)	**0.6**	0.9	**1.2**	**1.5**	1.8	2.5	3.3
(1-h)/h	**0.2**	0.8	**1.4**	**2**	2.6	4	5.6
Ro1 (Ohm)	**200**	806	**1.4K**	**2K**	2.61K	4.02K	5.62K
Ro2 (Ohm)	**1K**	1K	**1K**	**1K**	1K	1K	1K

Only the voltages in boldface can be precisely set with standard 1% resistors.
From this table, one may also observe that when the value

$$\frac{1-h}{h} = \frac{V_o - 0.5}{0.5}$$

and its multiples fall into the standard resistor value chart (1%, 5% or so), it is possible to use standard value resistors to exactly set up the required output voltage value.
The input bias current of the error amplifier also causes an error in setting the output voltage. The maximum inverting input bias currents of error amplifiers 1 and 2 is -250nA. Since the non-inverting input is biased to 0.5V, the percentage error in the second output voltage will be $-100\% \cdot (0.25\mu A) \cdot R_{o1}R_{o2}/[0.5 \cdot (R_{o1}+R_{o2})]$. To keep this error below 0.2%, $R_{o2} < 4k\Omega$.

Loop Compensation

SC2446A uses current-mode control for both step-down channels. Current-mode control is a dual-loop control system in which the inductor peak current is loosely controlled by the inner current-loop. The higher gain outer loop regulates the output voltage. Since the current loop makes the inductor appear as a current source, the complex high-Q poles of the output LC networks is split into a dominant pole determined by the output capacitor and the load resistance and a high frequency pole. This pole-splitting property of current-mode control greatly simplifies loop compensation.

The inner current-loop is unstable (sub-harmonic oscillation) unless the inductor current up-slope is steeper than the inductor current down-slope. For stable operation above 50% duty-cycle, a compensation ramp is added to the sensed-current. In the SC2446A the compensation ramp is made duty-ratio dependent. The compensation ramp is approximately

$$I_{ramp} = De^{1.76D} * 30\mu A.$$

The slope of the compensation ramp is then

$$S_e = (1+1.76D)e^{1.76D}f_s * 30\mu A.$$

The slope of the internal compensation ramp is well above the minimal slope requirement for current loop stability and is sufficient for all the applications.
With the inner current loop stable, the output voltage is then regulated with the outer voltage feedback loop. A simplified equivalent circuit model of the synchronous Buck converter with current mode control is shown in Figure 12.

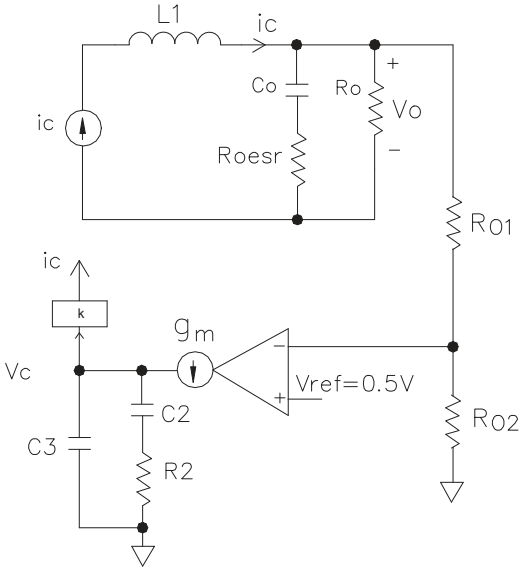


Figure 12. A simple model of synchronous buck converter with current mode control.
The transconductance error amplifier (in the SC2446A) has a gain g_m of 260µA/V. The target of the compensation design is to select the compensation network consisting of C_2, C_3 and R_2, along with the feedback resistors R_{o1},

Application Information (Cont.)

R_{o2} and the current sensing gain, such that the converter output voltage is regulated with satisfactory dynamic performance.

With the output voltage V_o known, the feedback gain h and the feedback resistor values are determined using the equations given in the **"Output Voltage Setting"** section with

$$h = \frac{0.5}{V_o}.$$

For the rated output current I_o, the current sensing gain k is first estimated as

$$k = \frac{I_o}{2.1}.$$

From the transfer function from the voltage error amplifier output v_c to the converter output v_o is

$$\frac{V_o(s)}{V_c(s)} := G_{vc}(s) = kR_o \frac{1+\frac{s}{s_{z1}}}{1+\frac{s}{s_{p1}}}.$$

where, the single dominant pole is

$$s_{p1} = \frac{1}{(R_o + R_{oesr})C_o},$$

and the zero due to the output capacitor ESR is

$$s_{z1} = \frac{1}{R_{oesr}C_o}.$$

The dominant pole moves as output load varies.

The controller transfer function (from the converter output v_o to the voltage error amplifier output v_c) is

$$C(s) = \frac{g_m h}{s(C_2 + C_3)} \frac{1+\frac{s}{s_{z2}}}{1+\frac{s}{s_{p2}}},$$

where

$$s_{z2} = \frac{1}{R_2 C_2},$$

and

$$s_{p2} = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}.$$

The loop transfer function is then

$$T(s) = G_{vc}(s)C(s).$$

To simplify design, we assume that $C_3 << C_2$, $R_{oesr} << R_o$, selects $S_{p1} = S_{z2}$ and specifies the loop crossover frequency f_c. It is noted that the crossover frequency determines the converter dynamic bandwidth. With these assumptions, the controller parameters are determined as following.

$$C_2 = \frac{g_m h k R_o}{2\pi f_c},$$

$$R_2 = \frac{R_o C_o}{C_2},$$

and

$$C_3 = \frac{R_{oesr} C_o}{R_2} K,$$

with a constant K.

For example, if V_o=2.5V, I_o=15A, f_s=300kHz, C_o=1.68mF, R_{oesr}=4.67mΩ, one can calculate that

$$R_o = \frac{V_o}{I_o} = 167\text{m}\Omega,$$

$$h = \frac{0.5}{V_o} = 0.2,$$

and

$$k = \frac{I_o}{2.1} = 7.14.$$

If the converter crossover frequency is set around 1/10 of the switching frequency, f_c = 30kHz, the controller parameters then can be calculated as

$$C_2 = \frac{g_m h k R_o}{2\pi f_c} \approx 0.328\text{nF}.$$

where, gm is the error amplifier transconductance gain (260 $\mu\Omega^{-1}$).

If we use C_2 = 0.33 nF,

$$R_2 = \frac{R_o C_o}{C_2} \approx 848.5\text{k}\Omega,$$

Application Information (Cont.)

use R_2 = 770kΩ.
With K = 1, it is further calculated that

$$C_3 = \frac{R_{oesr} C_o}{R_2} K \approx 10.2pF,$$

use C_3 = 10pF. The Bode plot of the loop transfer function (magnitude and phase) is shown in Figure 13

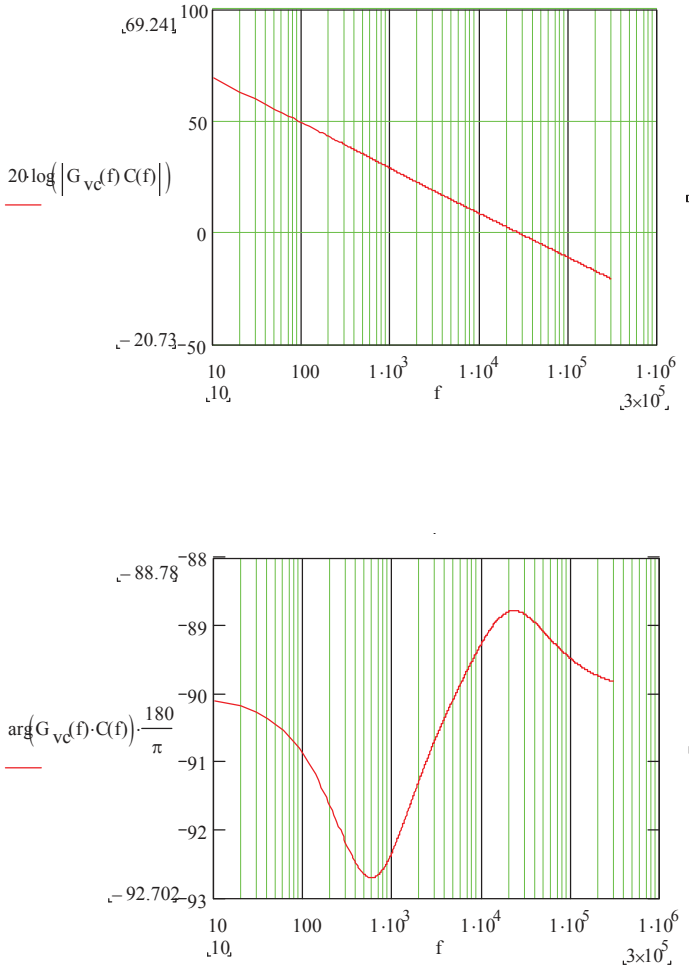


Figure 13. The loop transfer function Bode plot of the example.

It is clear that the resulted crossover frequency is about 27.1 *kHz* with phase margin 91°.

It is noted that the current sensing gain k was first estimated using the DC value in order to quickly get the compensation parameter value. When the circuit is operational and stable, one can further improve the compensation parameter value using AC current sensing gain. One simple and practical method is to effectively measure the output current at two points, e.g. I_{o1} and I_{o2} and the corresponding error amplifier output voltage V_{c1} and V_{c2}. Then, the first order AC gain is

$$k = \frac{\Delta I_o}{\Delta V_c} = \frac{I_{o1} - I_{o2}}{V_{c1} - V_{c2}}$$

With this k value, one can further calculate the improved compensator parameter value using the previous equations.

For example, if one measured that I_{o1}=1A, I_{o2}=15A and V_{c1}=2.139V, V_{c2}=2.457V. k is then calculated as 44. Substituting this parameter to the equations before, one can derive that

$C_2 \approx$ 2.024nF. Select C_2 = 2.2nF.
$R_2 \approx$ 127.3kΩ. Select R_2 = 127kΩ.
$C_3 \approx$ 61.78pF. Select C_3 = 47pF

In some initial prototypes, if the circuit noise makes the control loop jittering, it is suggested to use a bigger C_3 value than the calculated one here. Effectively, the converter bandwidth is reduced in order to reject some high frequency noises. In the final working circuit, the loop transfer function should be measured using network analyzer and compared with the design to ensure circuit stability under different line and load conditions. The load transient response behavior is further tested and measured to meet the specification.

Application Information (Cont.)

PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

Power Stage

1) Separate the power ground from the signal ground. In SC2446A, the power ground PGND should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor.

2) Minimize the size of high pulse current loop. Keep the top MOSFET, bottom MOSFET and the input capacitors within a small area with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

Control Section

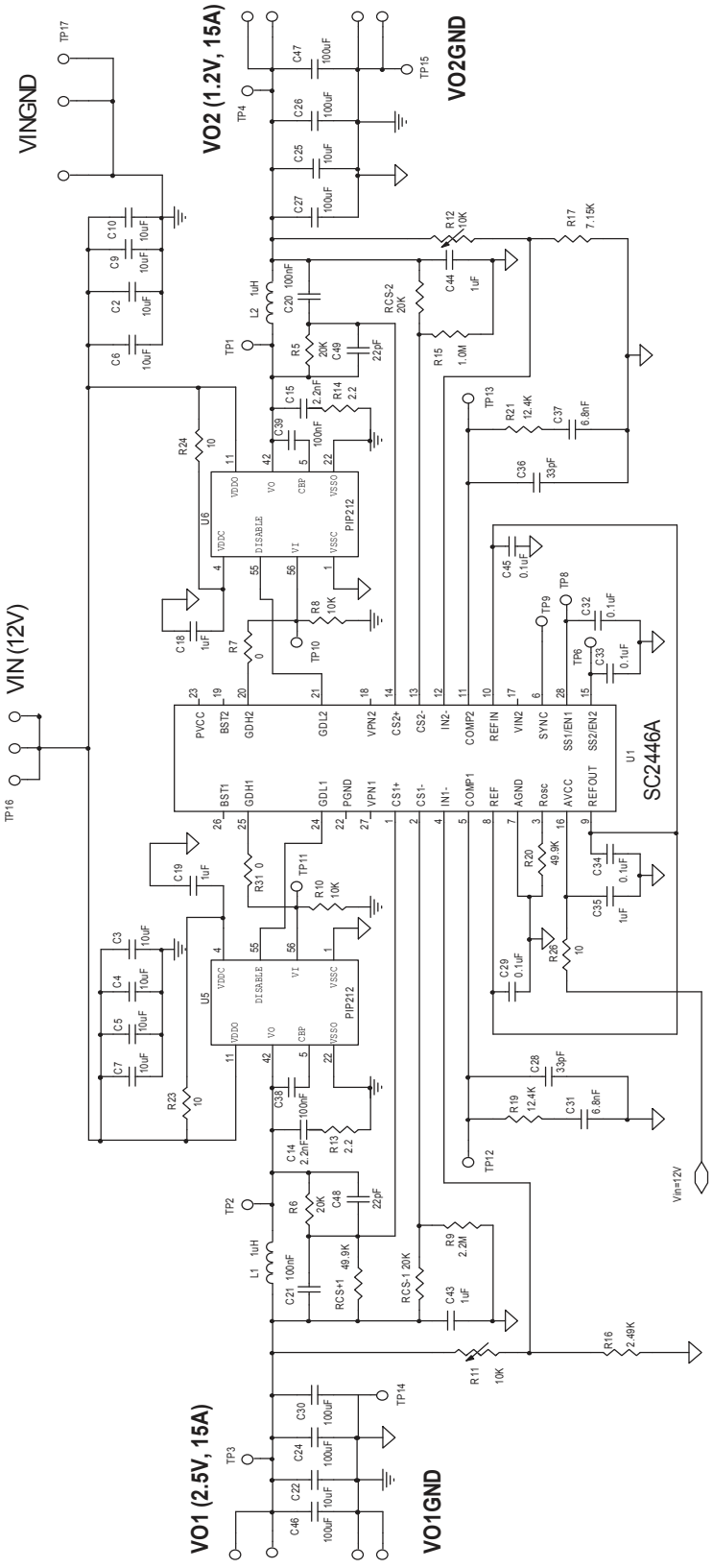
3) The frequency-setting resistor Rosc should be placed close to Pin 3. Trace length from this resistor to the analog ground should be minimized.

4) Solder the bias decoupling capacitor right across the AVCC and analog ground AGND.

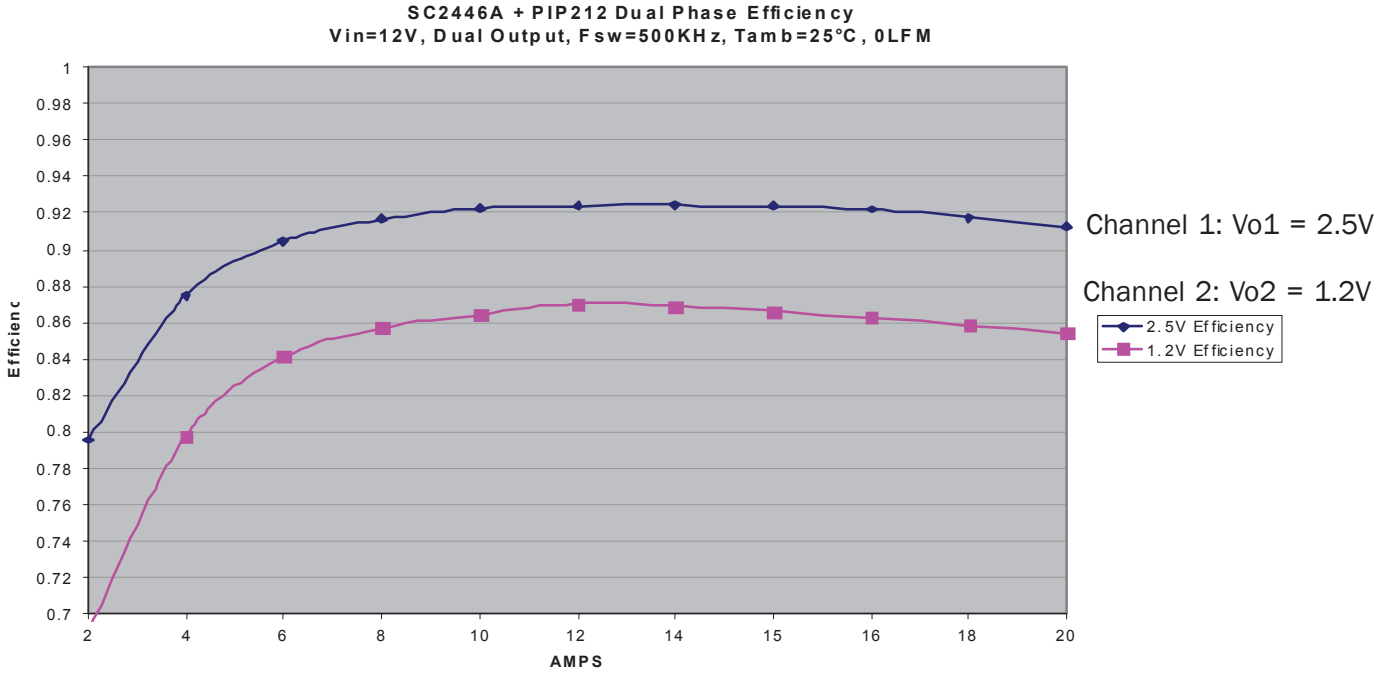
5) Place the Combi-sense components away from the power circuit and close to the corresponding CS+ and CS- pins. Use X7R type ceramic capacitor for the Combi-sense capacitor because of their temperature stability.

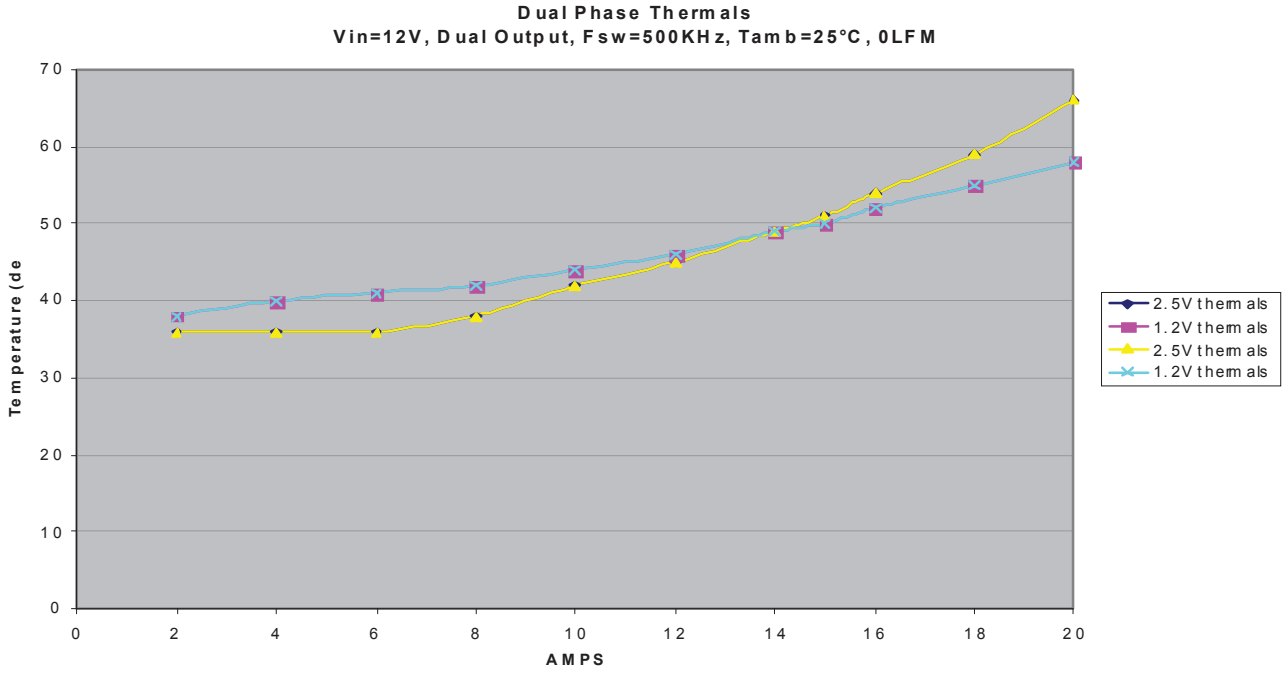
6) Use an isolated local ground plane for the controller and tie it to the negative side of output capacitor bank.

Typical Application Schematic



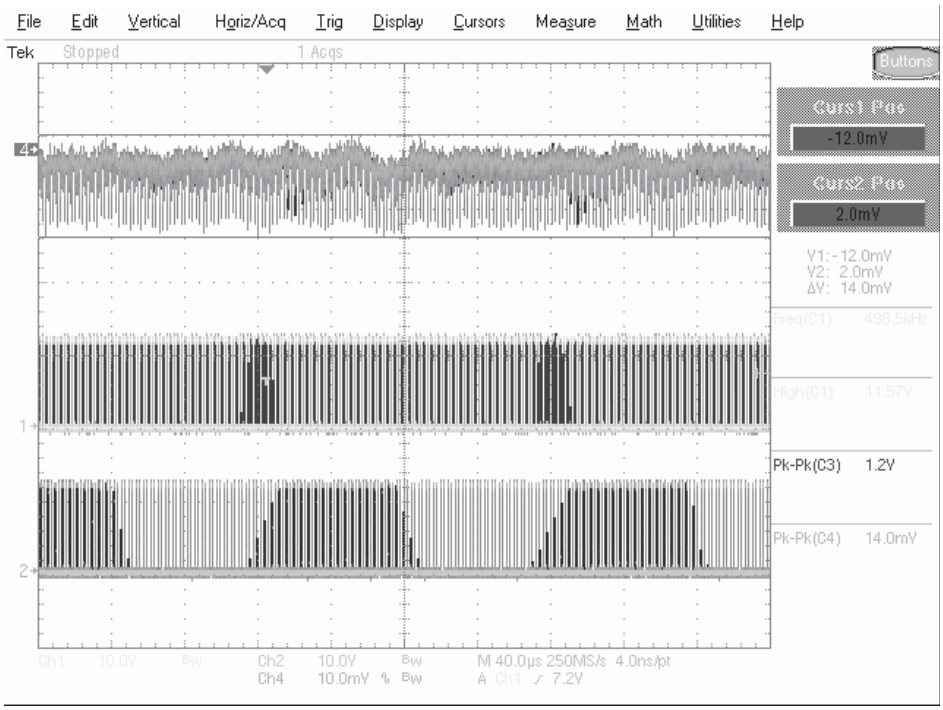
Typical Characteristics



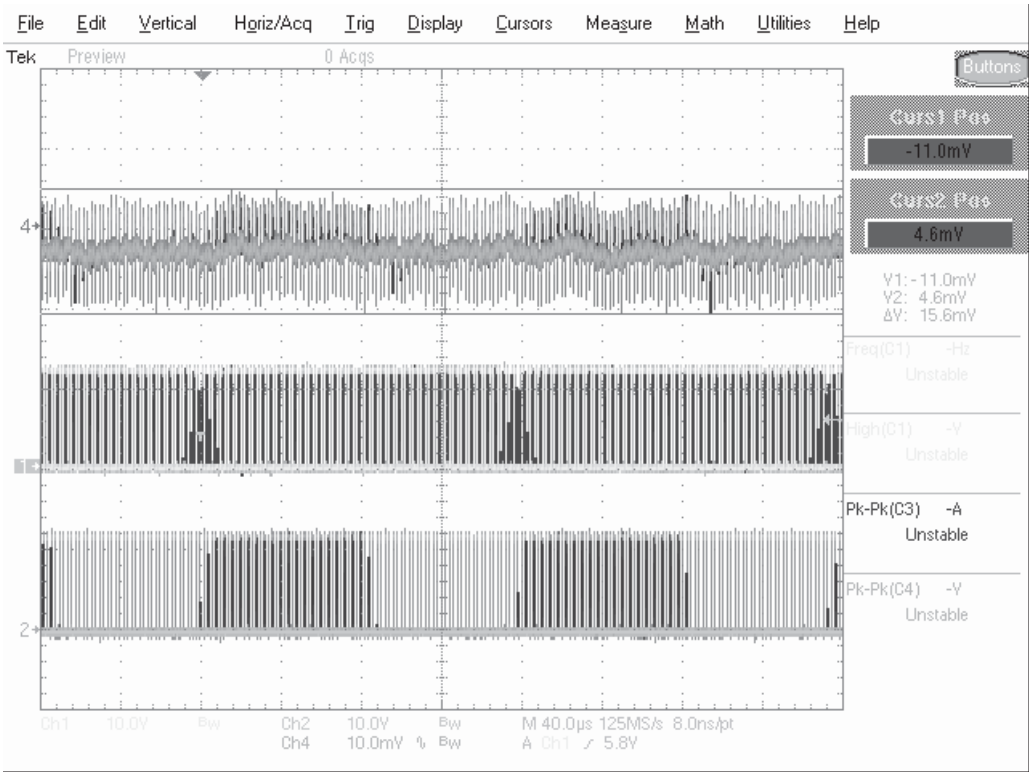


Typical Characteristics (Cont.)

Ch1 (2.5V) Output voltage ripple = 14.0mV p-p

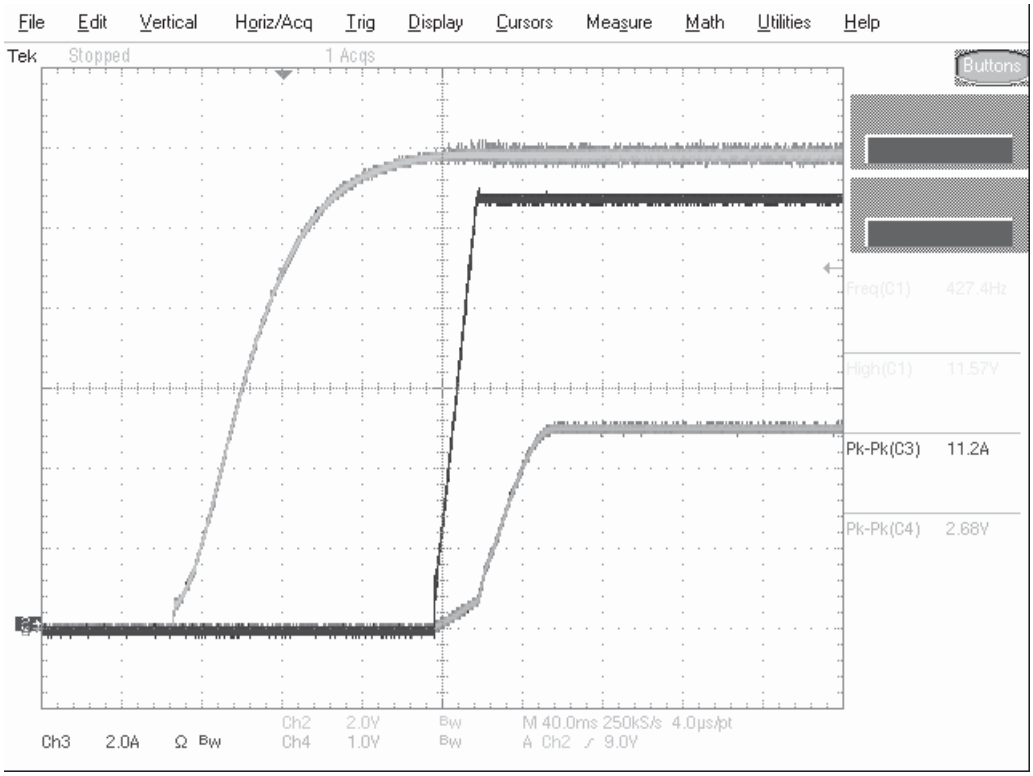


Ch2 (1.2V) Output voltage ripple = 15.6mV p-p



Typical Characteristics (Cont.)

Ch1 (2.5V) Full load start-up

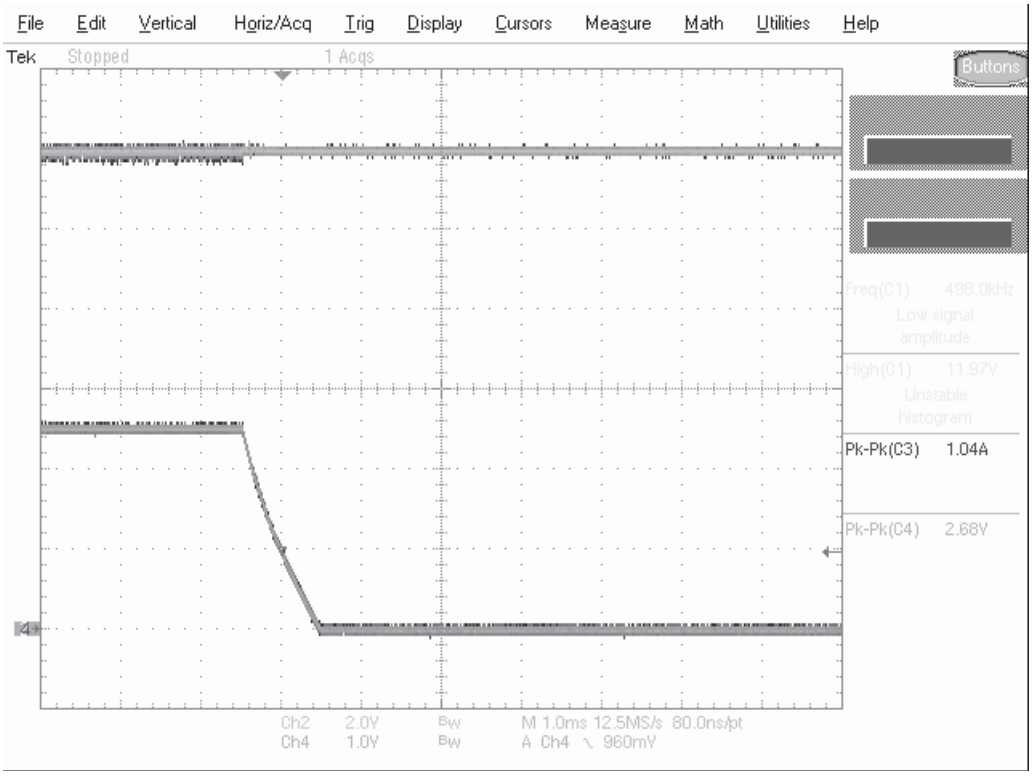


Vin = 12V

Io1

Vout1 = 2.5V

Ch1 (2.5V) Shutdown

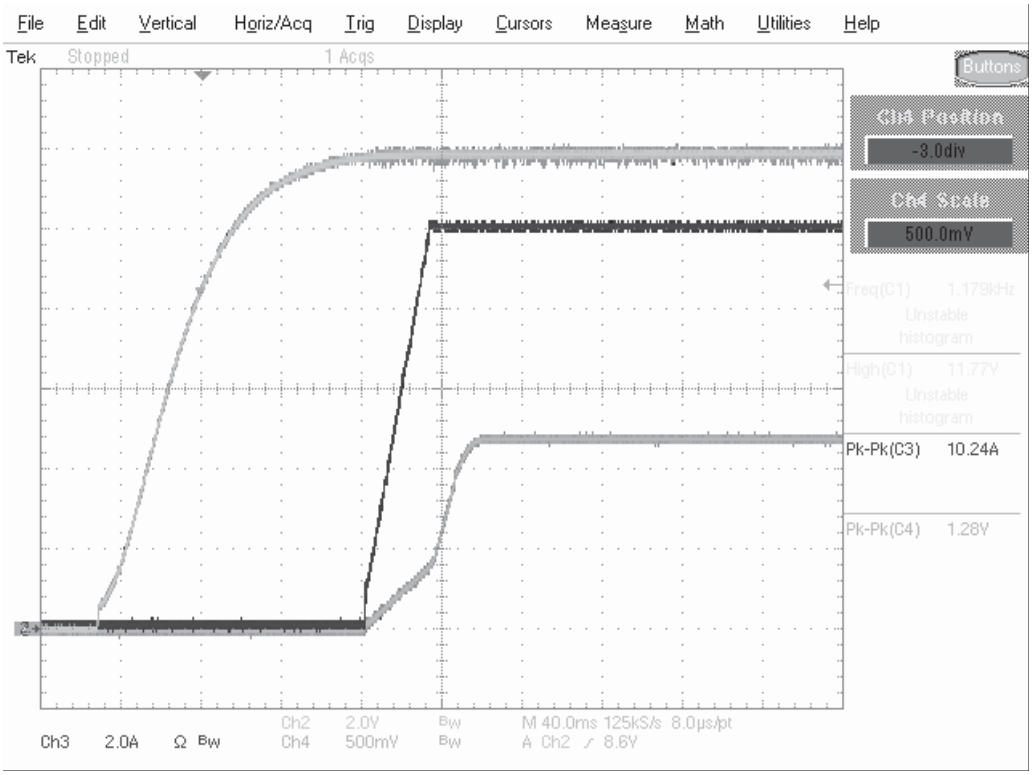


Vin = 12V

Vout1 = 2.5V

Typical Characteristics (Cont.)

Ch2 (1.2V) Full load start-up

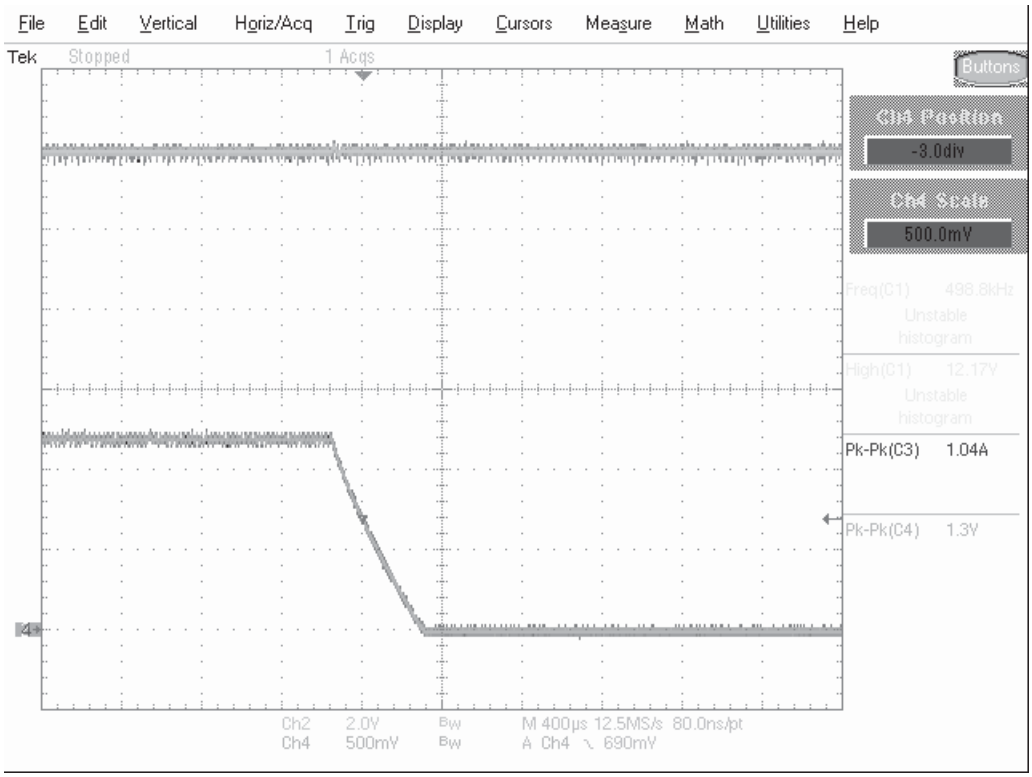


Vin = 12V

Io2

Vout2 = 1.2V

Ch2 (1.2V) Shutdown

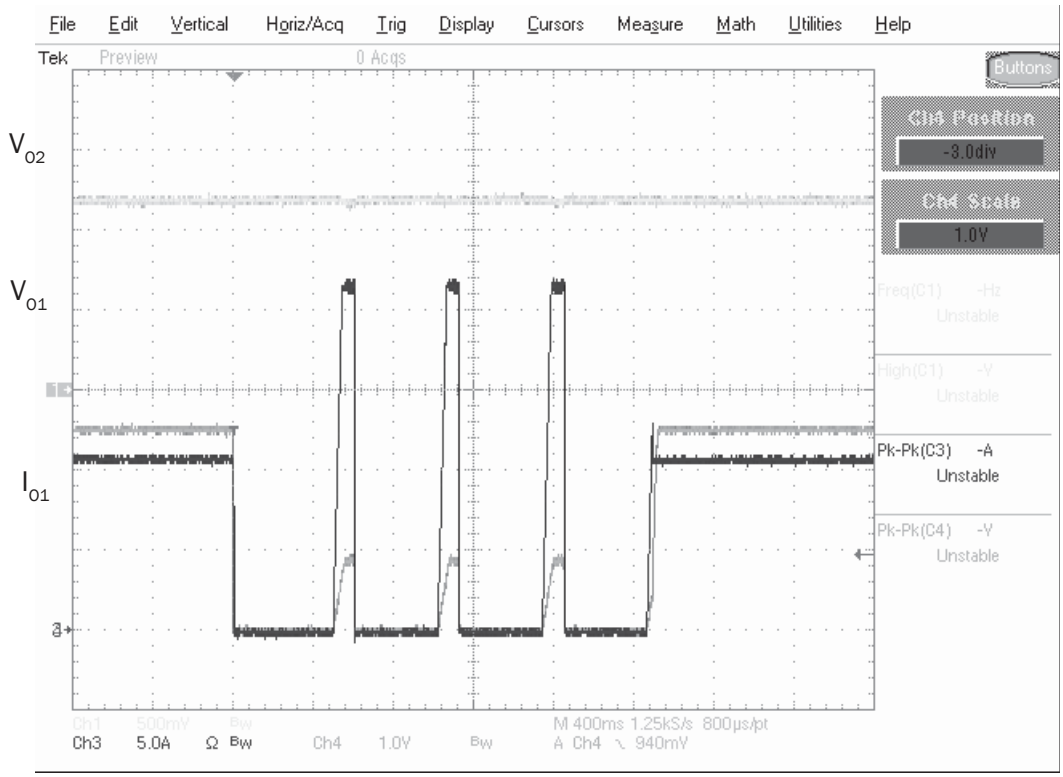


Vin = 12V

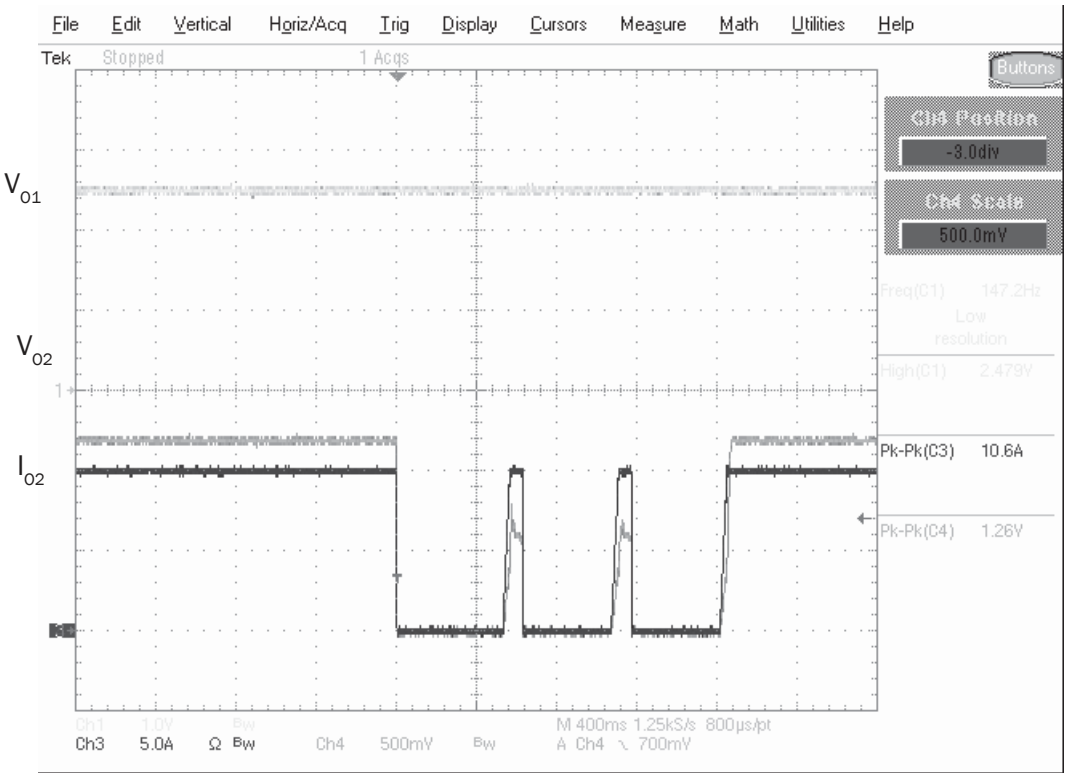
Vout2 = 1.2V

Typical Characteristics (Cont.)

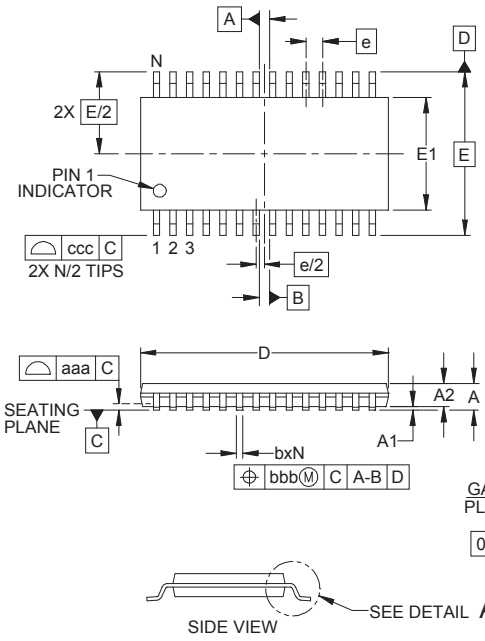
Vin = 12V, Dual output, Fsw = 500KHz, Tamb = 25° C, 0LFM 2.5V Output short and release.



Vin = 12V, Dual output, Fsw = 500KHz, Tamb = 25° C, 0LFM 1.2V Output short and release.



Outline Drawing - TSSOP-28

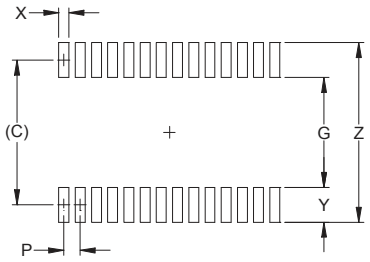


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.378	.382	.386	9.60	9.70	9.80
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	28			28		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AE.

Land Pattern - TSSOP-28



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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