Evaluation Kit Available

Click here to ask an associate for production status of specific part numbers.

Single/Dual/Quad Ultra-Low Input Bias Current, Low-Noise Amplifiers

MAX40079/MAX40087/ MAX40077/MAX40089/ MAX40078

General Description

The MAX40079/MAX40087/MAX40077/MAX40089/ MAX40078 are wide band, low-noise, low-input bias current operational amplifiers that offer rail-to-rail outputs and single-supply operation from 2.7V to 5.5V. These low-noise amps draw 2.2mA of quiescent supply current per amplifier. This family of amplifiers offers ultra-low distortion (0.0002% THD+N), as well as low input voltage-noise density (4.2nV/√Hz) and low input current-noise density (0.5fA/√Hz). The low input bias current of 0.3pA (typ) and low noise(4.5nV/√Hz), together with the wide bandwidth, provides excellent performance for transimpedance (TIA) and imaging applications.

These amplifiers have outputs which swing rail-to-rail and their input common-mode voltage range includes ground. The MAX40079/MAX40077/MAX40078 are single/dual/quad respectively in unity-gain stable with a bandwidth of 10MHz. The MAX40087/MAX40089 are single/dual respectively with gain ≥ 5 stable and bandwidth of 42MHz. They operate over the full -40°C to +125°C temperature range.

Single channel op amps are available in 6-bump wafer-level package (WLP) and SOT23 6-pin packages. The dual channel op amps are available in 8-bump WLP and µMAX-8 packages. The quad channel option is available in 14-TSSOP package.

Applications

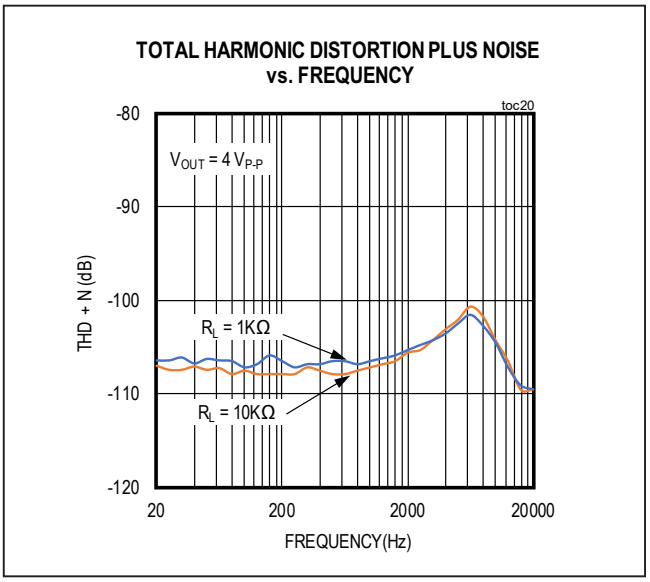
- Transimpedance Amplifiers
- pH Probes and Reference Electrodes
- ADC Buffers
- DAC Output Amplifiers
- Low-Noise Microphone/Preamplifiers
- Digital Scales
- Strain Gauges/Sensor Amplifiers
- Medical Instrumentation

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Low Input Voltage Noise Density: 4.2nV/√Hz at 30KHz
- Low Input Current Noise Density: 0.5fA/√Hz
- Low Input Bias Current: 0.3pA (typ)
- Low Distortion: 0.00035% or -109dB THD+N (1kΩ Load)
- Single-Supply Operation from +2.7V to +5.5V
- Input Common-Mode Voltage Range Includes Ground
- Rail-to-Rail Output Swings with a 1kΩ Load
- Wide Bandwidth: MAX40079/MAX40077/MAX40078 (10MHz); MAX40087/MAX40089 (42MHz)
- Excellent DC Characteristics: V_{OS} ≤ 30µV
- Single-Channel 6-bump WLP in 1.31mm x 0.73mm with 0.35mm Bump Pitch
- Dual-Channel 8-bump WLP in 0.96mm x 1.66mm with 0.35mm Bump Pitch
- Available in Space-Saving 6-WLP, 6-SOT, 8-WLP and µMAX Packages

THD+N Performance



19-100237; Rev 10; 10/21

Absolute Maximum Ratings

Input Differential Voltage(IN+ - IN-)
MAX40079/MAX40087/MAX40077/MAX40089/MAX40078 (continuous).....-3V to +3V
MAX40079/MAX40087/MAX40077/MAX40089/MAX40078 (transient, 10s).....-6V to +6V
Power-Supply Voltage (V_{DD} to V_{SS}).....-0.3V to +6V
Analog Input Voltage ((IN+,IN-) to V_{SS}).....V_{SS} - 0.3V to V_{DD} + 0.3V
$\overline{SHDN}$ Input Voltage (to V_{SS}).....V_{SS} - 0.3V to +6V
Continuous Input Current (IN+,IN-).....±20mA
Output Short-Circuit Duration to Either Supply .....Continuous

Operating Temperature Range..... -40°C to +125°C
Continuous Power Dissipation (T_A = +70°C)
SOT23-6 (derate 8.7mW/°C above +70°C).....696mW
6-Bump WLP (derate 10.19mW/°C above +70°C).....815mW
8-µMAX (derate 4.8mW/°C above +70°C) 387.80mW
8-Bump WLP (derate 10.90mW/°C above +70°C).....872mW
14-TSSOP (derate 10mW/°C above +70°C).....796.80mW
Storage Temperature Range..... -65°C to +150°C
Lead Temperature ((soldering, 10s)).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6-SOT23

PACKAGE CODE	U6+1
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	115°C/W
Junction to Case (θ_{JC})	80°C/W

6-WLP

PACKAGE CODE	N60F1+1
Outline Number	21-100174
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	98.06°C/W
Junction to Case (θ_{JC})	N/A

8-µMAX

PACKAGE CODE	U8+1
Outline Number	21-0036
Land Pattern Number	90-0092
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	221°C/W
Junction to Case (θ_{JC})	42°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	206.30°C/W
Junction to Case (θ_{JC})	42°C/W

Package Information (continued)

8-WLP

PACKAGE CODE	N80C1+1
Outline Number	21-100236
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	91.72°C/W
Junction to Case (θ_{JC})	N/A

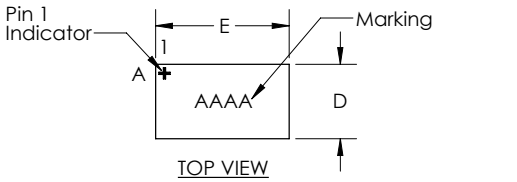
14-TSSOP

PACKAGE CODE	U14M+1
Outline Number	21-0066
Land Pattern Number	90-0113
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	110°C/W
Junction to Case (θ_{JC})	30°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	100.4°C/W
Junction to Case (θ_{JC})	30°C/W

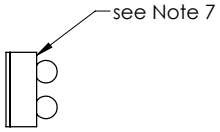
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

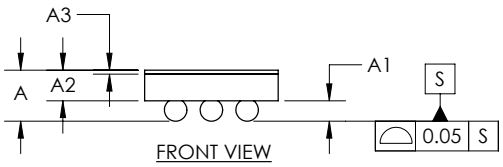
Package Information (continued)



TOP VIEW

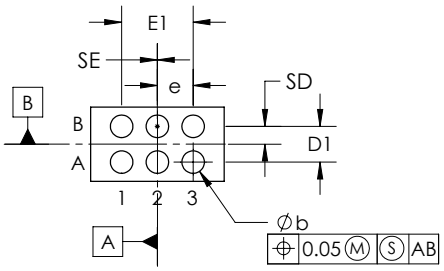


SIDE VIEW



FRONT VIEW

COMMON DIMENSIONS	
A	0.50 MAX
A1	0.17 ±0.03
A2	0.30 REF
A3	0.040 BASIC
b	∅0.22 ±0.03
D	0.727 ±0.025
E	1.308 ±0.025
D1	0.35 BASIC
E1	0.70 BASIC
e	0.35 BASIC
SD	0.175 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

maxim integrated™

TITLE
PACKAGE OUTLINE 6 BUMPS
THIN WLP PKG. 0.35 mm PITCH,N60F1+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100174	A	1/1

Electrical Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 2.5V, $\overline{SHDN}$ = V_{DD}, V_{OUT} = V_{DD}/2, R_L = 10kΩ = tied to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR test	2.7		5.5	V
Quiescent Supply Current, per Amplifier	I_{DD}	V_{DD} = 3.3V (T_A = 25°C only)		2.2	2.9	mA
		V_{DD} = 5V, over temperature to 125°C		2.5	3.8	
Power-Up Time		V_{DD} = 0 to 5V step, V_{OUT} = 2.5V ±1%		13		µs
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ function only for Single Versions (MAX40079/MAX40087)		0.4		µA
Input Offset Voltage	V_{OS}	at 25°C		30	350	µV
		Over the full temperature range			750	
Input Offset Drift	V_{OS}-TC	Over temperature, to 125°C		0.3	6	µV/°C
Input Bias Current (Note 2)	I_B			0.3	260	pA
Input Offset Current (Note 2)	I_{OS}			0.1	150	pA
Input Resistance	R_{IN}			1000		GΩ
Input Capacitance	C_{IN}	Either input, over entire CMIR		7		pF
Input Common Mode Range	V_{IN+}, V_{IN-}	Guaranteed by CMRR test at 25°C	-0.2		V_{DD} - 1.5	V
		Guaranteed by CMRR test, -40°C to +125°C	-0.1		V_{DD} - 1.5	
Common Mode Rejection Ratio	CMRR	DC, -0.2V < V_{IN+}, V_{IN-} < V_{DD} - 1.5V, at 25°C	90	120		dB
		DC, -0.1V < V_{IN+}, V_{IN-} < V_{DD} - 1.5V, -40°C to +125°C	87			
		AC, 100mV_{PP} at 10kHz, DC in 0V to V_{DD} - 2V range		60		
Power Supply Rejection Ratio, DC	PSRR	DC, 2.7V < V_{DD} < 5.5V	90	120		dB
Power Supply Rejection Ratio, AC	PSRR	AC, 100mV_{PP} at 1MHz with V_{DD} = 5V DC offset		40		dB
Open-Loop Gain	A_{OL}	R_L = 10KΩ to V_{DD}/2, V_{OUT} = 200mV to V_{DD} - 250mV	90	120		dB
		R_L = 1kΩ to V_{DD}/2, V_{OUT} = 200mV to V_{DD} - 250mV	85	110		
		R_L = 50Ω to V_{DD}/2, V_{OUT} = 200mV to V_{DD} - 250mV	85	110		
Output Voltage Swing High (V_{OH})	V_{DD}-V_{OH}	R_L = 10KΩ to V_{DD}/2, V_{DD} - V_{OH}		10	45	mV
		R_L = 1KΩ to V_{DD}/2, V_{DD} - V_{OH}		80	200	
		R_L = 500Ω to V_{DD}/2, V_{DD} - V_{OH}		100	300	
Output Voltage Swing Low (V_{OL})	V_{OL}	R_L = 10KΩ to V_{DD}/2, V_{OL} - V_{SS}		10	40	mV
		R_L = 1KΩ to V_{DD}/2, V_{OL} - V_{SS}		50	150	
		R_L = 500Ω to V_{DD}/2, V_{OL} - V_{SS}		80	250	

Electrical Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 2.5V, $\overline{SHDN}$ = V_{DD}, V_{OUT} = V_{DD}/2, R_L = 10kΩ = tied to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Short-Circuit Current	I_{SC}	To either V_{DD} or V_{SS}		50		mA
Gain Bandwidth Product	GBWP	Unity Gain, A_V = +1 (MAX40079/MAX40077/MAX40078)		10		MHz
		Min Gain version, A_V = +5 (MAX40087/MAX40089)		42		
Phase Margin	Φ_m	Unity Gain version, A_V = +1		70		°
		Minimum Gain, A_V = +5 version		80		
Gain Margin	GM			12		dB
Slew Rate	SR	Unity Gain version, A_V = +1		3		V/µs
		Minimum Gain, A_V = +5 version		10		
Settling Time		Unity gain version, A_V = +1, to 0.01%, V_{OUT} = 2V step		2		µs
		Minimum gain, A_V = +5, to 0.01%, V_{OUT} = 2V step		2		
Stable Capacitive Load	C_{LOAD}	No sustained oscillation		50		pF
Integrated 1/f Input Voltage Noise	V*n*	0.1Hz to 10Hz		1.7		μV_{PP}
Input Voltage Noise Density	e_N	f = 10Hz		260		$nV/\sqrt{Hz}$
		f = 1kHz		5.5		
		f = 30kHz		4.2		
Input Current Noise density	i_N	f = 1kHz		0.5		$fA/\sqrt{Hz}$
Total Harmonic Distortion + Noise (A_V = +1 stable)	THD+N	Unity gain, A_V = +1, V_{OUT} = $4V_{PP}$ at 1kHz, R_L = 10kΩ to GND		114		dB
		Unity gain, A_V = +1, V_{OUT} = $4V_{PP}$ at 20kHz, R_L = 10kΩ to GND		103		
		Unity gain, A_V = +1, V_{OUT} = $4V_{PP}$ at 1kHz, R_L= 1kΩ to GND		114		
		Unity gain, A_V = +1, V_{OUT} = $4V_{PP}$ at 20kHz, R_L= 1kΩ to GND		100		
Total Harmonic Distortion + Noise (Min A_V = +5 stable)	THD+N	Unity gain, A_V = +5, V_{OUT} = $4V_{PP}$ at 1kHz, R_L = 10kΩ to GND		108		dB
		Unity gain, A_V = +5, V_{OUT} = $4V_{PP}$ at 20kHz, R_L = 10kΩ to GND		110		
		Unity gain, A_V = +5, V_{OUT} = $4V_{PP}$ at 1kHz, R_L = 1kΩ to GND		106		
		Unity gain, A_V = +5, V_{OUT} = $4V_{PP}$ at 20kHz, R_L = 1kΩ to GND		110		
ElectroMagnetic Interference Rejection Ratio	EMIRR	V_{RF_PP} = 100mV, f_{IN} = 2400MHz		55		dB

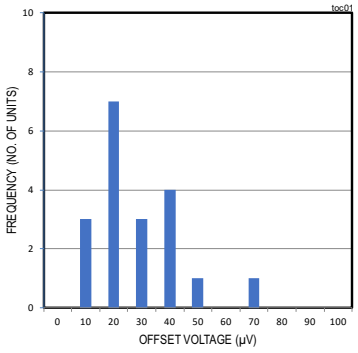
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design and bench characterization.

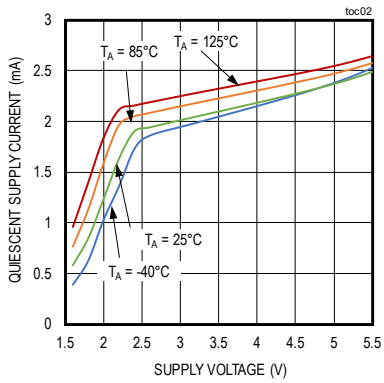
Typical Operating Characteristics

V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, C_L = 10pF to GND, T_A = +25°C, unless otherwise noted. (T_A = +25°C, unless otherwise noted.)

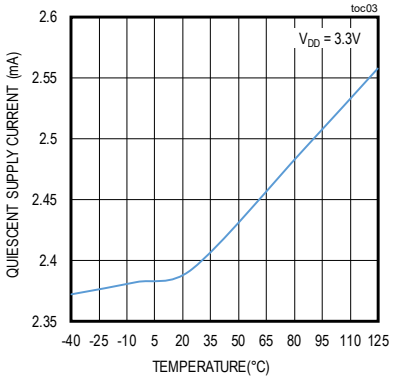
OFFSET VOLTAGE HISTOGRAM



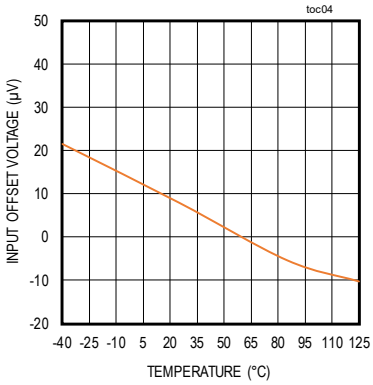
SUPPLY CURRENT vs. SUPPLY VOLTAGE



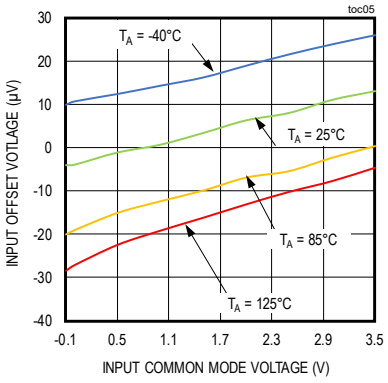
SUPPLY CURRENT vs. TEMPERATURE



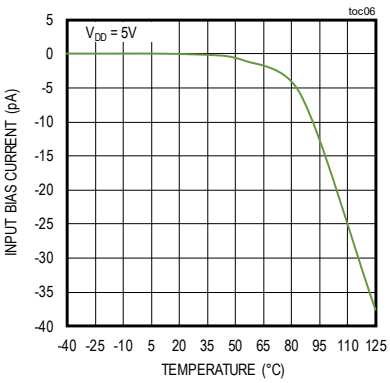
INPUT OFFSET VOLTAGE vs. TEMPERATURE



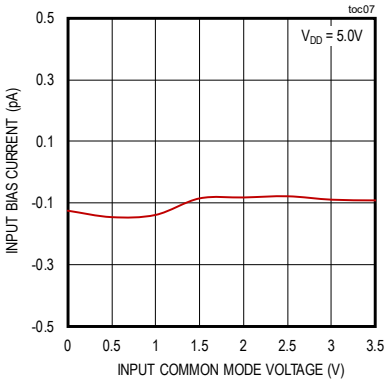
INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE VOTLAGE



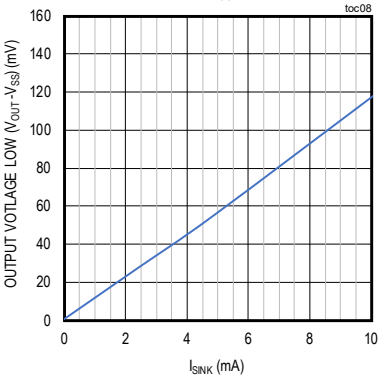
INPUT BIAS CURRENT vs. TEMPERATURE



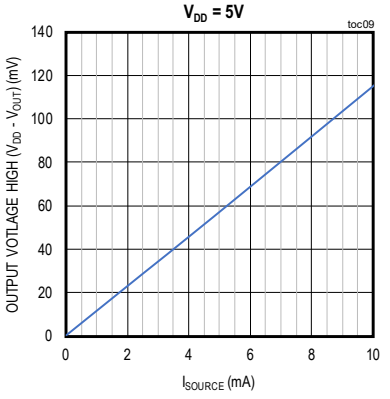
INPUT BIAS CURRENT vs. INPUT COMMON MODE VOLTAGE



OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT
V_{DD} = 5V, V_{SS} = 0V



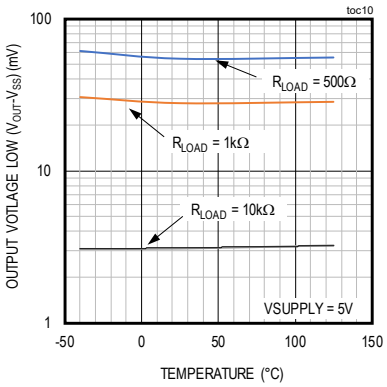
OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT
V_{DD} = 5V



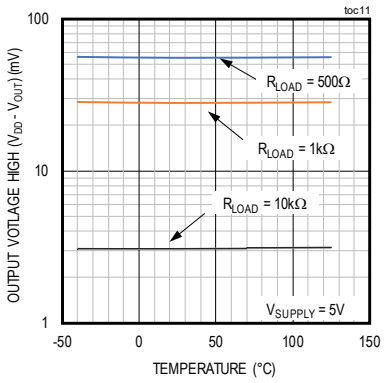
Typical Operating Characteristics (continued)

V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, C_L = 10pF to GND, T_A = +25°C, unless otherwise noted. (T_A = +25°C, unless otherwise noted.)

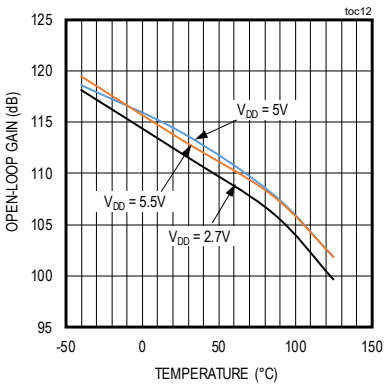
OUTPUT VOLTAGE LOW vs. TEMPERATURE



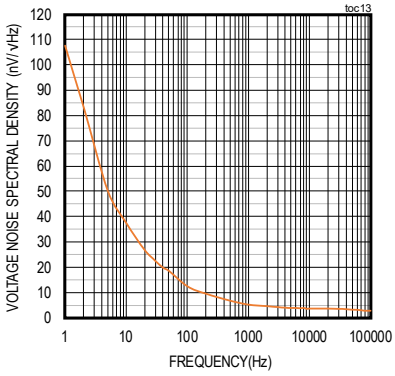
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



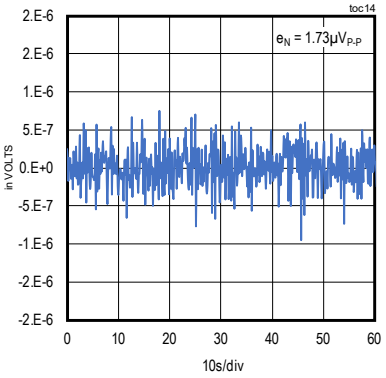
OPEN-LOOP GAIN vs. TEMPERATURE



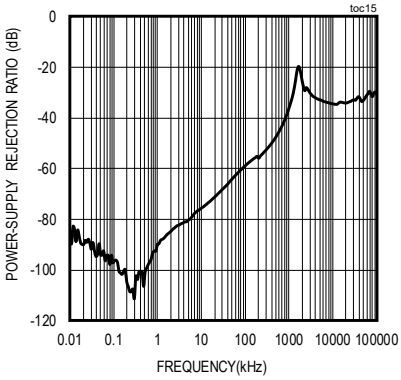
VOLTAGE NOISE DENSITY vs. FREQUENCY



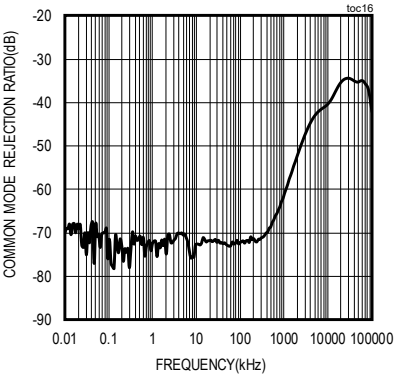
INPUT VOLTAGE NOISE 0.1Hz TO 10Hz NOISE



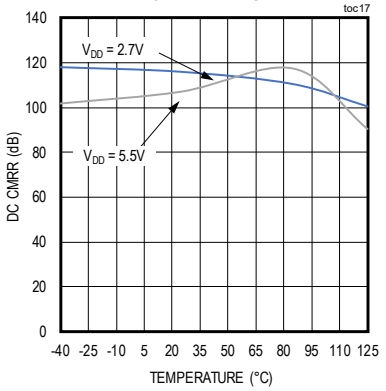
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



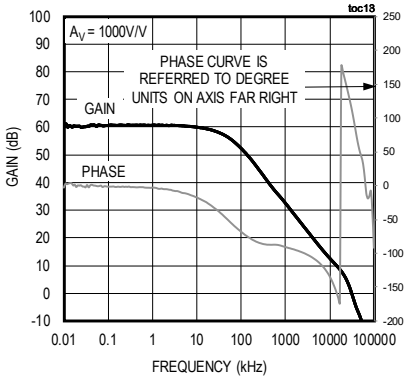
COMMON MODE REJECTION RATIO vs. FREQUENCY



COMMON MODE REJECTION RATIO vs. TEMPERATURE



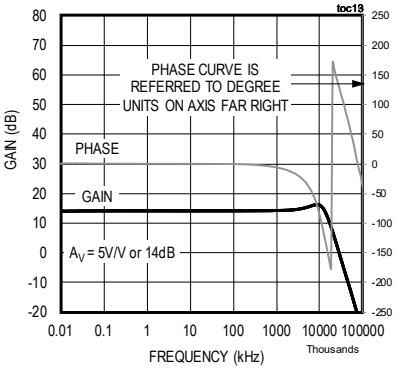
GAIN AND PHASE vs. FREQUENCY (R_L = 10kΩ, C_L = 10pF)



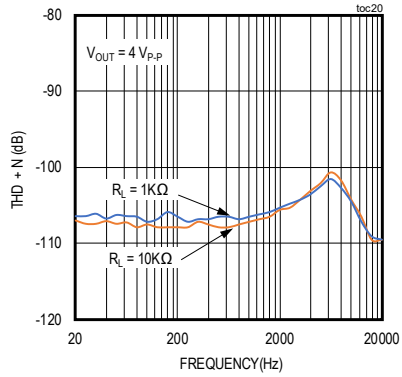
Typical Operating Characteristics (continued)

V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, C_L = 10pF to GND, T_A = +25°C, unless otherwise noted. (T_A = +25°C, unless otherwise noted.)

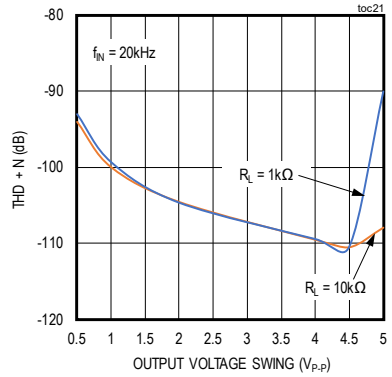
GAIN AND PHASE vs. FREQUENCY
(R_L = 10kΩ, C_L = 10pF)



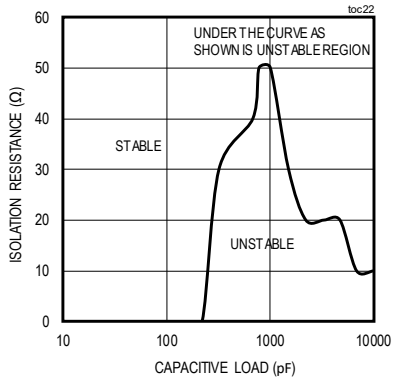
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. FREQUENCY



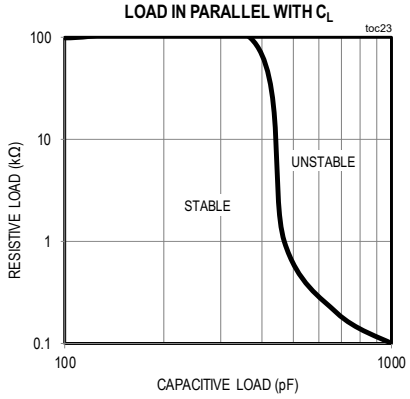
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. OUTPUT VOLTAGE SWING



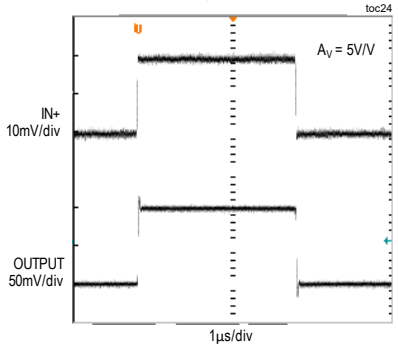
ISOLATION RESISTANCE
vs. CAPACITIVE STABILITY



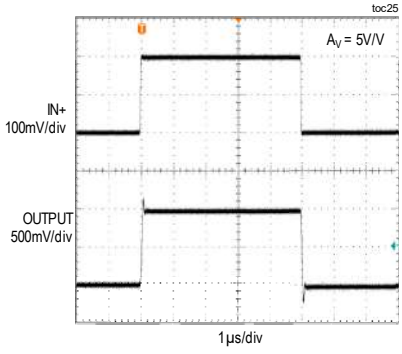
STABILITY vs. CAPACITIVE AND RESISTIVE
LOAD IN PARALLEL WITH C_L



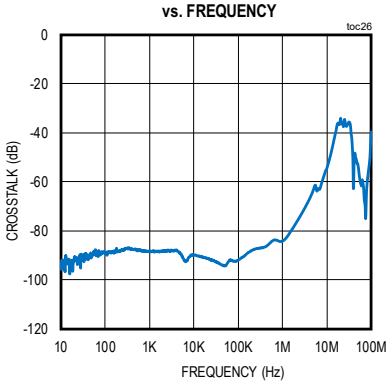
SMALL-SIGNAL PULSE RESPONSE
(C_{LOAD}= 10pF)



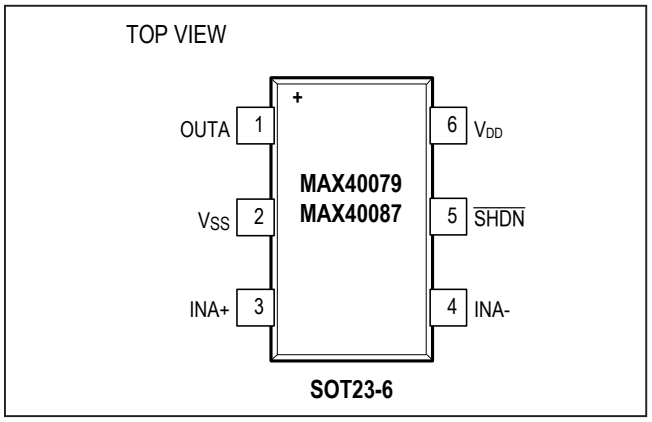
LARGE-SIGNAL PULSE RESPONSE
(C_L = 10pF)

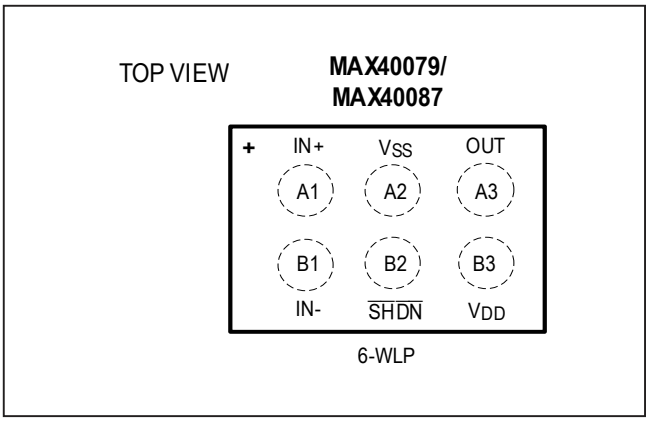


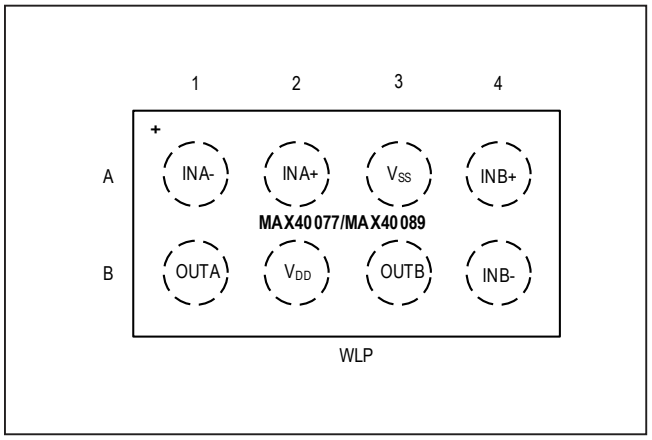
CROSSTALK
vs. FREQUENCY

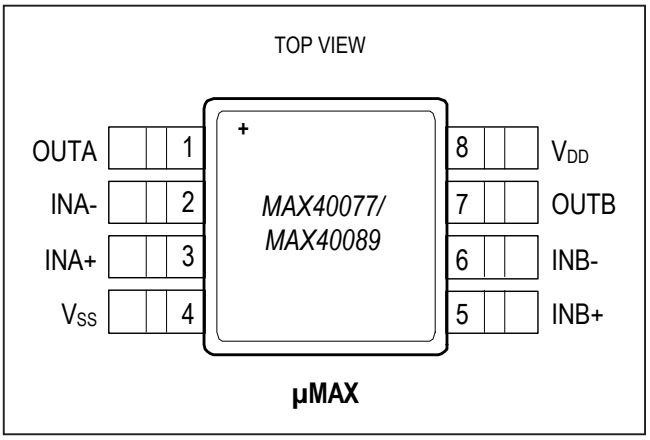


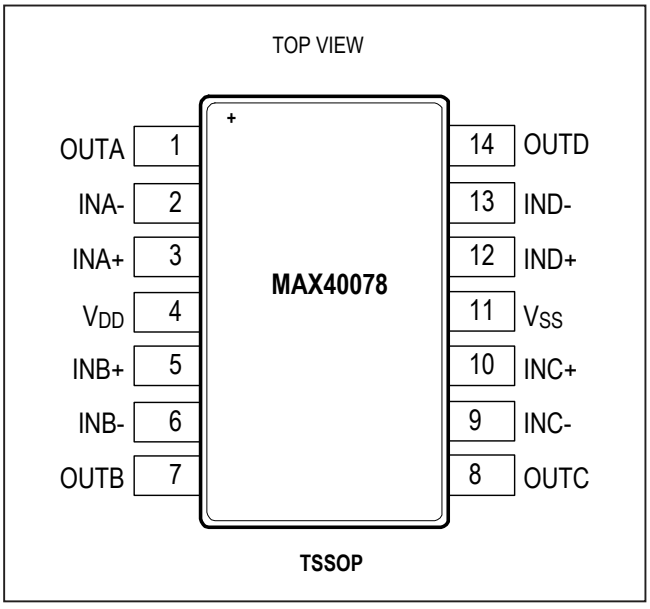
Pin Configurations









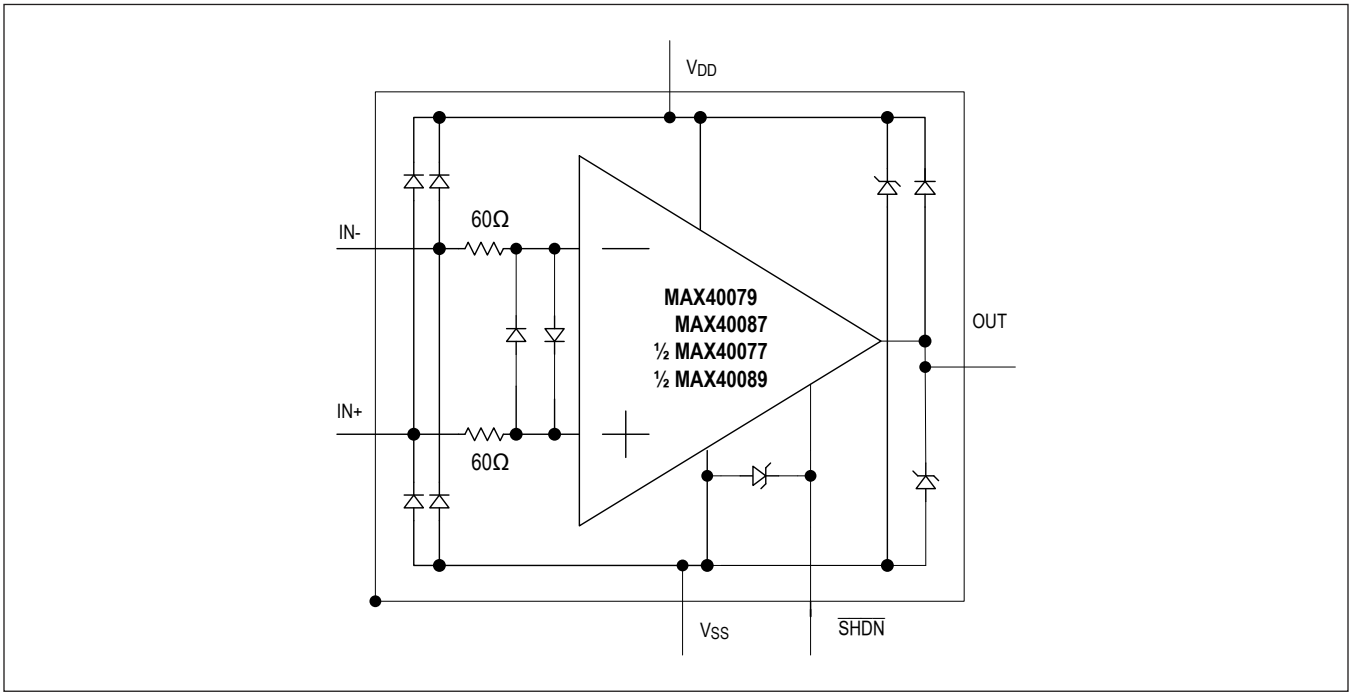


Pin Description

PIN					NAME	FUNCTION
SOT23-6	6-WLP	8-WLP	8-MMAX	14-TSSOP		
1	A3	B1	1	1	OUTA	Output, Channel A
2	A2	A3	4	11	V_{SS}	Negative Power Supply Input. Connect V_{SS} to 0V in single-supply application.
3	A1	A2	3	3	INA+	Non-Inverting Input, Channel A
4	B1	A1	2	2	INA-	Inverting Input, Channel A
5	B2	—	—	—	$\overline{SHDN}$	Shutdown. Pull high for normal operation and low for shutdown
6	B3	B2	8	4	V_{DD}	Positive Power Supply Voltage Input
—	—	A4	5	5	INB+	Noninverting Input, Channel B
—	—	B4	6	6	INB-	Inverting Input, Channel B
—	—	B3	7	7	OUTB	Output, Channel B
—	—	—	—	10	INC+	Noninverting Input, Channel C
—	—	—	—	9	INC-	Inverting Input, Channel C
—	—	—	—	8	OUTC	Output, Channel C
—	—	—	—	12	IND+	Noninverting Input, Channel D
—	—	—	—	13	IND-	Inverting Input, Channel D
—	—	—	—	14	OUTD	Output, Channel D

Functional Diagram

Internal ESD Protection



Detailed Description

The MAX40079/MAX40087/MAX40077/MAX40089/MAX40078 single/dual/quad channel operational amplifiers feature ultra-low noise and distortion. Their low distortion and low noise make them ideal for use as pre-amplifiers in wide dynamic range applications, such as 16-bit analog-to-digital converters. Their high input impedance and low noise are also useful for signal conditioning of high-impedance sources, such as piezoelectric transducers.

These devices have true rail-to-rail output operation, drive output resistive loads as low as 1kΩ while maintaining DC accuracy and can drive capacitive loads up to 200pF without any oscillation. The input common-mode voltage range extends from 0.2V below V_{SS} to (V_{DD} - 1.5V). The push-pull output stage maintains excellent DC characteristics, while delivering up to ±20 mA of source/sink output current.

The MAX40079/MAX40079/MAX40078 are single/dual/quad respectively that are unity-gain stable, while the MAX40087/MAX40089, single/dual respectively are decompensated version having higher slew rate and are stable for Gain ≥ 5V/V. The MAX40079/MAX40087 single channel op amps feature a low-power shutdown mode, which reduces the supply current to 0.1µA and places amplifiers outputs into a high impedance state.

Low Noise

The amplifiers input-referred voltage noise density is dominated by flicker noise(also known as 1/f noise) at lower frequencies and by thermal noise at higher frequencies. Overall thermal noise contribution is affected by the parallel combination of resistive feedback network ($R_F||R_G$) depicted in Figure 1. These resistors should be reduced in cases where system bandwidth is large and thermal noise is dominant. Noise contribution factor can be reduced with increased gain settings.

For example, the input noise voltage density (e_N) of the circuit with R_F = 100kΩ, R_G = 10kΩ with Gain = 11V/V non-inverting configuration is e_N = 12nV/√Hz.

e_N can be reduced to 6nV/√Hz by choosing R_F = 10kΩ, smaller R_G = 1kΩ compared to 10kΩ with still same Gain = 11V/V but at the expense of higher current consumption and higher distortion. Noise of this circuit is effectively reduced due to smaller value of R_G that dominates system noise.

Having a Gain of 101V/V with R_F = 100kΩ, R_G = 1kΩ, input referred voltage noise density is still a low 6nV/√Hz as the noise dominating resistor R_G remained the same.

Low Distortion

Many factors can affect the noise and distortion performance of the amplifier based on the design choices made. The following guidelines offer valuable information on the impact of design choices on total harmonic distortion (THD). Choosing correct feedback and gain resistor values for a particular application can be a very important factor in reducing THD. In general, the smaller the closed-loop gain, the smaller the THD generated, especially when driving heavy resistive loads (in other words, smaller resistive load with higher output current). Operating the device near or above the full-power bandwidth significantly degrades distortion.

Referencing the load to either supply also improves the amplifier distortion performance, because only one of the MOSFETs of the push-pull output stage drives the output. Referencing the load to mid-supply increases the amplifier distortion for a given load and feedback setting (See the *Total Harmonic Distortion vs. Frequency* graph in the *Typical Operating Characteristics*).

For gains ≥ 5V/V, the de-compensated MAX40087/MAX40089 deliver the best distortion performance as they have a higher slew rate and provide a higher amount of loop gain for a given closed-loop gain setting. Capacitive loads below 100pF do not significantly affect distortion results. Distortion performance is relatively constant over supply voltages.

Input Protection

As per **Functional Diagram**, when voltage on either of the input pins goes up or below V_{DD} or V_{SS} by more than a diode voltage drop, ESD diodes begin to turn-on/forward bias and large amount of current flow through these diodes. If op amp inputs in certain applications are subject to these over-voltage conditions, insert a series current limiting 50 ohm resistors on either inputs. However, note that DC precision of the system be affected due to these series resistors and also thermal noise of these resistors need to be considered while making noise analysis of the entire circuit.

An input differential protection scheme is used (refer to **Functional Diagram**) that protect the device if there is a large differential voltage applied across input pins. A series of 60Ω resistors are used in conjunction with a pair of back to back diodes that turn on in an event of differential voltage beyond a diode drop. A pair of 60Ω resistors limit current flowing through these diodes so that the current is limited below abs max rating of ±20mA.

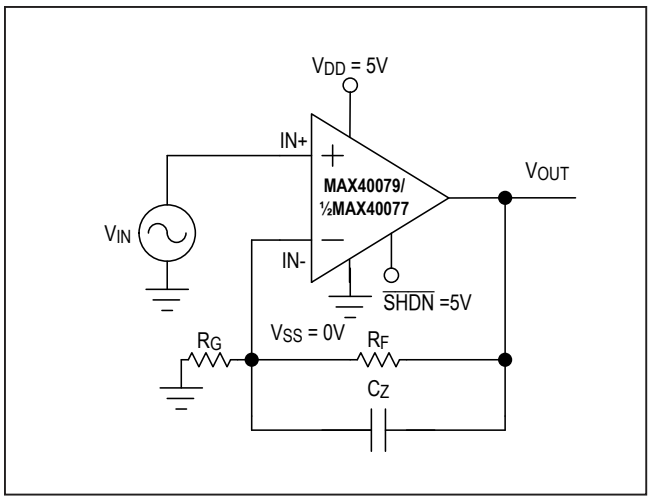


Figure 1. Adding Feed-Forward Compensation

Since there is a differential protection scheme used in these family of op amps, these amplifiers cannot be used as comparators in open loop, which is often a possibility on an unused channel of op amp.

Using a Feed-Forward Compensation Capacitor, C_Z

The amplifier's input capacitance is 7pF and if the resistance seen by the inverting input is large (Figure 1) as a result of feedback network, this resistance and capacitance combination can introduce a pole within the amplifier's bandwidth resulting in reduced phase margin. Compensate the reduced phase margin by introducing a feed-forward capacitor (C_Z) between the inverting input and the output (shown in Figure 1). This effectively cancels the pole from the inverting input of the amplifier. Choose the value of C_Z as follows:

$$C_Z = 10 \times (R_F/R_G)\ [pF]$$

In the unity-gain stable: MAX40079/MAX40077/MAX40078, the use of correct value C_Z is most important for closed loop non-inverting gain A_V = +2V/V, and inverting gain A_V = -1V/V.

In the de-compensated MAX40087/MAX40089, C_Z is most important for closed loop gain A_V = +10V/V.

Using a slightly smaller C_Z than suggested by the formula above achieves a higher bandwidth at the expense of reduced phase and gain margin. As a general guideline, consider using C_Z for cases where $R_G||R_F$ is greater than 20kΩ (for MAX40079/MAX40077/MAX40078) and greater than 5kΩ (for MAX40087/MAX40089).

Applications Information

The MAX40079/MAX40087/MAX40077/MAX40089/MAX40078 family of op amps combine good driving capability that can also support ground/low-side sensing input and rail-to-rail output operation. With their low distortion and low noise, they are ideal for use in ADC buffers, DAC output buffers, medical instrumentation systems and other noise-sensitive applications.

However, there are two main application areas where these ultra-low input bias current op amps find place and they are to measure high impedance measurements. High Impedance measurements can be interfacing either Current output sensors or voltage output sensors that would need very high output resistance to be interfaced with. These op amps offer just that as the input impedance of these amplifiers is in the range of **1000G**Ω.

Voltage output sensors readout can be accomplished with unity gain buffer configuration and current output sensors like photo-diodes current read out can be accomplished in transimpedance amplifier configuration discussed later in this data sheet.

Ground-Sensing and Rail-to-Rail Outputs

The common-mode input range of these devices extends below ground over temperature that offers excellent common mode rejection and can be used in low side current sensing applications. These devices are guaranteed not to undergo phase reversal when the input is overdriven over input common mode voltage range as shown in Figure 2.

Figure 3 showcases the true rail-to-rail output operation of the amplifier, configured with A_V = 5V/V. The output swings to within 8mV of the supplies with a 10kΩ load, making the devices ideal in low-supply voltage applications.

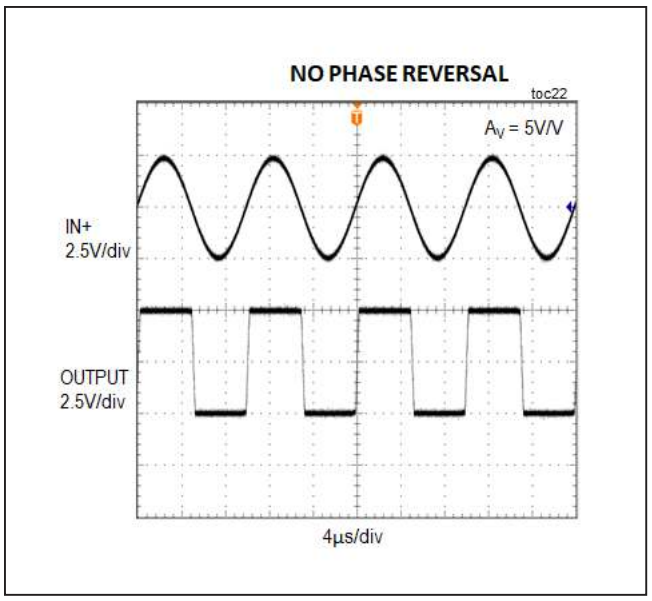


Figure 2. Scope Plot Showing Overdriven Input with No Phase Reversal

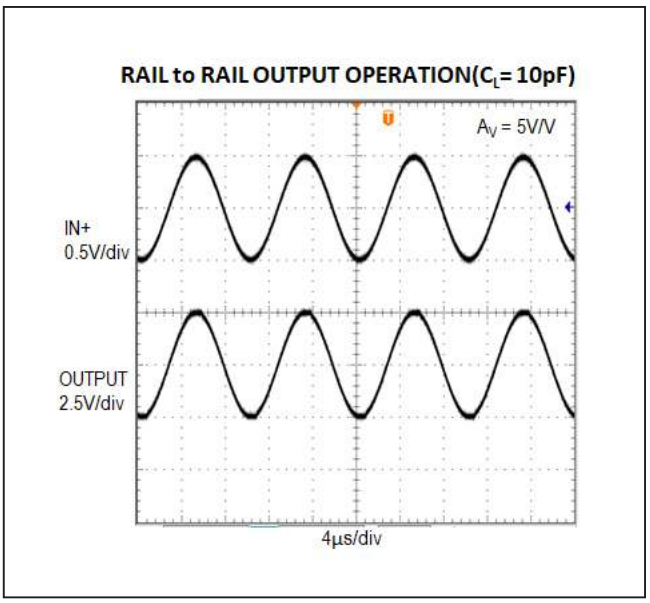


Figure 3. Rail-to-Rail Output Operation with 10kΩ

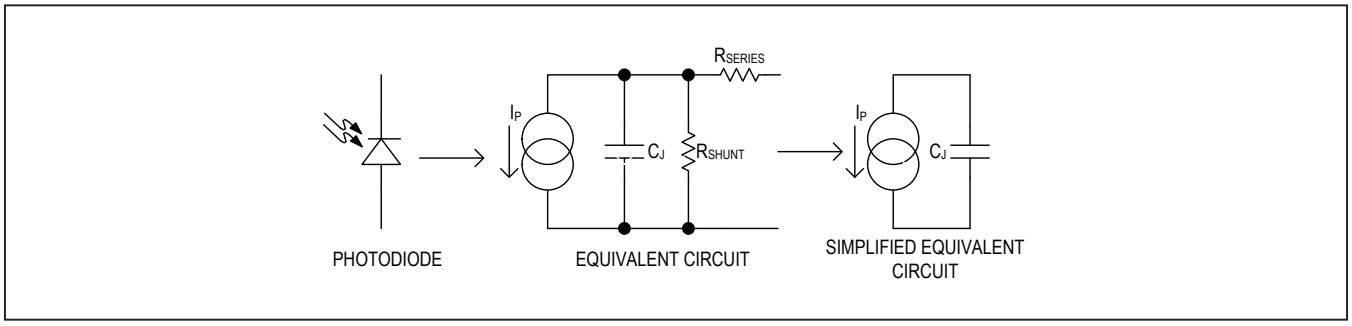


Figure 4. Photodiode Equivalent Circuit Showing Parasitics

Typical Application Circuit

Extremely Low-Leakage Op Amp (~50fA) Used as Transimpedance Amplifier

The ultra-low input bias current and low noise profile makes it an excellent choice for high impedance applications. It should be noted that unity gain stable is not a requirement for TIA applications. MAX40087/MAX40089 with increased GBW of 42MHz (min A_V ≥ 5V/V) may also be an option.

Figure 6 shows a transimpedance amplifier using MAX40077 suited for low to moderate TIA applications in photo-voltaic mode with buffered reference. This enables negligible reverse-voltage across the photodiode which ensures little to no dark current. A typical bias point of 100mV–200mV may be used to ensure the output of amplifier to be in linear range. Because of the nature of photo-diode in photo-voltaic modes, the input capacitance is more as compared to photo-conductive mode. Therefore, this mode is chosen for slower to moderate photo-diode current applications but this methodology provides high linearity, better accuracy and low noise performance.

Photodiode Equivalent Circuit (Figure 4):

I_P is current flowing through photodiode proportional to intensity of light on photodiode sensor

C_J is the junction input capacitance of the photodiode

R_{SHUNT} is the internal shunt resistance of the photodiode

R_{SERIES} is the internal series resistance of the photodiode

where $V_{OUT} = I_P \times R1$

where same equation still applies $V_{OUT} = I_P \times R1$

The input capacitance of the diode can destabilize the amplifier when choosing R1 in such a way that $1/(2 \times \pi \times R1 \times C_J) < GBW$ of the op amp. A feedback capacitance is required to add a zero to compensate for the phase shift. To learn more about Trans-impedance amplifier stabilization, please refer to the app note: AN5129: Stabilize your Transimpedance Amplifier.

For a critically damped system the $f_{-3dB} = \sqrt{(GBW/(2 \times \pi \times R1 \times (C1 + CJ))}$ and the value of C1 $= \sqrt{(CJ/2 \times \pi \times R1 \times GBW)}$.

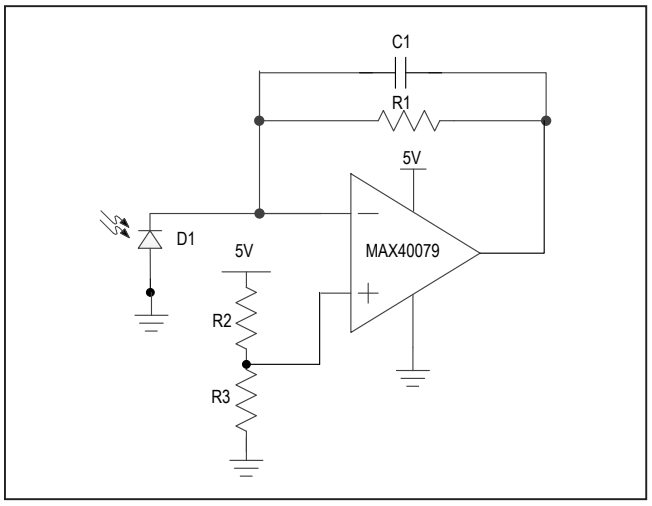


Figure 5. Single-Supply Transimpedance Amplifier Configuration with Single-Channel Op Amp

When using MAX40087 de-compensated Op-Amp, care must be taken that the noise gain $(1 + C_J/C1)$ at higher frequencies is higher than gain of 5V/V in order to stabilize the TIA.

Noise Consideration: choosing lower R1 will provide lower transimpedance and higher BW, but this may result in higher noise as the signal reduces by a factor of R1 and noise reduces by factor of $\sqrt{R1}$.

The noise contribution of R1 can be reduced by increasing the C1 value, but this lowers the bandwidth. A careful trade-off must be done to improve the signal-to-noise ratio (SNR).

Output Buffering of an Un-Buffered DAC:

The Figure 7 shows the single MAX40079 configured as an output buffer for the MAX5541 16-bit DAC. Because the MAX5541 has an unbuffered voltage output, the input bias current of the op amp used must be less than 6nA to maintain 16-bit accuracy. This family of amplifiers have an input bias current of only 160pA (max) over temperature, virtually eliminating this as a source of error. In addition, the MAX40079 has excellent open loop gain and common-mode rejection, making this an excellent output buffer amplifier.

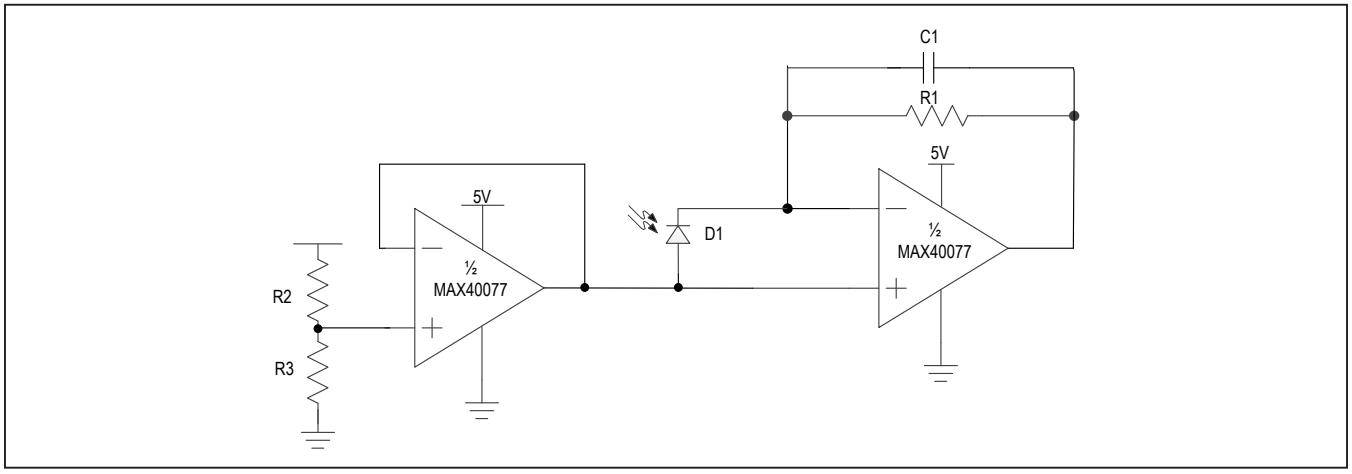


Figure 6. Single-Supply Transimpedance Amplifier Configuration with Dual-Channel Op Amp

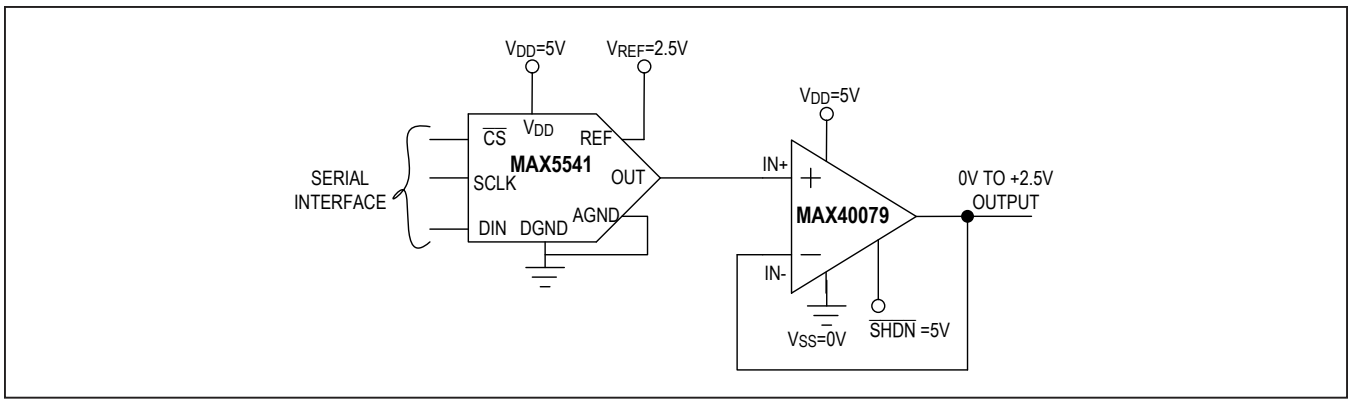


Figure 7. DAC Output Buffering with Op Amp

Capacitive Load Stability

The MAX40079 family of op amps drive up to 50pF in all configurations without any oscillation. Driving higher capacitive loads than 50pF might lead to oscillation in certain configurations due to reduction in phase margin and it can be seen as overshoot and undershoot with a step response on oscilloscope. If the application demands for the op amp to drive more than 50pF capacitive loads, it is recommended to add a series isolation resistor of 10-50Ω on the op amp output before capacitive load. Size of this resistor depends on the amount of capacitive load op amp is driving. Please refer to *Isolation Resistance vs. Capacitive Stability* graph in *Typical Operating Characteristics* for more information on resistance sizing.

This series isolation resistance is very useful in unity gain buffer configuration when full scale signal output swing is used as the unity gain configuration is the worst case for stability while driving capacitive loads.

Flux and Solder Contaminant Removal

Upon soldering process of the op amp on the PCB, remains of solder flux is a major performance degrading factor in measuring ultra-low input bias currents in the order of 50fA. Solvents like isopropyl alcohol (IPA) are effective in cleaning up solder flux contaminants. Upon clearly rubbing off the solder flux areas with IPA, ultrasonic cleaning in bath is highly recommended. Once the bath is completed, it can be dried up either at room temperature for several hours or placing the cleaned up PCB in an oven at elevated temperature for quick usage.

Power Supplies and Layout

The MAX40079/MAX40087/MAX40077/MAX40089/MAX40078 op amps operate from a single +2.7V to +5.5V power supply or from dual supplies of ±1.35V to ±2.75V. For single-supply operation, bypass the V_{DD} power supply pin with a 0.1µF ceramic capacitor placed close to the V_{DD} pin. If operating from dual supplies, bypass both V_{DD} and V_{SS} supply pins with 0.1µF ceramic capacitor to ground. If additional decoupling is needed add another 4.7µF or 10µF where supply voltage is applied on PCB.

Good layout improves performance by decreasing the amount of stray capacitance and noise at the op amp inputs and output. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amp's pins.

Guard rings and Shielding is highly recommended to guard the high impedance input traces against input leakage current. Refer to MAX40077 EV kit data sheet for more information on this. This is accomplished using a Triax connector and drving it's guard to the same potential as the signal on high impedance input.

Ordering Information

PART NUMBER	NUMBER OF CHANNELS	TEMP RANGE	PIN-PACKAGE	[STABLE GAIN V/V]	[GAIN BANDWIDTH PRODUCT IN MHZ]
MAX40079ANT+T	Single	-40°C to +125°C	6-WLP	1	10
MAX40079AUT+T	Single	-40°C to +125°C	6-SOT23	1	10
MAX40087ANT+T	Single	-40°C to +125°C	6-WLP	5	42
MAX40087AUT+T	Single	-40°C to +125°C	6-SOT23	5	42
MAX40077ANA+T	Dual	-40°C to +125°C	8-WLP	1	10
MAX40077AUA+T	Dual	-40°C to +125°C	µMAX-8	1	10
MAX40089ANA+T	Dual	-40°C to +125°C	8-WLP	5	42
MAX40089AUA+T	Dual	-40°C to +125°C	µMAX-8	5	42
MAX40078AUD+T	Quad	-40°C to +125°C	14 TSSOP	1	10
MAX40077AUA/V+T*	Dual	-40°C to +125°C	µMAX-8	1	10
MAX40089AUA/V+T*	Dual	-40°C to +125°C	µMAX-8	5	42

/V denotes an automotive qualified part.
** Denotes Future Product-Contact Maxim for availability*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/18	Initial release	—
1	3/18	Updated *Electrical Characteristics* and *Ordering Information* tables	3, 4, 6, 8, 16
2	5/18	Updated future product status of MAX40078AUD+T in *Ordering Information* table	16
3	7/18	Updated *General Description* section and *Ordering Information* table	16
4	3/19	Updated *Ordering Information*	16
5	7/19	Updated *Pin Configuration* diagram and *Pin Description* table	9, 10
6	11/19	Updated *Pin Configuration, Pin Description,* and *Ordering Information*	9, 10, 16
7	1/20	Updated *Pin Configuration* and *Ordering Information*	9, 16
8	4/20	Updated *Benefits and Features*, added package outline drawing	1, 3
9	6/21	Updated *Ordering Information* table.	17
10	10/21	Updated *Electrical Characteristics* table	5