BLF647PS

Broadband power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON Product data sheet

1. Product profile

1.1 General description

A 200 W LDMOS RF power transistor for broadcast transmitter and industrial applications. The transistor is suitable for the frequency range HF to 1500 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

Table 1. Application information

RF performance at $T_h = 25$ °C in a common source test circuit.

| Test signal | f | V _{DS} | I_{Dq} | P _{L(AV)} | P _{L(M)} | Gp | η_D | IMD3 |
|------------------|--|-----------------|----------|--------------------|-------------------|------|----------|-------|
| | (MHz) | (V) | (A) | (W) | (W) | (dB) | (%) | (dBc) |
| Pulsed, class-B | 1300 | 32 | 0.1 | - | 200 | 17.5 | 70 | - |
| CW, class-B | 1300 | 32 | 0.1 | 200 | - | 17.5 | 70 | - |
| 2-tone, class-AB | f ₁ = 1299.95; f ₂ = 1300.05 | 32 | 0.7 | 75 | - | 19 | 48 | -33 |

1.2 Features and benefits

- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications in the HF to 1500 MHz frequency range
- Industrial applications in the HF to 1500 MHz frequency range

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2. Pinning information

Table 2. Pinning

| | 9 | | |
|-----|-------------|--------------------|----------------|
| Pin | Description | Simplified outline | Graphic symbol |
| 1 | drain1 | | |
| 2 | drain2 | | 1 |
| 3 | gate1 | 5 | 3 |
| 4 | gate2 | | 5 |
| 5 | source | [1] | 4 7 |
| | | 3 4 | '□ |
| | | 3 4 | sym117 |

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

| Type number | Packag | Package | | |
|-------------|--------|--|----------|--|
| | Name | Description | Version | |
| BLF647PS | - | earless flanged ceramic package; 4 leads | SOT1121B | |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|----------------------|------------|-------|------|------|
| V_{DS} | drain-source voltage | | - | 65 | V |
| V_{GS} | gate-source voltage | | -0.5 | +11 | V |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| Tj | junction temperature | | [1] - | 225 | °C |

Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Тур | Unit |
|----------------------|--|---|-----------------|------|
| $R_{\text{th(j-c)}}$ | thermal resistance from junction to case | $T_{case} = 80 ^{\circ}C; P_{L} = 200 W$ | <u>[1]</u> 0.34 | K/W |

^[1] $R_{th(j-c)}$ is measured under RF conditions.

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6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|----------------------|----------------------------------|--|------|-----|------|------|
| V _{(BR)DSS} | drain-source breakdown voltage | $V_{GS} = 0 \text{ V}; I_D = 1.1 \text{ mA}$ | 65 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | V_{DS} = 28 V; I_{D} = 110 mA | 1.55 | 1.8 | 2.25 | V |
| I _{DSS} | drain leakage current | $V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$ | - | - | 1.4 | μΑ |
| I _{DSX} | drain cut-off current | $V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 20 \text{ V}$ | 18.1 | 20 | - | Α |
| I_{GSS} | gate leakage current | V_{GS} = 11 V; V_{DS} = 0 V | - | - | 140 | nA |
| g _{fs} | forward transconductance | V_{DS} = 20 V; I_{D} = 5500 mA | - | 7.6 | - | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 3.85 \text{ A}$ | - | 140 | - | mΩ |

Table 7. AC characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|------------------|----------------------|--|-----|-----|-----|------|
| C _{iss} | input capacitance | $V_{GS} = 0 \text{ V}; V_{DS} = 32 \text{ V}; f = 1 \text{ MHz}$ | - | 78 | - | pF |
| C _{oss} | output capacitance | $V_{GS} = 0 \text{ V}; V_{DS} = 32 \text{ V}; f = 1 \text{ MHz}$ | - | 30 | - | pF |
| C _{rs} | feedback capacitance | V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz | - | 1.3 | - | pF |

Table 8. RF characteristics

Test signal: CW; f = 1300 MHz; RF performance at $V_{DS} = 32$ V; $I_{Dq} = 100$ mA; $T_{case} = 25$ °C; unless otherwise specified; in a class-AB production test circuit.

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|------------|------------------|-------------------------|------|------|-----|------|
| Gp | power gain | $P_{L} = 200 \text{ W}$ | 16.5 | 17.5 | - | dB |
| η_{D} | drain efficiency | P _L = 200 W | 66 | 70 | _ | % |

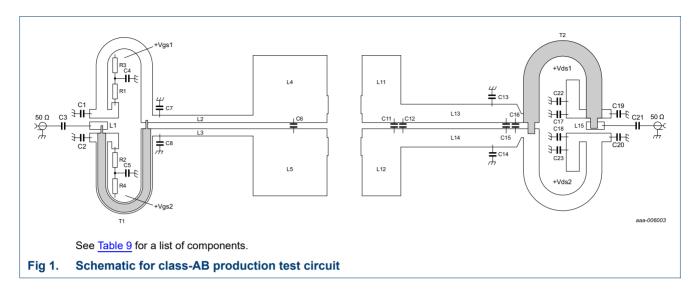
7. Test information

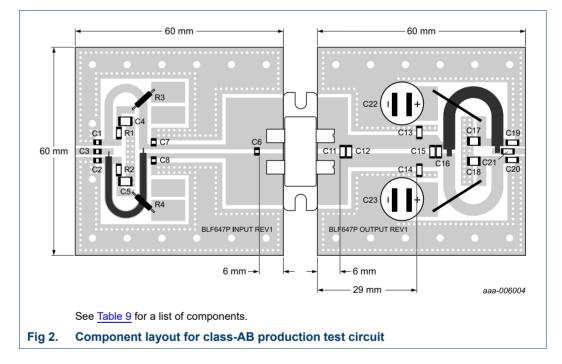
7.1 Ruggedness in class-AB operation

The BLF647PS is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 1300 MHz at rated load power.

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7.2 Test circuit information





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Table 9. List of components

Printed-Circuit Board (PCB): RF 35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μ m. See Figure 1 and Figure 2.

| Component | Description | Value | Remarks |
|---------------|-----------------------------------|------------------------------|--|
| C1, C2, C3 | multilayer ceramic chip capacitor | 68 pF | 1] |
| C4, C5 | multilayer ceramic chip capacitor | 4.7 μF, 50 V | |
| C6 | multilayer ceramic chip capacitor | 2.4 pF | 2] |
| C7, C8 | multilayer ceramic chip capacitor | 4.7 pF | <u>1]</u> |
| C11 | multilayer ceramic chip capacitor | 3.3 pF | 3] |
| C12 | multilayer ceramic chip capacitor | 2.4 pF | <u>3]</u> |
| C13, C14 | multilayer ceramic chip capacitor | 3.3 pF | 3] |
| C15, C16 | multilayer ceramic chip capacitor | 1.2 pF | 3] |
| C17, C18 | multilayer ceramic chip capacitor | 4.7 μF, 50 V | |
| C19, C20, C21 | multilayer ceramic chip capacitor | 220 pF | 3] |
| C22, C23 | electrolytic capacitor | 470 μF, 63 V | |
| L1 | microstrip | | (L \times W) 4 mm \times 1.7 mm |
| L2, L3 | microstrip | | (L \times W) 22.5 mm \times 1.6 mm |
| L4, L5 | microstrip | | (L \times W) 16.5 mm \times 15 mm |
| L11, L12 | microstrip | | (L \times W) 8.5 mm \times 15 mm |
| L13, L14 | microstrip | | (L \times W) 26 mm \times 4.2 mm |
| L15 | microstrip | | (L \times W) 4 mm \times 1.7 mm |
| R1, R2 | SMD resistor | 5.6 Ω | SMD1206 |
| R3, R4 | wire resistor | 100 Ω | |
| T1 | semi rigid coax | $25~\Omega$, $40~\text{mm}$ | Micro-Coax UT-090C-25 |
| T2 | semi rigid coax | 25Ω , 40mm | Micro-Coax UT-141C-25 |

^[1] American Technical Ceramics type 800A or capacitor of same quality.

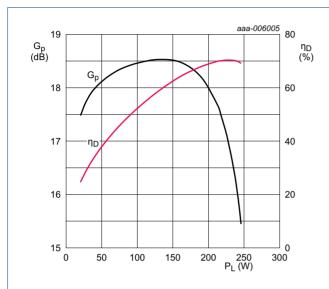
^[2] American Technical Ceramics type 100A or capacitor of same quality.

^[3] American Technical Ceramics type 800B or capacitor of same quality.

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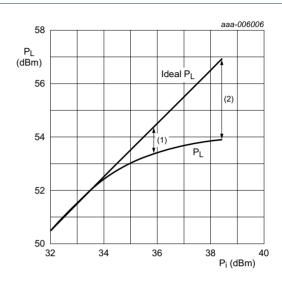
7.3 Graphical data

7.3.1 1-Tone CW



 V_{DS} = 32 V; I_{Dq} = 100 mA; f = 1300 MHz.

Fig 3. Power gain and drain efficiency as function of output power; typical values

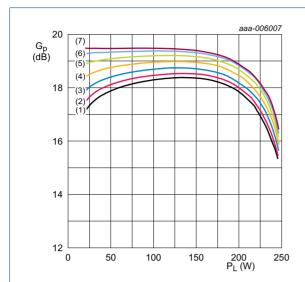


 V_{DS} = 32 V; I_{Dq} = 100 mA; f = 1300 MHz.

- (1) $P_{L(1dB)} = 53.4 \text{ dBm } (217 \text{ W})$
- (2) $P_{L(3dB)} = 53.9 \text{ dBm } (245 \text{ W})$

Fig 4. Output power as a function of input power; typical values

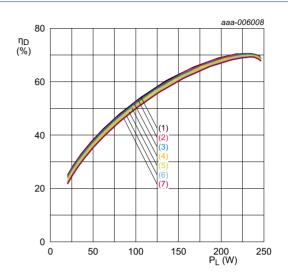
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V_{DS} = 32 V; f = 1300 MHz.

- (1) $I_{Dq} = 50 \text{ mA}$
- (2) $I_{Dq} = 100 \text{ mA}$
- (3) $I_{Dq} = 200 \text{ mA}$
- (4) $I_{Dq} = 300 \text{ mA}$
- (5) $I_{Dq} = 700 \text{ mA}$
- (6) $I_{Dq} = 1000 \text{ mA}$
- (7) $I_{Dq} = 1200 \text{ mA}$

Fig 5. Power gain as a function of output power; typical values

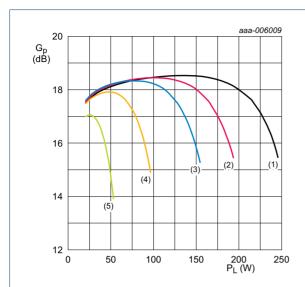


 $V_{DS} = 32 \text{ V}; f = 1300 \text{ MHz}.$

- (1) $I_{Dq} = 50 \text{ mA}$
- (2) $I_{Dq} = 100 \text{ mA}$
- (3) $I_{Dq} = 200 \text{ mA}$
- (4) $I_{Dq} = 300 \text{ mA}$
- (5) $I_{Dq} = 700 \text{ mA}$
- (6) $I_{Dq} = 1000 \text{ mA}$
- (7) $I_{Dq} = 1200 \text{ mA}$

Fig 6. Drain efficiency as a function of output power; typical values

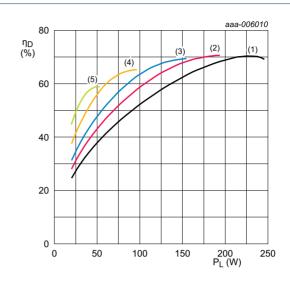
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 $I_{Dq} = 100 \text{ mA}$; f = 1300 MHz.

- (1) $V_{DS} = 32 V$
- (2) $V_{DS} = 28 \text{ V}$
- (3) $V_{DS} = 25 \text{ V}$
- (4) $V_{DS} = 20 \text{ V}$
- (5) $V_{DS} = 15 V$

Fig 7. Power gain as a function of output power; typical values

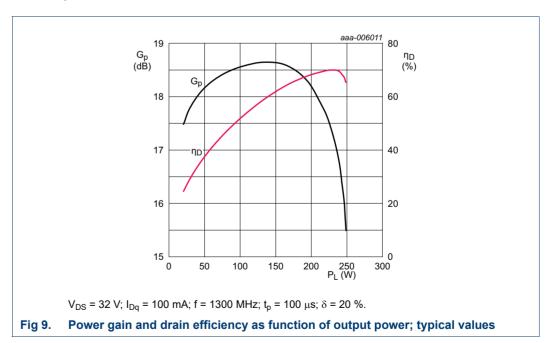


I_{Dq} = 100 mA; f = 1300 MHz.

- (1) $V_{DS} = 32 V$
- (2) $V_{DS} = 28 \text{ V}$
- (3) $V_{DS} = 25 V$
- (4) $V_{DS} = 20 V$
- (5) $V_{DS} = 15 V$

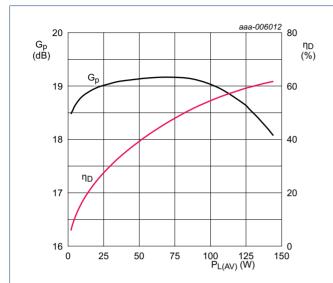
Fig 8. Drain efficiency as a function of output power; typical values

7.3.2 1-Tone pulsed



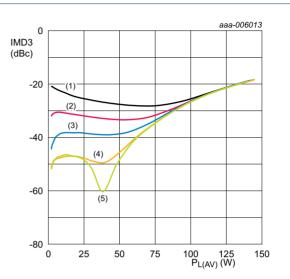
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7.3.3 2-Tone CW



 V_{DS} = 50 V; I_{Dq} = 700 mA; f_1 = 1299.95 MHz; f_2 = 1300.05 MHz.

Fig 10. Power gain and drain efficiency as function of average output power; typical values



 V_{DS} = 32 V; f_1 = 1299.95 MHz; f_2 = 1300.05 MHz.

- (1) $I_{Dq} = 100 \text{ mA}$
- (2) $I_{Dq} = 400 \text{ mA}$
- (3) $I_{Dq} = 700 \text{ mA}$
- (4) $I_{Dq} = 1000 \text{ mA}$
- (5) $I_{Dq} = 1200 \text{ mA}$

Fig 11. Third order intermodulation distortion as a function of average output power; typical values

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8. Package outline

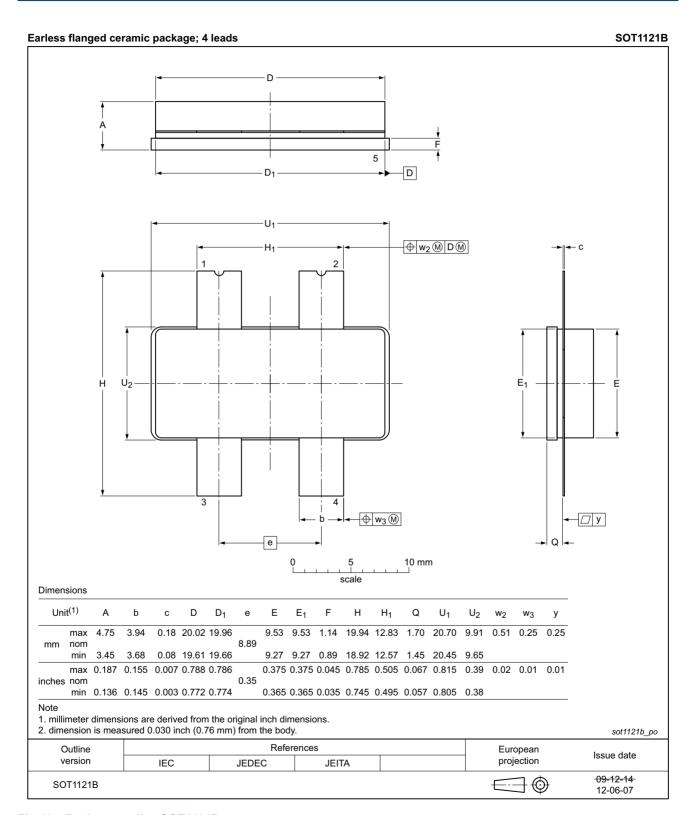


Fig 12. Package outline SOT1121B

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CW | Continuous Wave |
| ESD | ElectroStatic Discharge |
| HF | High Frequency |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| SMD | Surface Mounted Device |
| VSWR | Voltage Standing-Wave Ratio |

11. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes | | |
|----------------------|--|--|---------------|----------------------|--|--|
| BLF647PS#3 | 20150901 | Product data sheet | - | BLF647P_BLF647PS v.2 | | |
| Modifications: | | The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. | | | | |
| | Legal texts have been adapted to the new company name where appropriate. | | | | | |
| BLF647PS v.2 | 20131118 | Product data sheet | - | BLF647P_BLF647PS v.1 | | |
| BLF647P_BLF647PS v.1 | 20120803 | Objective data sheet | - | - | | |

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| Document status[1][2] | Product status[3] | Definition |
|--------------------------------|-------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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- [1] Please consult the most recently issued document before initiating or completing a design.
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