ZL30321

GbE/SONET/SDH/PDH Network Interface Synchronizer

Short Form Data Sheet

July 2009

Features

- Provides synchronous clocks for network interface cards that support synchronous Ethernet (SyncE) in addition to telecom interfaces (e.g. T1/E1, DS3/E3, etc)
- Two independant DPLLs provides timing for the transmit path (backplane to line rate) and the receive path (recovered line rate to backplane)
- Supports the requirements of ITU-T G.8262 for Synchronous Ethernet equipment slave clocks (EEC option 1 and 2) when combined with a system synchronizer such as the ZL30116, ZL30121, ZL30130, ZL30138
- Supports the requirements of Telcordia GR-253 SONET clocks and ITU-T G.813 SDH equipment slave clocks (SEC)
- Synchronizes to any standard telecom system reference with a multiple of 8 kHz up to 77.76 MHz or to Ethernet clock rates including 25 MHz, 50 MHz, 62.5 MHz, and 125 MHz
- Low jitter APLL generates either Ethernet clock rates (25 MHz, 50 MHz, 62.5 MHz, and 125 MHz) or SONET/SDH (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz) clock rates
- Programmable output synthesizers (P0, P1) generate clock frequencies with any multiple of 8 kHz up to 100 MHz

Ordering Information

ZL30321GGG	100 Pin CABGA	Trays
ZL30321GGG2	100 Pin CABGA*	Trays

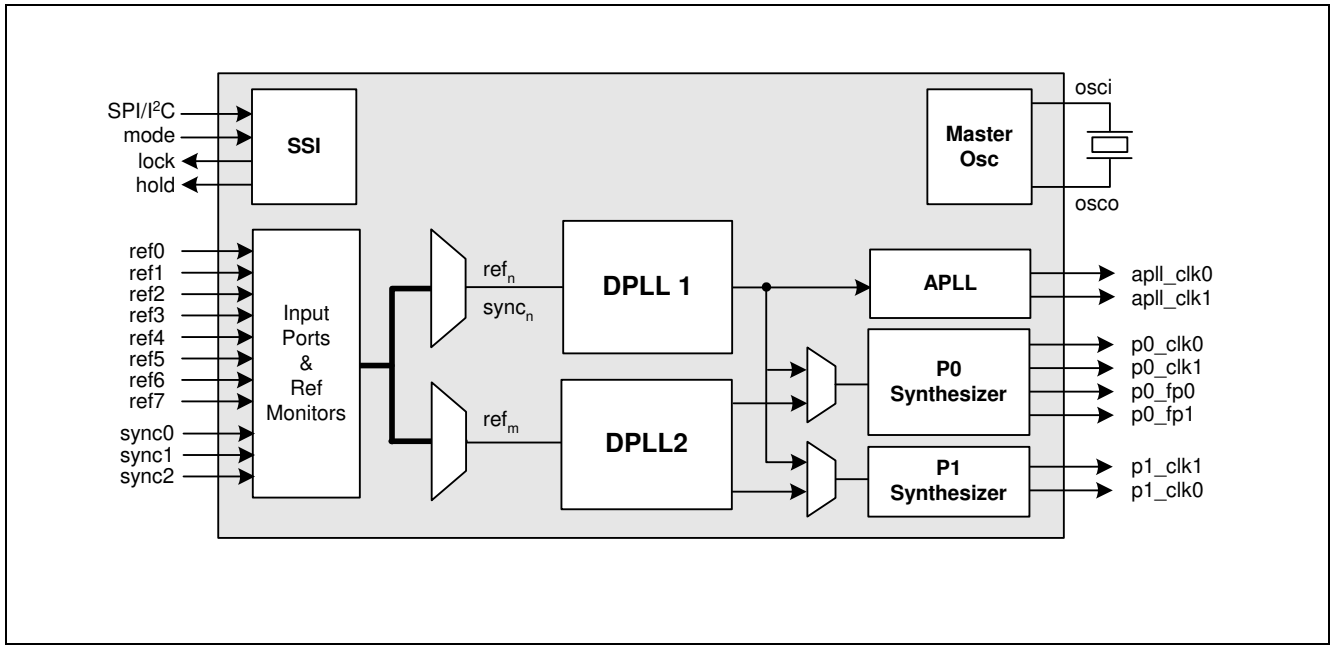
*Pb Free Tin/Silver/Copper in sampling phase

-40°C to +85°C

- Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- DPLLs can be configured to provide synchronous or asynchronous clock outputs
- Generates several styles of output frame pulses with selectable pulse width, polarity, and frequency
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities

Applications

- Carrier Grade Ethernet/SONET/SDH/PDH Network Interface Cards
- GPON ONT/ONU
- T1/E1 line cards
- DS3/E3 line cards



Pin Description

100BGA Pin #	Name	I/O Type	Description
Input Reference			
C1 B2 A3 C3 B3 B4 C4 A4	ref0 ref1 ref2 ref3 ref4 ref5 ref6 ref7	I_u	**Input References 7:0 (LVCMOS, Schmitt Trigger).** These input references are available to both DPLL1 and DPLL2 for synchronizing output clocks. All eight input references can lock to any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. Input ref0 and ref1 have additional configurable pre-dividers allowing input frequencies such as 62.5 MHz, 125 MHz. These pins are internally pulled up to V_{dd}.
B1 A1 A2	sync0 sync1 sync2	I_u	**Frame Pulse Synchronization References 2:0 (LVCMOS, Schmitt Trigger).** These are optional frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled up to $V_{dd.}$
Output Clocks and Frame Pulses			
D10	apll_clk0	O	**APLL Output Clock 0 (LVCMOS).** Output clock 0 of the APLL. The APLL can be configured to provide either SONET/SDH or Ethernet clock rates. The default frequency for this output is 77.76 MHz.
G10	apll_clk1	O	**APLL Output Clock 1 (LVCMOS).** Output clock 1 of the APLL. The APLL can be configured to provide either SONET/SDH or Ethernet clock rates. The default frequency for this output is 19.44 MHz.
K9	p0_clk0	O	**Programmable Synthesizer 0 - Output Clock 0 (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz, in addition to 2 kHz. The default frequency for this output is 65.536 MHz.
K7	p0_clk1	O	**Programmable Synthesizer 0 - Output Clock 1 (LVCMOS).** This is a programmable clock output configurable as a multiple or division of the p0_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 32.768 MHz.
K8	p0_fp0	O	**Programmable Synthesizer 0 - Output Frame Pulse 0 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz.
J7	p0_fp1	O	**Programmable Synthesizer 0 - Output Frame Pulse 1 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz
J10	p1_clk0	O	**Programmable Synthesizer 1 - Output Clock 0 (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 34.368 MHz.
K10	p1_clk1	O	**Programmable Synthesizer1 - Output Clock 1 (LVCMOS).** This is a programmable clock output configurable as a multiple or division of the p1_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 68.736 MHz.

100BGA Pin #	Name	I/O Type	Description
E1	ref_out	O	**DPLL2 Selected Output Reference (LVCMOS).** This is a buffered copy of the output of the reference selector for DPLL2. Switching between input reference clocks at this output is not hitless.
Control			
H5	rst_b	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
J5	hs_en	I_u	**DPLL1 Hitless Switching Enable (LVCMOS, Schmitt Trigger).** A logic high at this input enables hitless reference switching. A logic low disables hitless reference switching and re-aligns DPLL1's output phase to the phase of the selected reference input. This feature can also be controlled through software registers. This pin is internally pulled up to Vdd.
C2 D2	mod0 mod1	I_u	**DPLL1 Mode Select 1:0 (LVCMOS, Schmitt Trigger).** During reset, the levels on these pins determine the default mode of operation for DPLL1 (Automatic, Normal, Holdover or Freerun). After reset, the mode of operation can be controlled directly with these pins, or by accessing the dpll1_modesel register (0x1F) through the serial interface. This pin is internally pulled up to Vdd.
Status			
H1	lock	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for DPLL1. This output goes high when DPLL1's output is frequency and phase locked to the input reference.
J1	hold	O	**Holdover Indicator (LVCMOS).** This pin goes high when DPLL1 enters the holdover mode.
Serial Interface			
E2	sck_scl	I/B	**Clock for Serial Interface (LVCMOS).** Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I^2C interface.
F1	si_sda	I/B	**Serial Interface Input (LVCMOS).** Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I^2C interface.
G1	so	O	**Serial Interface Output (LVCMOS).** Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
E3	cs_b_asel0	I_u	**Chip Select for SPI/Address Select 0 for I^2C (LVCMOS).** When i2c_en = 0, this pin acts as the chip select pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the asel0 pin for the I^2C interface.
F3	asel1	I_u	**Address Select 1 for I^2C (LVCMOS).** When i2c_en = 1, this pin acts as the asel1 pin for the I^2C interface. Internally pulled up to Vdd. Leave open when not in use.
F2	asel2	I_u	**Address Select 2 for I^2C (LVCMOS).** When i2c_en = 1, this pin acts as the asel2 pin for the I^2C interface. Internally pulled up to Vdd. Leave open when not in use.

100BGA Pin #	Name	I/O Type	Description
G2	int_b	O	**Interrupt Pin (LVCMOS).** Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled-up to Vdd.
J2	i2c_en	I_u	**I^2C Interface Enable (LVCMOS).** If set high, the I^2C interface is enabled, if set low, the SPI interface is enabled. Internally pull-up to Vdd.
APLL Loop Filter			
A6	apll_filter	A	**External Analog PLL Loop Filter terminal.**
B6	filter_ref0	A	**Analog PLL External Loop Filter Reference.**
C6	filter_ref1	A	**Analog PLL External Loop Filter Reference.**
JTAG and Test			
J4	tdo	O	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K2	tdi	I_u	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.
H4	trst_b	I_u	**Test Reset (LVCMOS).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
K3	tck	I	**Test Clock (LVCMOS):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
J3	tms	I_u	**Test Mode Select (LVCMOS).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
K4	osci	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (TCXO, OCXO). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
K5	osco	O	**Oscillator Master Clock Output (LVCMOS).** This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
J6	IC		**Internal Connection.** Connect to ground.
C5 B5 K6 H10 E10 F10	IC		**Internal Connection.** Leave unconnected.

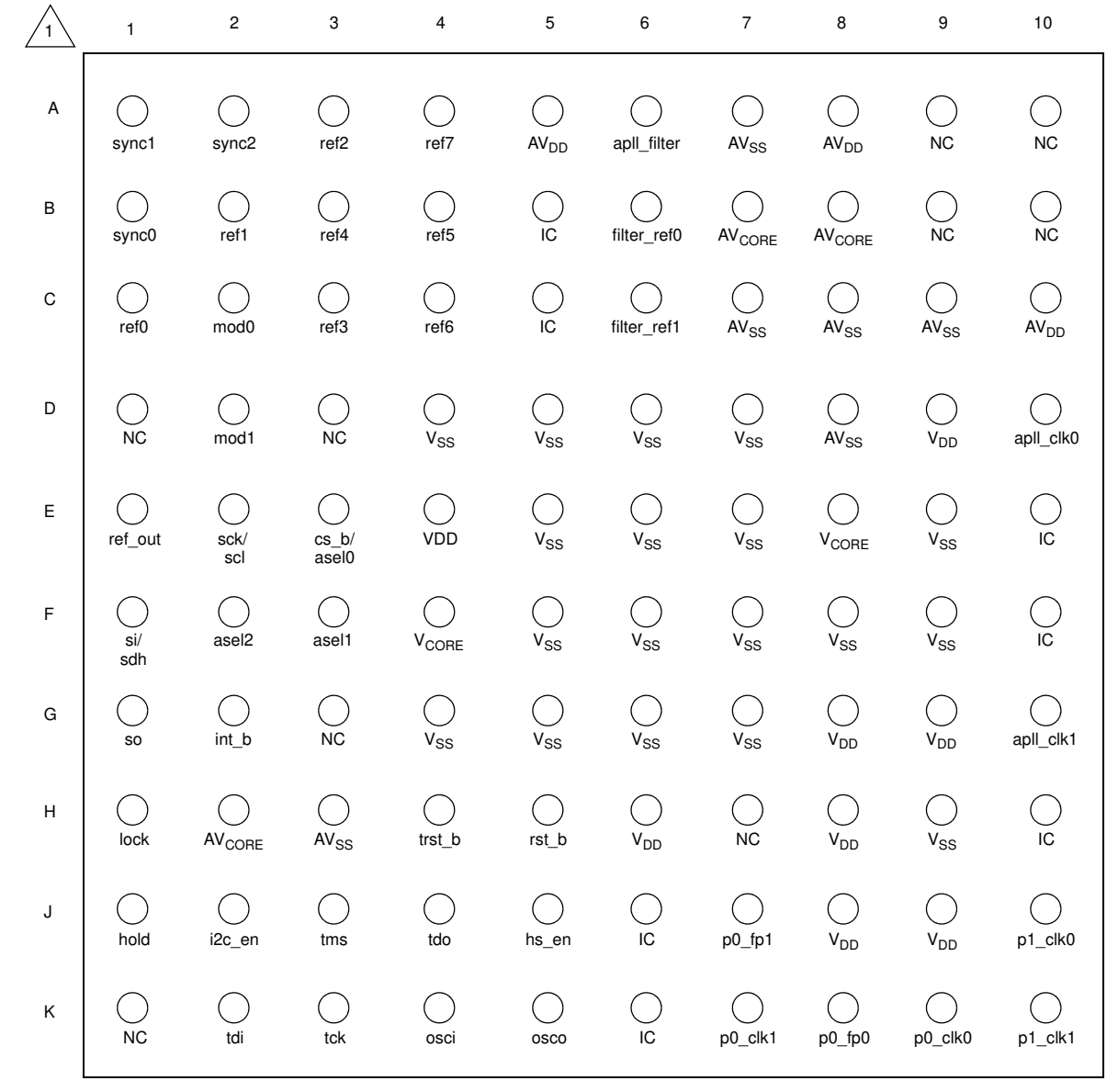
100BGA Pin #	Name	I/O Type	Description
D3 K1 H7 G3 D1 A9 B10 A10 B9	NC		**No Connection.** Leave unconnected.
Power and Ground			
D9 E4 G8 G9 J8 J9 H6 H8	V_{DD}	P P P P P P P P	**Positive Supply Voltage.** +3.3V_{DC} nominal.
E8 F4	V_{CORE}	P P	**Positive Supply Voltage.** +1.8V_{DC} nominal.
A5 A8 C10	AV_{DD}	P P P	**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
B7 B8 H2	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
D4 D5 D6 D7 E5 E6 E7 F5 F6 F7 G4 G5 G6 G7 E9 F8 F9 H9	V_{SS}	G G G G G G G G G G G G G G G G G G	**Ground.** 0 Volts.

100BGA Pin #	Name	I/O Type	Description
A7 C7 C8 C9 D8 H3	AV_{SS}	G G G G G G	**Analog Ground.** 0 Volts.

I - Input
I_d - Input, Internally pulled down
I_u - Input, Internally pulled up
O - Output
A - Analog
P - Power
G - Ground

1.0 Pin Diagram

TOP VIEW



1 - A1 corner is identified with a dot.

2.0 Overview

The ZL30321 SONET/SDH/GbE Mulit-Rate Line Card Synchronizer is a highly integrated device that provides timing for network interface cards. It incorporates two independent DPLLs, each capable of locking to one of eight input references and provides a wide variety of synchronized output clocks and frame pulses.

This device is ideally suited for designs that require both a transmit timing path (backplane to PHY) and a receive timing path (PHY to backplane). Each path is controlled with separate DPLLs (DPLL1, DPLL1) which are both independently configurable through the serial interface (SPI or I^2C). A typical application of the ZL30321 is shown in Figure 2. In this application, the ZL30321 translates the 19.44 MHz clock from the telecom rate backplane (system timing bus), translates the frequency to 125 MHz for the PHY Tx clock, and filters the jitter to ensure compliance with the related standards. A programmable synthesizer (P0) provides optional synchronous PDH clocks with multiples of 8 kHz for generating PDH interface clocks. On the receive path, DPLL2 and the P1 synthesizer translate the line recovered clock (8 kHz or 1.544 MHz) from the PHY to the 19.44 MHz telecom backplane (line recovered timing) for the central timing cards. The ZL30321 allows easy integration of Ethernet line rates with today's telecom backplanes.

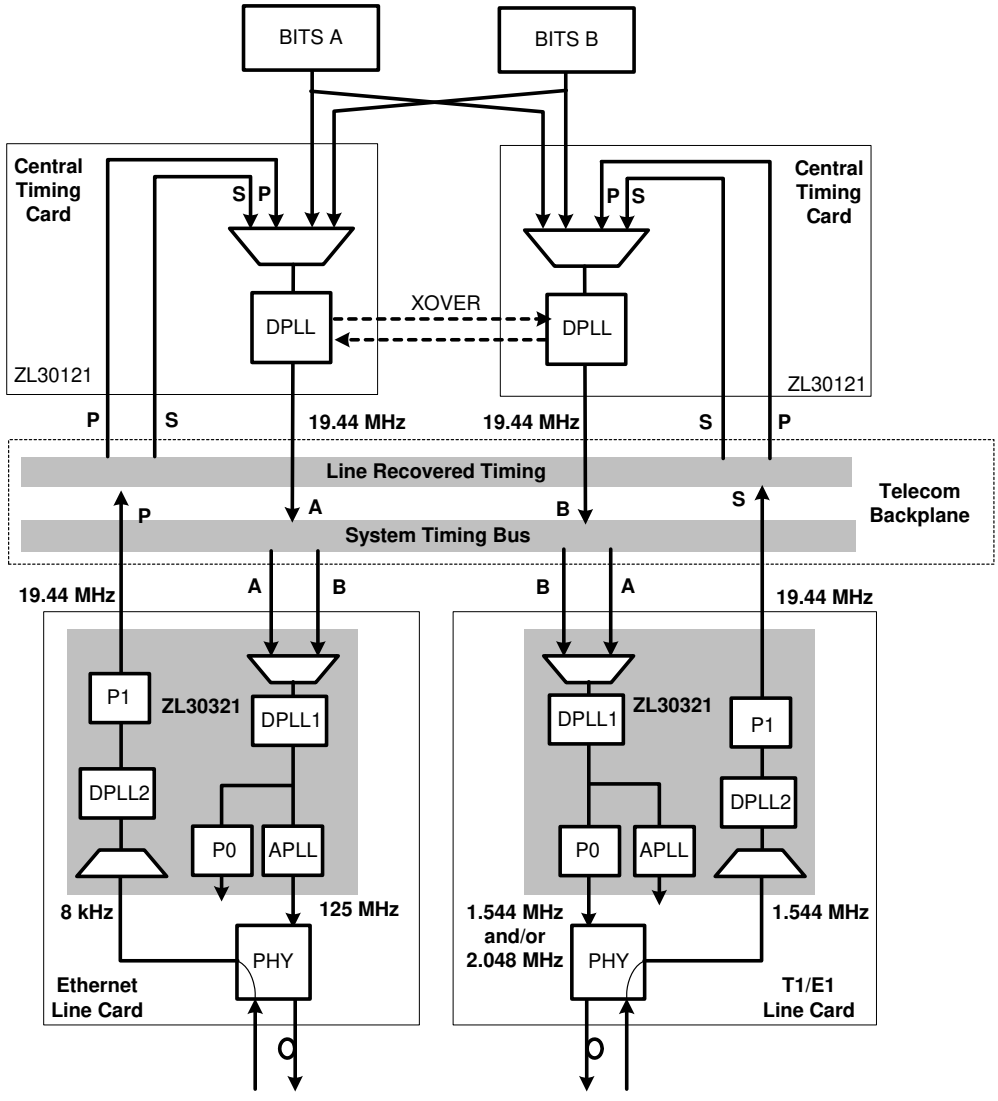
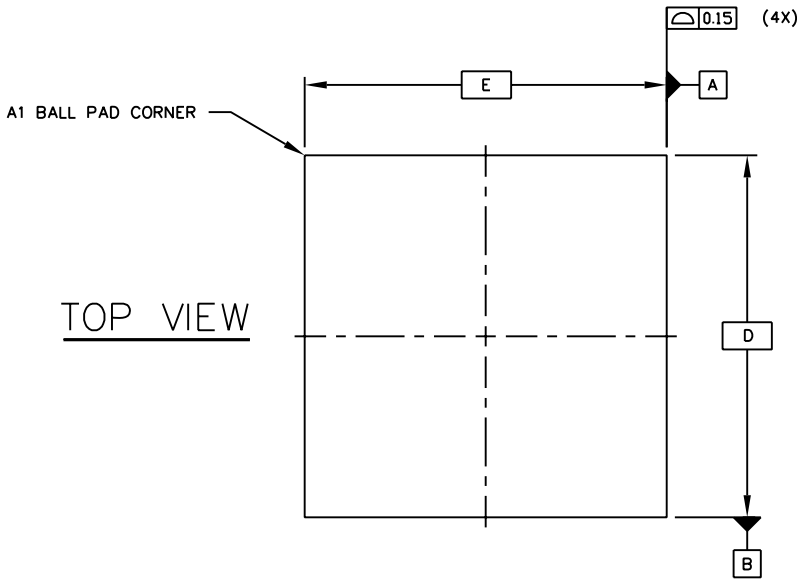
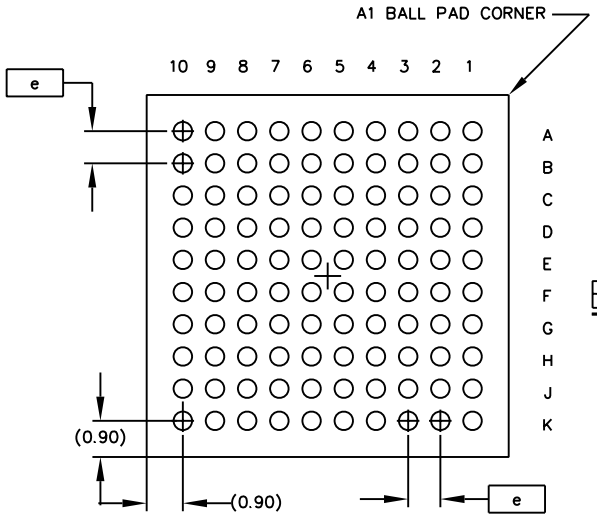


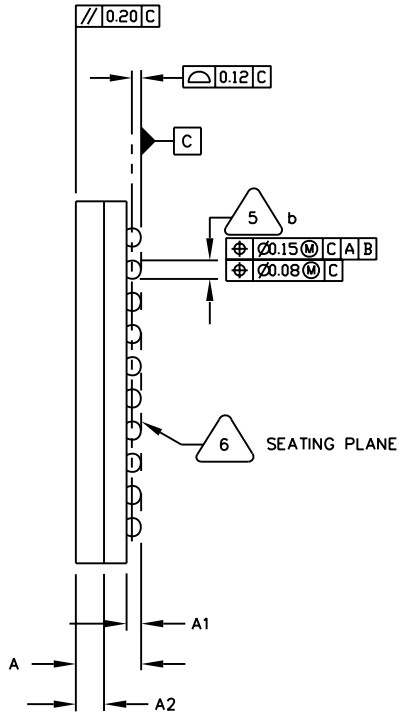
Figure 2 - Typical Application of the ZL30321





BOTTOM VIEW

100 SOLDER BALLS



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D	8.85	9.00	9.15
E	8.85	9.00	9.15
e		0.8 Ref	
n		100	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.8mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1	2	3	
ACN	CDCA	CDCA	CDCA	
DATE	15April05	24Aug05	26Oct06	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 100ball 9x9mm, 0.8 mm Pitch, 4 layer, CABGA

111040

For more information about all Zarlink products visit our Web Site at

www.zarlink.com