

ZL30152 Universal Rate Adapting Synchronous Clock Generator

Short Form Data Sheet

Features

- Programmable synthesizers generate any clockrate from 1 kHz to 750 MHz
- Precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- Programmable digital PLL synchronize to any clock rate from 1 kHz to 750 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLL filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Two reference inputs configurable as single ended or differential
- · Four LVPECL outputs and two LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

Ordering Information

ZL30152GGG 64 Pin LBGA ZL30152GGG2 64 Pin LBGA*

Trays Trays

January 2012

*Pb Free Tin/Silver/Copper -40°C to +85°C

Applications

- Clock Generation for Physical Line Interface:
 - SONET/SDH, OC-192/OC-48
 - SONET/SDH with FEC
 - 10G Base X, R and W
 - 100 BaseX, GE, Fibre channel
- Clock Generation and Distribution for back plane Interface:
 - TDM, Telecom Bus, Utopia, SBI
- Rapid-IO, PCI-Express, serial MII, Star Fabric, XAUI

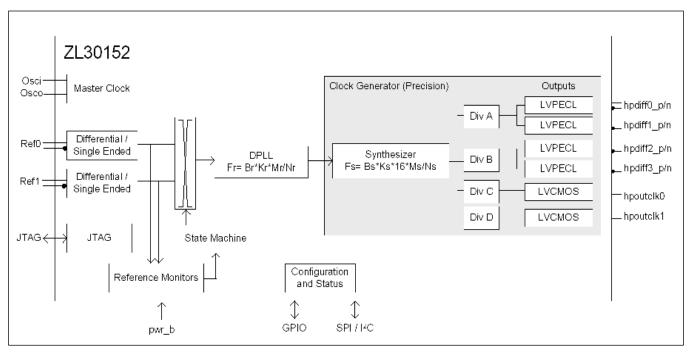
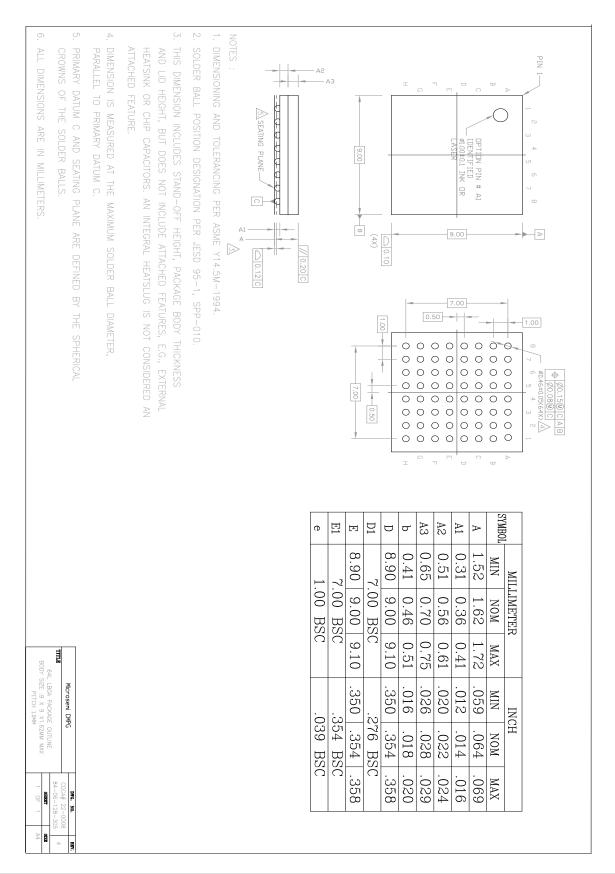


Figure 1 - Functional Block Diagram



ZL30152

Mechanical Drawing



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