Low Power Multiclock Generator with VCFS
AK8135F

Features

- 24.576MHz Crystal Input
- One 24.576MHz-Reference Output
- Selectable Clock out Frequencies:
  - 24.576 MHz at CLK1
  - 24.99972 MHz at CLK2
  - 33.332965 MHz at CLK3
  - 27.000 MHz at REF1-4
- Built-in two VCFS
  - Pull Range: ±85ppm (typ.)
- Low Jitter Performance
  - Period Jitter:
    150 psec (Typ.) at CLK1-3, REF1-4
  - Long term jitter:
    400 psec (Typ.) at CLK1-3, REF1-4
- Low Current Consumption:
  24 mA (Typ.) at 3.3V
- Low C/N output:
  72 dB (Typ.) at REF1-4
- Supply Voltage:
  3.0 – 3.6V
- Operating Temperature Range:
  -20 to +85℃
- Package:
  30-pin VSOP (Lead free)

Description

AK8135F is a member of AKM's low power multi clock generator family designed for Recorders, DTVs or STBs, requiring a range of system clocks with high performance. AK8135F generates different frequency clocks from a 24.576MHz crystal oscillator and provides them to seven outputs. The on-chip VCFS (Voltage Controlled Frequency Synthesizer) accepts a voltage control input to allow the output clocks to vary by ±85 ppm for synchronizing to the external clock system. Both circuitries of VCFS and PLL in AK8135F are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption.
AK8135F is available in a 30-pin VSOP package.

Applications

- HDD, DVD, BD Recorder
- DTV
- Set-Top-Boxes

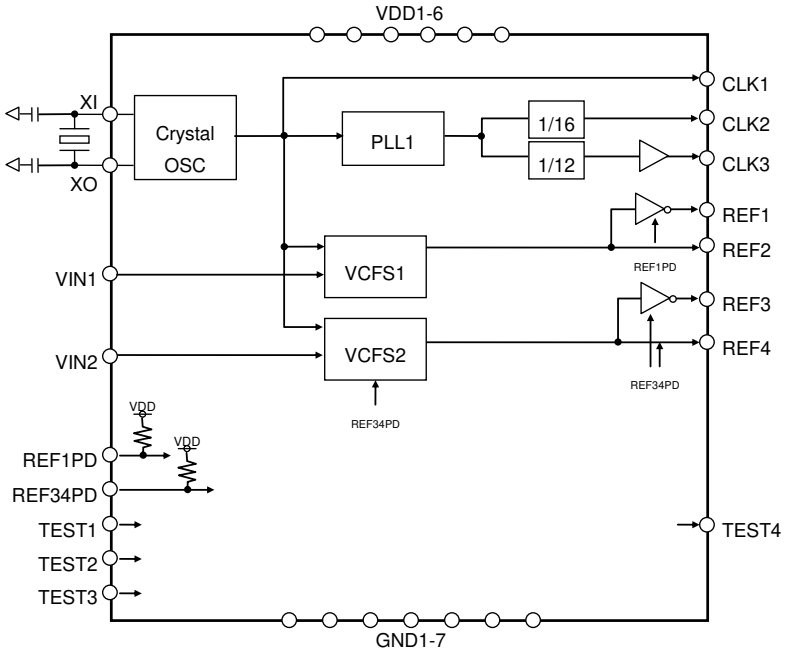


Figure 1: AK8135F Multi Clock Generator

Pin Descriptions

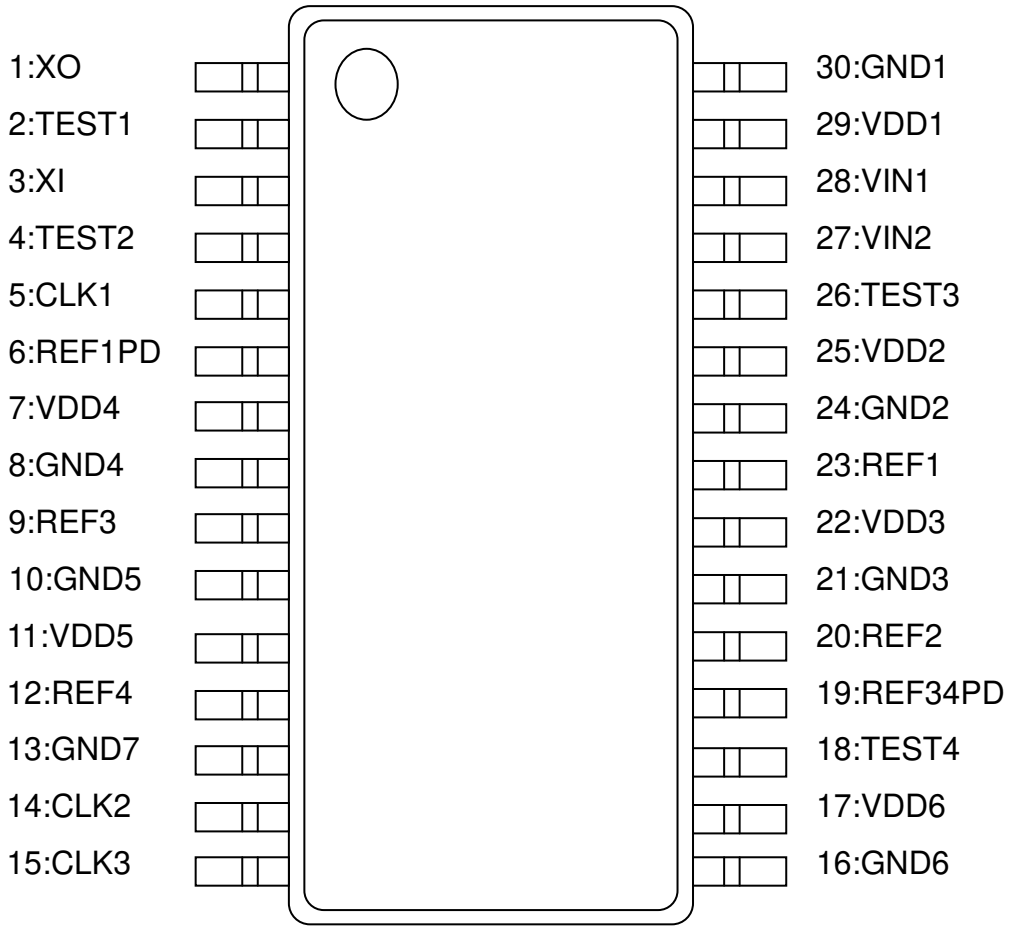


Figure 2: Package: 30-Pin VSOP(Top View)

Pin No.	Pin Name	Pin Type	Description
1	XO	AO	Crystal connection, Connect to 24.576MHz crystal
2	TEST1	DI	TEST input pin, Connect to GND.
3	XI	AI	Crystal connection, Connect to 24.576MHz crystal
4	TEST2	DI	TEST input pin, Connect to GND.
5	CLK1	DO	Reference Clock Output of XO based on 24.576MHz Crystal
6	REF1PD	DI	REF1 pin Mode Select pin "H": Enable, REF1 pin outputs 27.00MHz. "L": Disable, REF1 pin is "L". (1)
7	VDD4	PWR	Power Supply 4
8	GND4	PWR	Ground 4
9	REF3	DO	Reference Clock Output 3 from VCFS2 When REF34PD pin = "H", Output frequency is 27.00MHz. When REF34PD pin = "L", this pin is "L" output.
10	GND5	PWR	Ground 5
11	VDD5	PWR	Power Supply 5
12	REF4	DO	Reference Clock Output 4 from VCFS2 When REF34PD pin = "H", Output frequency is 27.00MHz. When REF34PD pin = "L", this pin is "L" output.
13	GND7	PWR	Ground 7
14	CLK2	DO	Clock output 2, Output frequency is 25.000MHz.
15	CLK3	DO	Clock output 3, Output frequency is 33.333MHz.
16	GND6	PWR	Ground 6
17	VDD6	PWR	Power Supply 6
18	TEST4	DO	TEST output pin, this pin is "L" output and should be open.
19	REF34PD	DI	REF3 and REF4 pins Mode Select pin, VCFS2 Power Down pin "H": Enable, REF3 and REF4 pins output 27.00MHz and VCFS2 is Normal Operation. (1) "L": Disable, REF3 and REF4 pins are "L" and VCFS2 is powered down.
20	REF2	DO	Reference Clock Output 2 from VCFS1, Output frequency is 27.00MHz.
21	GND3	PWR	Ground 3
22	VDD3	PWR	Power Supply 3
23	REF1	DO	Reference Clock Output 1 from VCFS1 When REF1PD pin = "H", Output frequency is 27.00MHz. When REF1PD pin = "L", this pin is "L" output.
24	GND2	PWR	Ground 2
25	VDD2	PWR	Power Supply 2
26	TEST3	DI	TEST input pin, Connect to GND.
27	VIN2	AI	VCFS2 Control Voltage Input
28	VIN1	AI	VCFS1 Control Voltage Input
29	VDD1	PWR	Power Supply 1
30	GND1	PWR	Ground 1

(1) Internal pull up 52kΩ

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8135F	AK8135F	Tape and Reel	30-pin VSOP	-20 to 85℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	VIN	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	IIN	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage(1)	VDD	Pin: VDD1-6	3.0	3.3	3.6	V

Note:

(1) Power to VDD1-6 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pin.

DC Characteristics

VDD: over 3.0 to 3.6V, Ta: -20 to +85°C, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: REF1PD, REF34PD, TEST1-3	0.7VDD			V
Low Level Input Voltage	V_{IL}	Pin: REF1PD, REF34PD, TEST1-3			0.3VDD	V
Input Current 1	I_L1	Pin: TEST1-3	-10		+10	µA
Input Current 2	I_L2	Pin: REF1PD, REF34PD V_{IH}=VDD	-10		+10	µA
Input Current 3	I_L3	Pin: REF1PD, REF34PD V_{IL}=GND	-134	-58	-25	µA
Input Current 4	I_L4	Pin: VIN1, VIN2	-3		+3	µA
High Level Output Voltage	V_{OH}	Pin: CLK1-3, REF1-4 I_{OH}=-4mA	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: CLK1-3, REF1-4 I_{OL}=+4mA			0.2VDD	V
Current Consumption 1	$I_{DD}1$	No load REF1PD='H', REF34PD='H'		24	32	mA
Current Consumption 2	$I_{DD}2$	No load REF1PD='L', REF34PD='H'		23	31	mA
Current Consumption 3	$I_{DD}3$	No load REF1PD='H', REF34PD='L'		17	22	mA
Current Consumption 4	$I_{DD}4$	No load REF1PD='L', REF34PD='L'		16	21	mA

AC Characteristics

VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency (1)	F_{osc}	Pin:XI,XO		24.576		MHz
Output Clock Accuracy (1)	$F_{accuracy}$	Pin:CLK1 24.576MHz Crystal CL=10[pF]	-30	0	+30	ppm
		Pin:CLK2 24.99972MHz Relative to 25.000MHz Crystal CL=10[pF]	-41	-11	+19	ppm
		Pin:CLK3 33.332965MHz Relative to 33.333MHz Crystal CL=10[pF]	-41	-11	+19	ppm
		Pin:REF1-4 27.000MHz VIN1/VIN2=0.5VDD Crystal CL=10[pF]	-30	0	+30	ppm
VCFS Pullable Range	PR_{VCFS}	Pin:REF1-4 VIN1/VIN2=0.5VDD±1.0	±65	±85	±115	ppm
VCFS Response Time	RT_{VCFS}	Pin:REF1-4 VIN1/VIN2=0.5VDD±1.0	5	20		ppm/100ms
C/N	CN	Pin:REF1-4 with Load Cpl2=25pF		72		dB
Output Clock Rise Time 1	$T_{\_rise1}$	Pin:CLK1, CLK2 with Load Cpl1=15pF 0.2VDD → 0.8VDD		1.5	4.0	ns
Output Clock Fall Time 1	$T_{\_fall1}$	Pin:CLK1, CLK2 with Load Cpl1=15pF 0.8VDD → 0.2VDD		1.5	4.0	ns
Output Clock Rise Time 2	$T_{\_rise2}$	Pin:CLK3, REF1-4 with Load Cpl2=25pF 0.2VDD → 0.8VDD		2.5	4.0	ns
Output Clock Fall Time 2	$T_{\_fall2}$	Pin:CLK3, REF1-4 with Load Cpl2=25pF 0.8VDD → 0.2VDD		2.5	4.0	ns
Period Jitter (2)	$Jit_{\_period}$	Pin:CLK1, CLK2 with Load Cpl1=15pF		150 (6 σ)	300 (6 σ)	ps
		Pin:CLK3, REF1-4 with Load Cpl2=25pF				
Long Term Jitter (2)	$Jit_{\_long}$	Pin:CLK1, CLK2 with Load Cpl1=15pF 1000 cycle delay		400 (6 σ)	600 (6 σ)	ps
		Pin:CLK3, REF1-4 with Load Cpl2=25pF 1000 cycle delay				
Output Clock Duty Cycle	DtyCyc	Pin:CLK2 with Load Cpl1=15pF	45	50	55	%
		Pin:CLK3, REF1-4 with Load Cpl2=25pF				
		Pin: CLK1 with Load Cpl1=15pF	40	50	60	%
Power-up Time (3)	$T_{\_put}$	Pin:CLK1, CLK2 with Load Cpl1=15pF		1	2	ms
		Pin:CLK3, REF1-4 with Load Cpl2=25pF				

(1) Output Clock Accuracy depends on crystal characteristics, on-chip load capacitance, and stray capacity of PCB. MIN., Max.=±30ppm is applied to AKM's authorized test condition.
Please contact us when you plan the use of other crystal unit.

(2) ±3σ in 10000 sampling or more

(3) Time to settle output into 0.1% of specified frequency.

Function Description

Voltage Controlled Frequency Synthesizer (VCFS)

AK8135F has a voltage controlled frequency synthesizer (VCFS), featuring fine frequency tuning for 27MHz of primary clock frequency by external DC voltage control. This tuning enables output clock frequency to synchronize the external clock system.
VCFS is composed of analog-to-digital converter and high resolution PLL as shown in Figure 3. VIN1 (Pin28) and VIN2 (Pin27) accept DC voltage control from a processor or a system controller, and pulls the primary frequency of crystal to higher or lower. This pulling range is determined by supply Voltage to AK8135F. AK8135F is designed to range ±85ppm of primary frequency, and the typical pulling profile is shown in **Figure 4**.

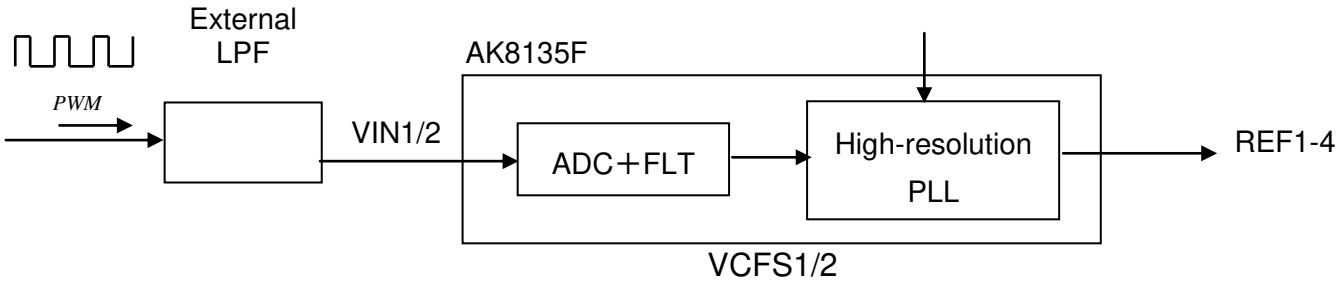


Figure 3: VCFS Diagram

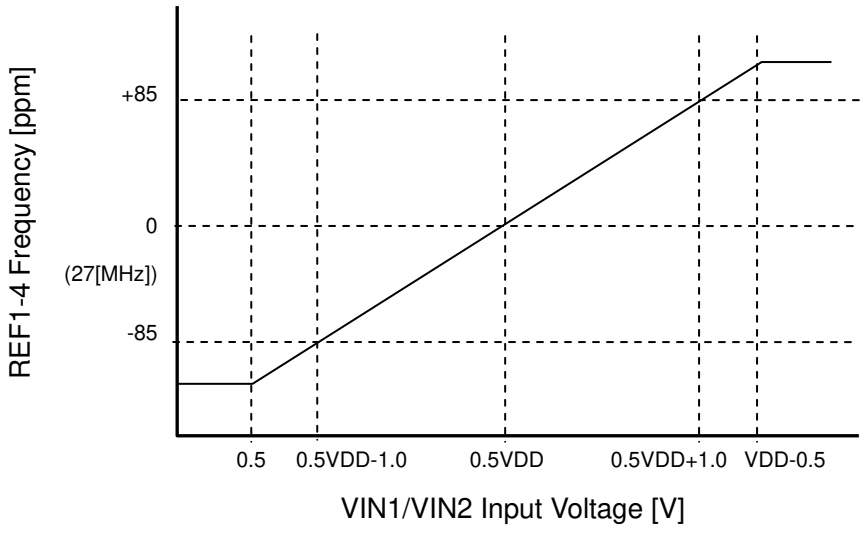


Figure 4: Typical VCFS Pulling Profile

Typical Connection Diagram

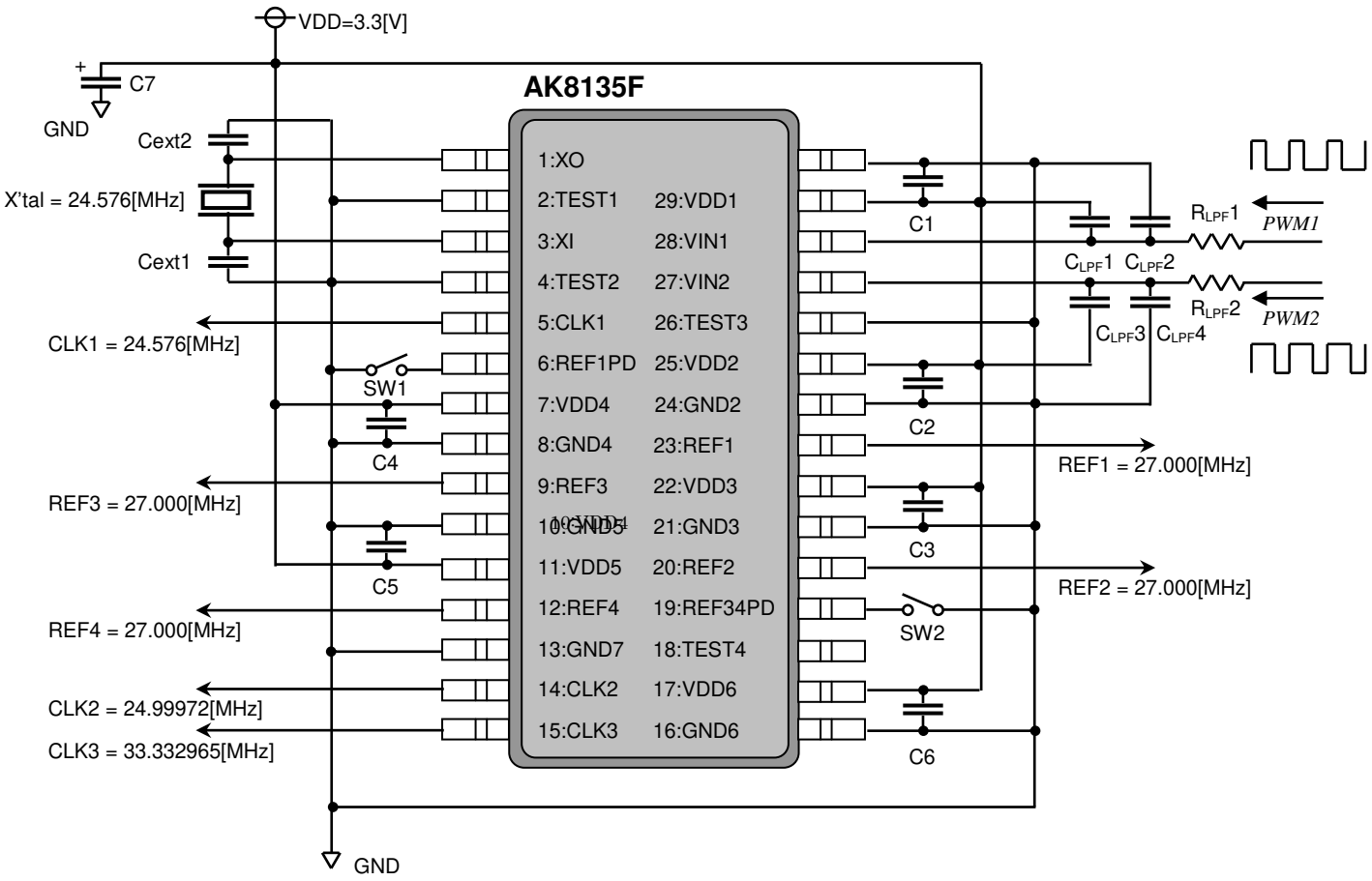


Figure 5: Typical Connection Diagram

C1, C2, C3, C4, C5, C6: 0.1µF
C7 : Electrolytic capacitor
Cext1, Cext2: Depends on crystal characteristics. Refer the specification of the crystal.
SW1, SW2: It is a switch that controls outputs of REF1, REF3 and REF4 and power up/down of VCFS2.
$R_{LPF}1$, $R_{LPF}2$, $C_{LPF}1$, $C_{LPF}2$, $C_{LPF}3$, $C_{LPF}4$: In case of interface by PWM. For right configuration, refer the specification of the applied processor.

PCB Layout Consideration

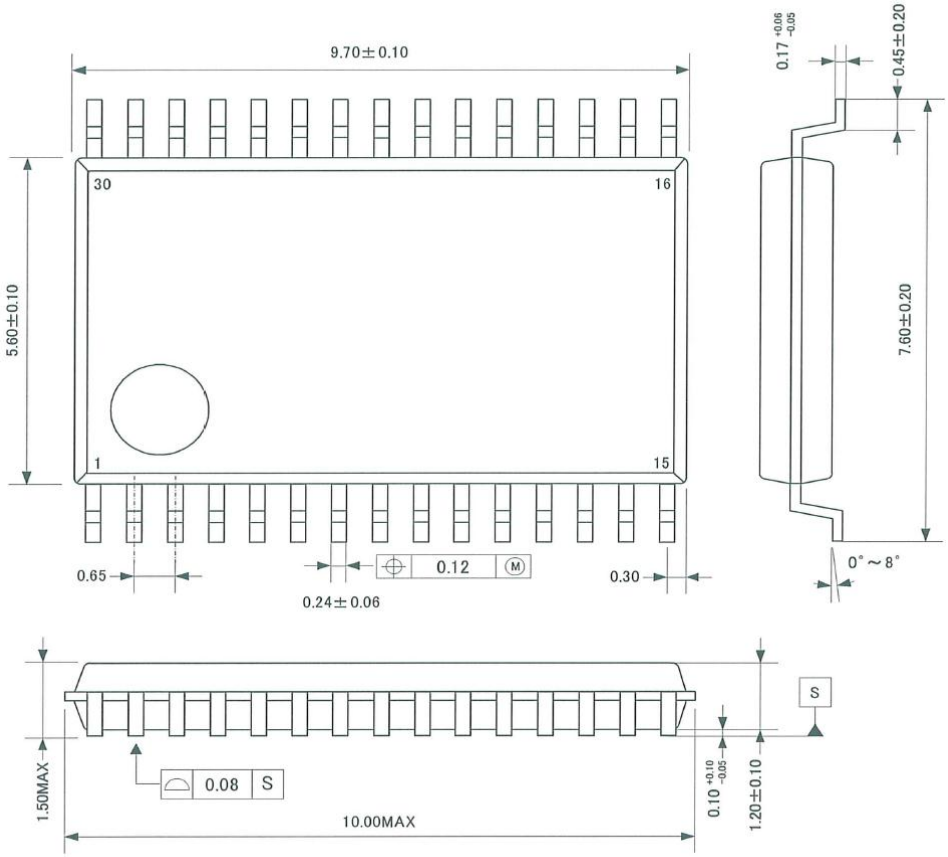
AK8135F is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 5

Power supply line – AK8135F has six power supply pins (VDD1-6) which deliver power to internal circuitry segments. A 0.1μF decoupling capacitor should be placed as close to each VDD pin as possible.

Ground pin connection – AK8135F has seven ground pins (GND1-7). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. 0.1μF decoupling capacitors placed at VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, and VDD7 should be grounded at close to the GND1pin, the GND2 pin, the GND3 pin, the GND4 pin, the GND5 pin, the GND6 pin, and the GND7 respectively.

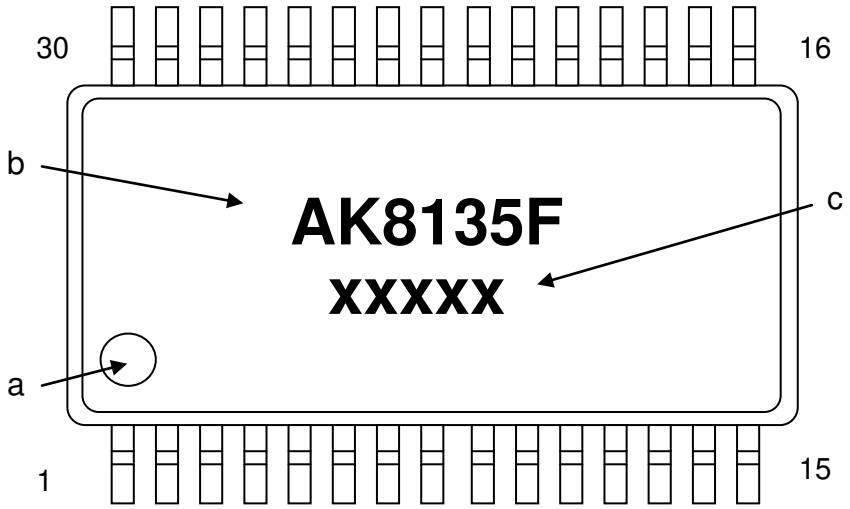
Crystal connection – Proper oscillation performance is susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form XI (Pin 3) and XO (Pin 1) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

Package Information

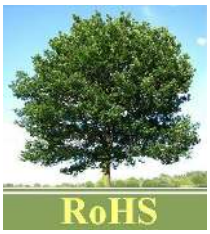


- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (5 digits)



- **RoHS Compliance**



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