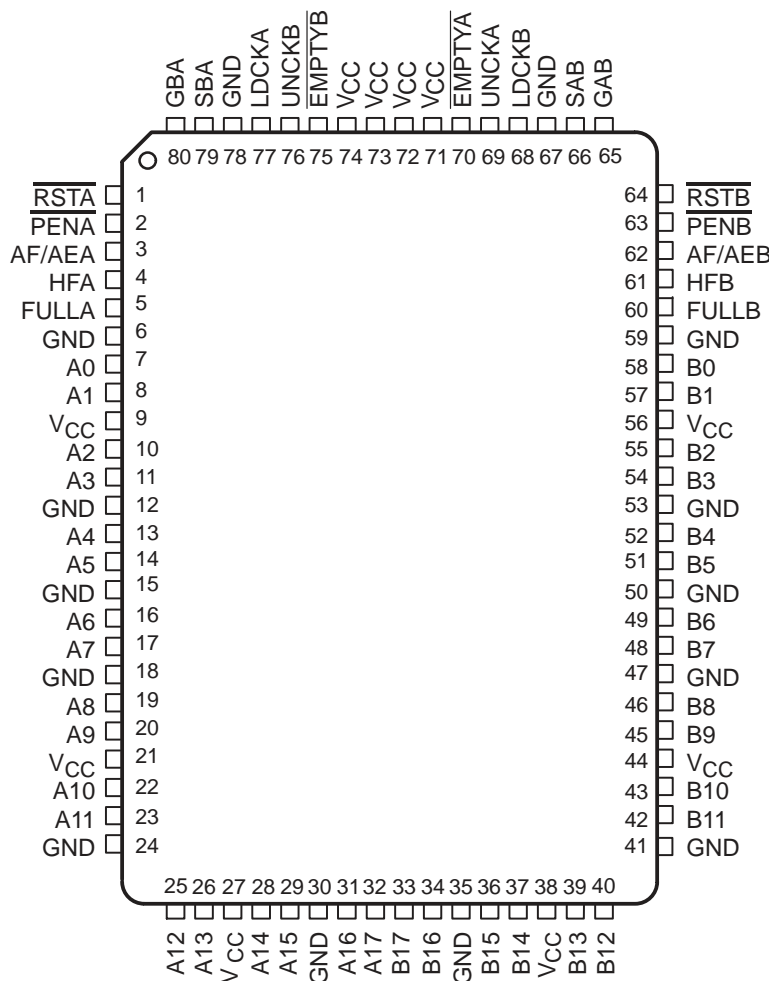


STROBED BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS206D – AUGUST 1991 – REVISED APRIL 1998

- Member of the Texas Instruments Widebus™ Family
- Advanced BiCMOS Technology
- Independent Asynchronous Inputs and Outputs
- Two Separate 512 × 18 FIFOs Buffering Data in Opposite Directions
- Programmable Almost-Full/Almost-Empty Flags
- Empty, Full, and Half-Full Flags
- Fast Access Times of 12 ns With a 50-pF Load and Simultaneous Switching Data Outputs
- Supports Clock Rates up to 67 MHz
- Package Options Include 80-Pin Quad Flat (PH) and 80-Pin Thin Quad Flat (PN) Packages

PH PACKAGE
(TOP VIEW)



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Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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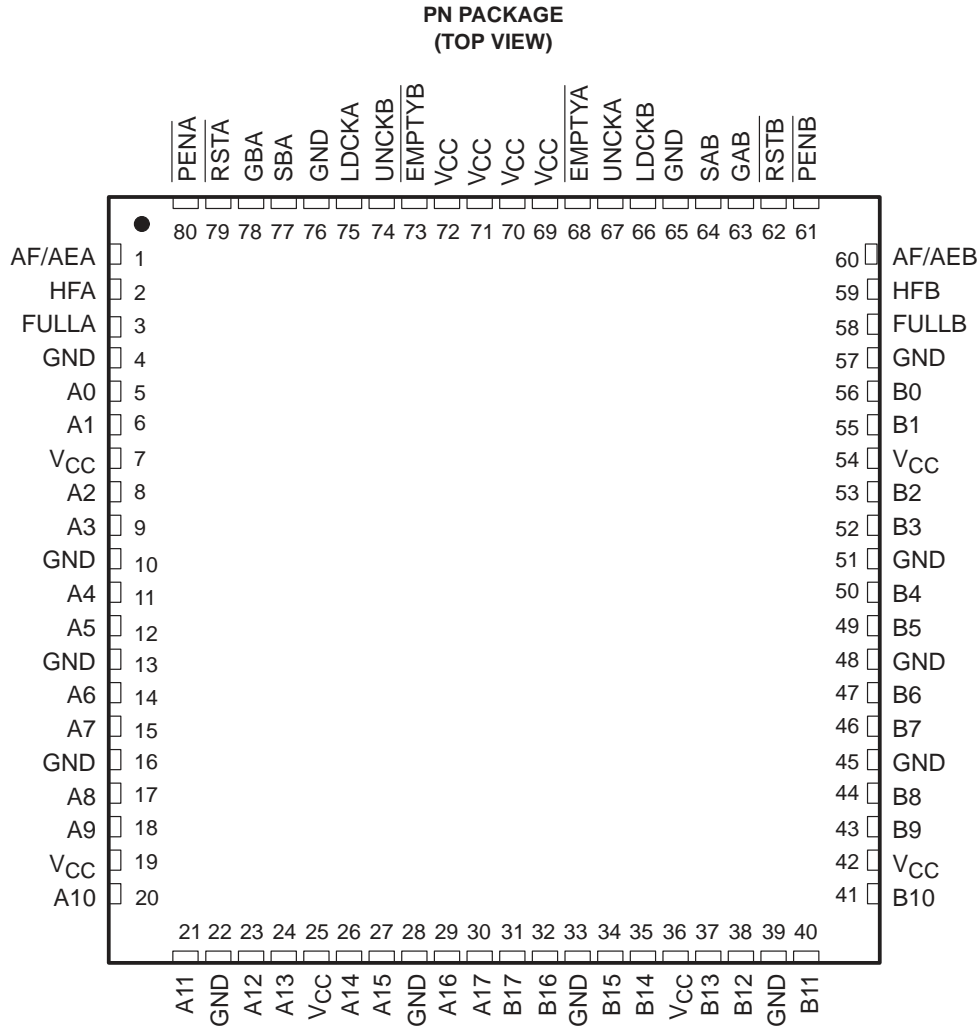
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SN74ABT7820

512 × 18 × 2

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description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ABT7820 is arranged as two 512 × 18-bit FIFOs for high speed and fast access times. It processes data at rates up to 67 MHz with access times of 12 ns in a bit-parallel format.

The SN74ABT7820 consists of bus-transceiver circuits, two 512 × 18 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable inputs (GAB and GBA) control the transceiver functions. The SAB and SBA control inputs select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the eight fundamental bus-management functions that can be performed with the SN74ABT7820.

The SN74ABT7820 is characterized for operation from 0°C to 70°C.



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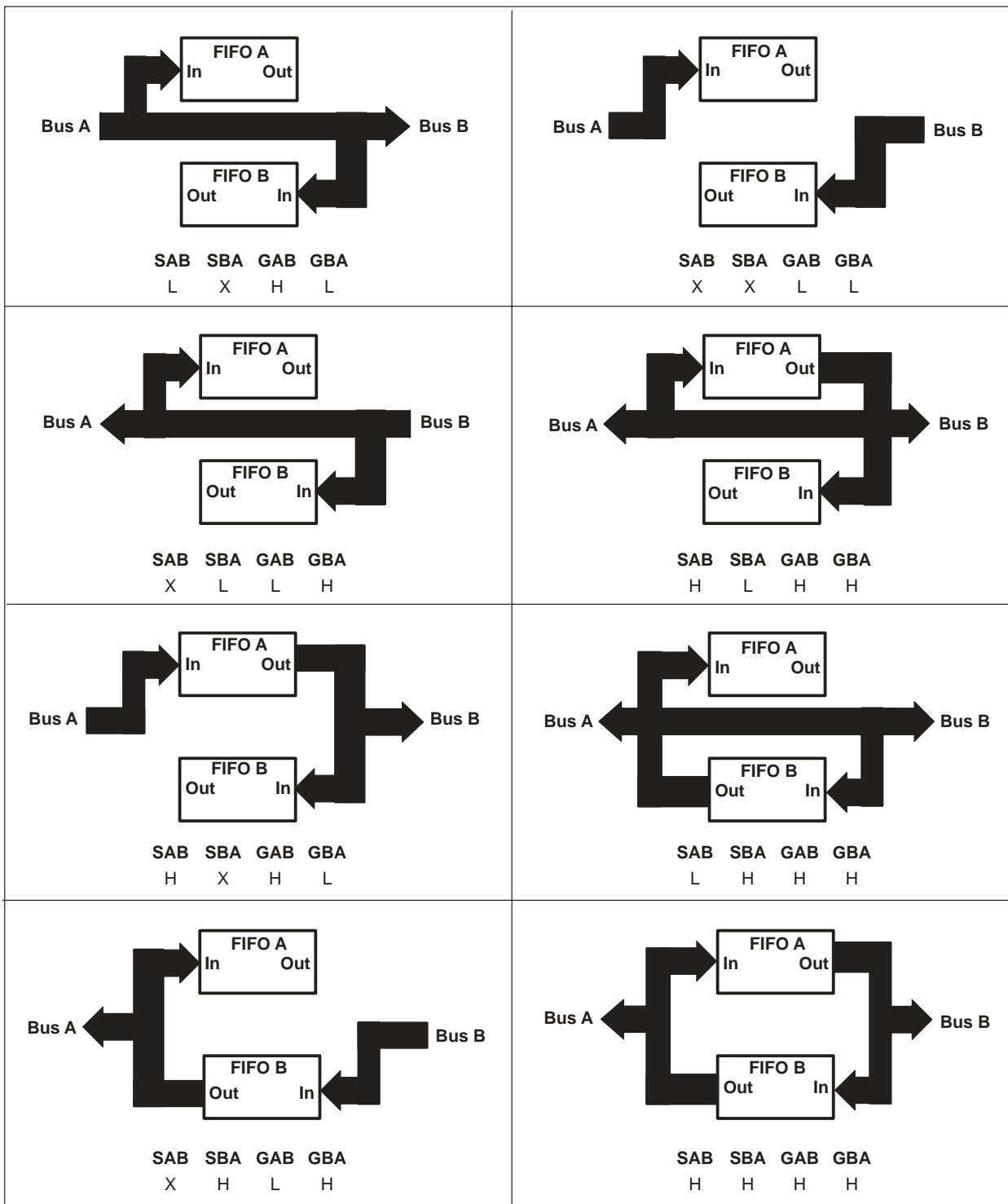


Figure 1. Bus-Management Functions

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SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SBA	SAB	A BUS	B BUS
L	L	Real-time B-to-A bus	Real-time A-to-B bus
H	L	FIFO B-to-A bus	Real-time A-to-B bus
L	H	Real-time B-to-A bus	FIFO A-to-B bus
H	H	FIFO B-to-A bus	FIFO A-to-B bus

OUTPUT-ENABLE CONTROL TABLE

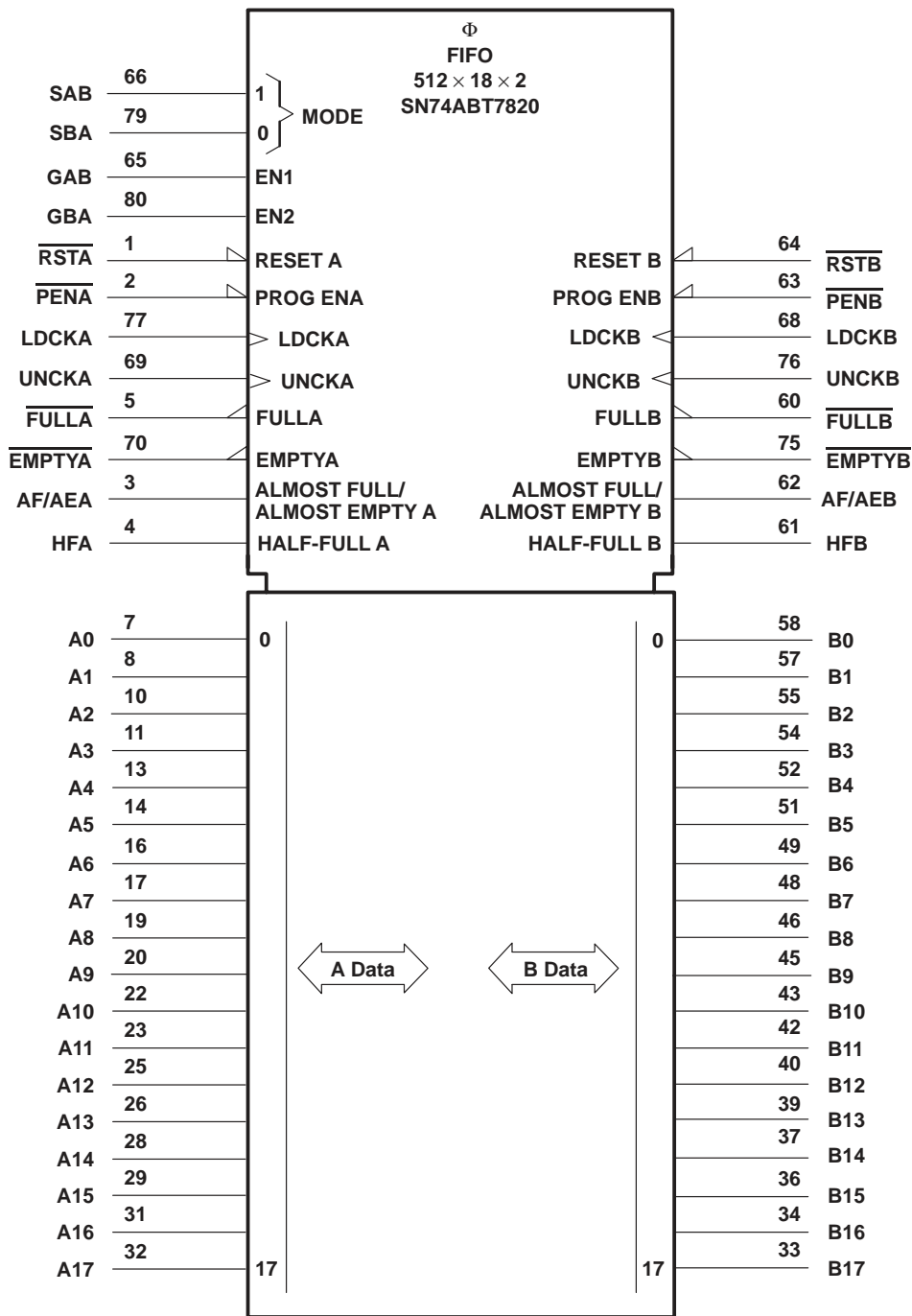
CONTROL		OPERATION	
GBA	GAB	A BUS	B BUS
L	L	Isolation/input to A bus	Isolation/input to B bus
H	L	A bus enabled	Isolation/input to B bus
L	H	Isolation/input to A bus	B bus enabled
H	H	A bus enabled	B bus enabled

Figure 1. Bus-Management Functions (Continued)

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the PH package.

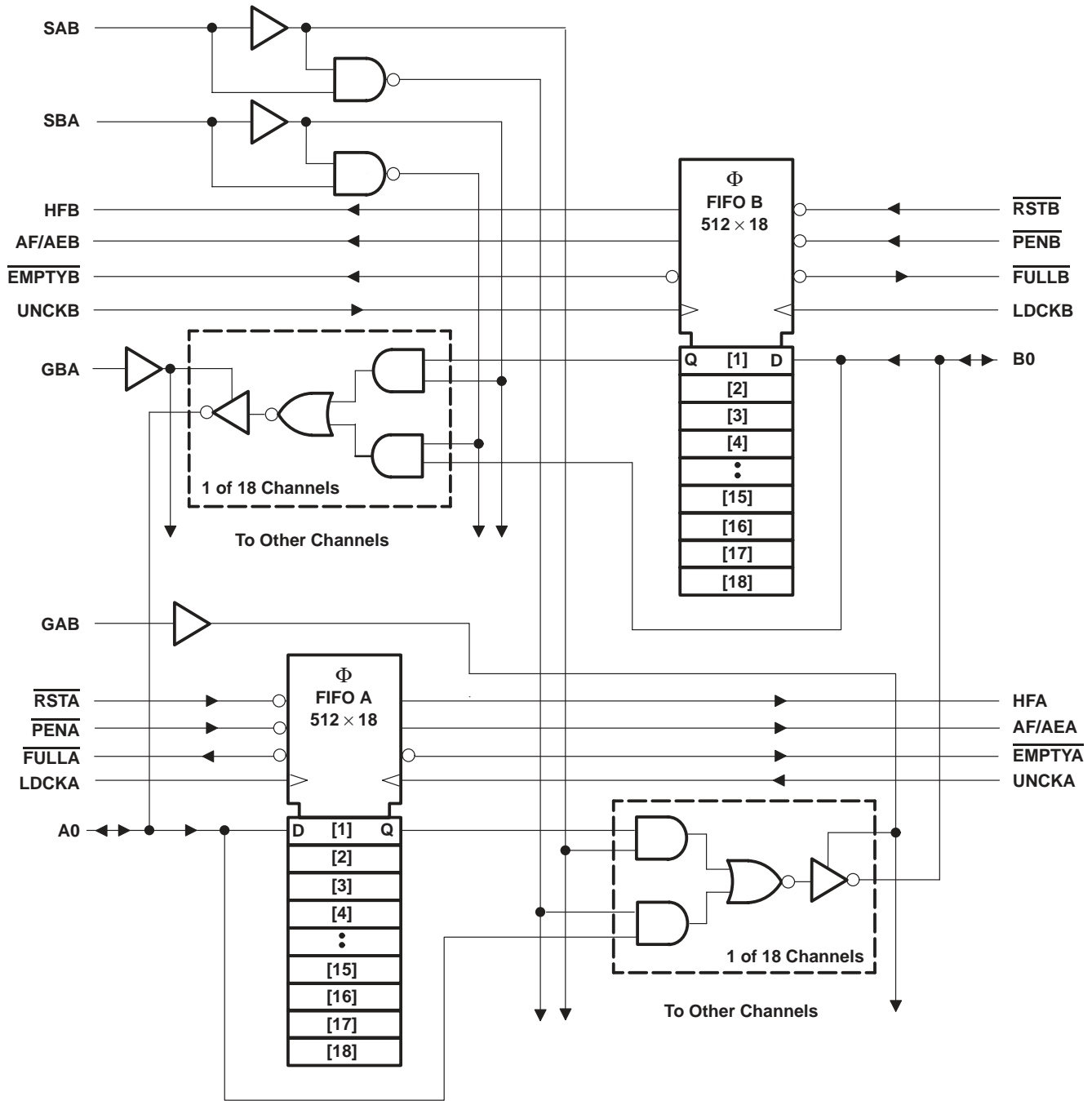
SN74ABT7820

512 × 18 × 2

STROBED BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

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logic diagram (positive logic)

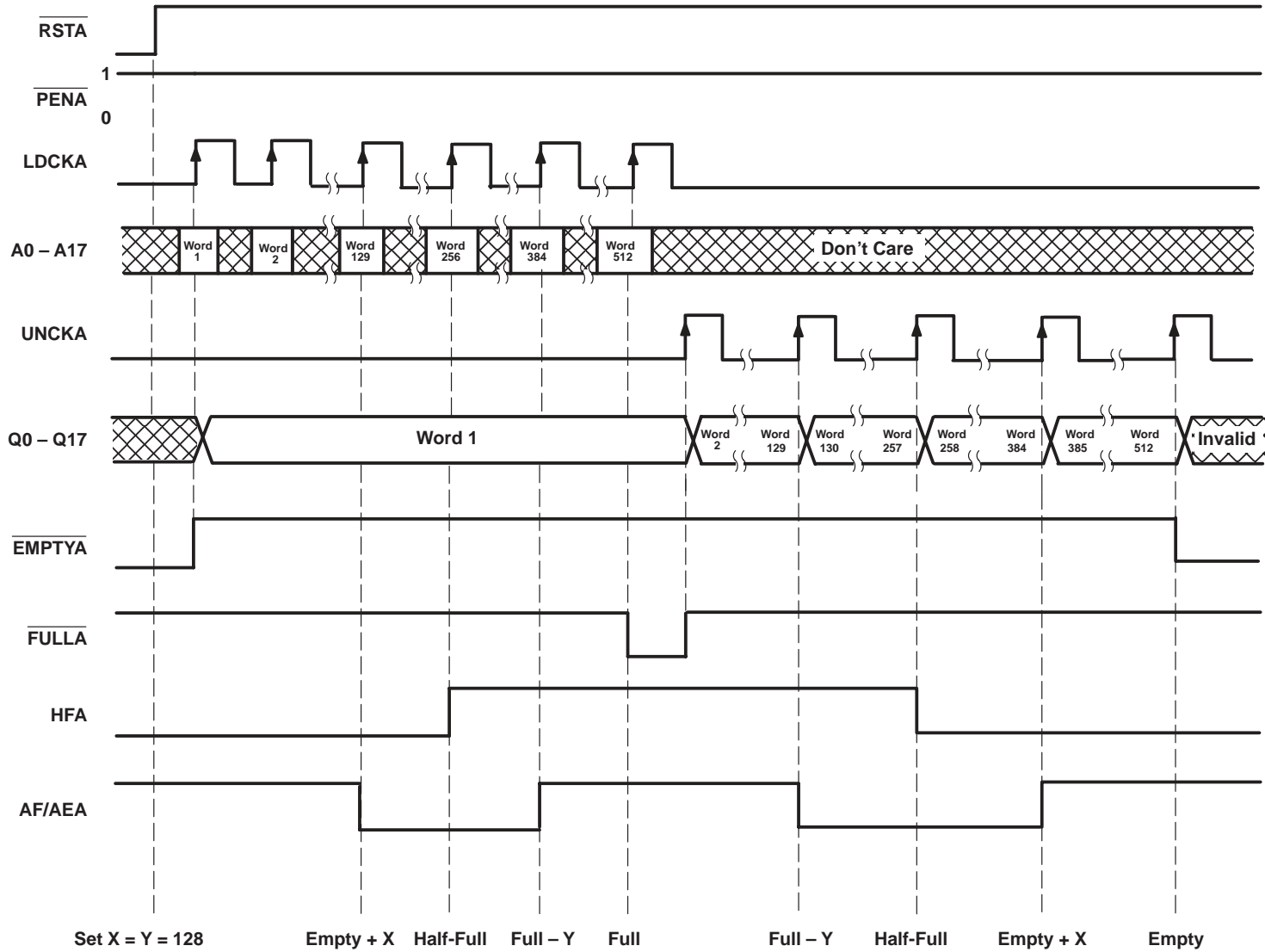


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Terminal Functions

TERMINAL	I/O	DESCRIPTION
A0–A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFO A almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AEA or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when FIFO A contains X or fewer words or (512 – Y) or more words. AF/AEA is set high after FIFO A is reset.
AF/AEB	O	FIFO B almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AEB or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when FIFO B contains X or fewer words or (512 – Y) or more words. AF/AEB is set high after FIFO B is reset.
B0–B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
$\overline{\text{EMPTYA}}$	O	FIFO A empty flag. $\overline{\text{EMPTYA}}$ is low when FIFO A is empty and high when FIFO A is not empty. $\overline{\text{EMPTYA}}$ is set low after FIFO A is reset.
$\overline{\text{EMPTYB}}$	O	FIFO B empty flag. $\overline{\text{EMPTYB}}$ is low when FIFO B is empty and high when FIFO B is not empty. $\overline{\text{EMPTYB}}$ is set low after FIFO B is reset.
$\overline{\text{FULLA}}$	O	FIFO A full flag. $\overline{\text{FULLA}}$ is low when FIFO A is full and high when FIFO A is not full. $\overline{\text{FULLA}}$ is set high after FIFO A is reset.
$\overline{\text{FULLB}}$	O	FIFO B full flag. $\overline{\text{FULLB}}$ is low when FIFO B is full and high when FIFO B is not full. $\overline{\text{FULLB}}$ is set high after FIFO B is reset.
GAB	I	Port-B output enable. B0–B17 outputs are active when GAB is high and in the high-impedance state when GAB is low.
GBA	I	Port-A output enable. A0–A17 outputs are active when GBA is high and in the high-impedance state when GBA is low.
HFA	O	FIFO A half-full flag. HFA is high when FIFO A contains 256 or more words and is low when FIFO A contains 255 or fewer words. HFA is set low after FIFO A is reset.
HFB	O	FIFO B half-full flag. HFB is high when FIFO B contains 256 or more words and is low when FIFO B contains 255 or fewer words. HFB is set low after FIFO B is reset.
LDCKA	I	FIFO A load clock. Data is written into FIFO A on a low-to-high transition of LDCKA when $\overline{\text{FULLA}}$ is high. The first word written into an empty FIFO A is sent directly to the FIFO A data outputs.
LDCKB	I	FIFO B load clock. Data is written into FIFO B on a low-to-high transition of LDCKB when $\overline{\text{FULLB}}$ is high. The first word written into an empty FIFO B is sent directly to the FIFO B data outputs.
$\overline{\text{PENA}}$	I	FIFO A program enable. After reset and before a word is written into FIFO A, the binary value on A0–A7 is latched as an AF/AEA offset value when $\overline{\text{PENA}}$ is low and LDCKA is high.
$\overline{\text{PENB}}$	I	FIFO B program enable. After reset and before a word is written into FIFO B, the binary value on B0–B7 is latched as an AF/AEB offset value when $\overline{\text{PENB}}$ is low and LDCKB is high.
$\overline{\text{RSTA}}$	I	FIFO A reset. A low level on $\overline{\text{RSTA}}$ resets FIFO A forcing $\overline{\text{EMPTYA}}$ low, HFA low, $\overline{\text{FULLA}}$ high, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFO B reset. A low level on $\overline{\text{RSTB}}$ resets FIFO B forcing $\overline{\text{EMPTYB}}$ low, HFB low, $\overline{\text{FULLB}}$ high, and AF/AEB high.
SAB	I	Port-B read select. SAB selects the source of B0–B17 read data. A low level selects real-time data from A0–A17. A high level selects the FIFO A output.
SBA	I	Port-A read select. SBA selects the source of A0–A17 read data. A low level selects real-time data from B0–B17. A high level selects the FIFO B output.
UNCKA	I	FIFO A unload clock. Data is read from FIFO A on a low-to-high transition of UNCKA when $\overline{\text{EMPTYA}}$ is high.
UNCKB	I	FIFO B unload clock. Data is read from FIFO B on a low-to-high transition of UNCKB when $\overline{\text{EMPTYB}}$ is high.



† SAB = GAB = H, GBA = L
 Operation of FIFO B is identical to that of FIFO A.

Figure 2. Timing Diagram for FIFO A†

offset values for AF/AE

The AF/AE flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). The offsets of a flag can be programmed from the input of its FIFO after it is reset and before any data is written to its memory. An AF/AE flag is high when its FIFO contains X or fewer words or $(512 - Y)$ or more words.

To program the offset values for AF/AEA, program enable ($\overline{\text{PENA}}$) can be brought low after FIFO A is reset and only when LDCKA is low. On the following low-to-high transition of LDCKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of LDCKA reprograms Y to the binary value on A0–A7 at the time of the second LDCKA low-to-high transition.

$\overline{\text{PENA}}$ can be brought back high only when LDCKA is low during the first two LDCKA cycles. $\overline{\text{PENA}}$ can be brought high at any time after the second LDCKA pulse returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 3). To use the default values of $X = Y = 128$ for AF/AEA, $\overline{\text{PENA}}$ must be tied high. No data is stored in the FIFO when its AF/AE offsets are programmed. The AF/AEB flag is programmed in the same manner. $\overline{\text{PENB}}$ enables LDCKB to program the AF/AEB offset values taken from B0–B7.

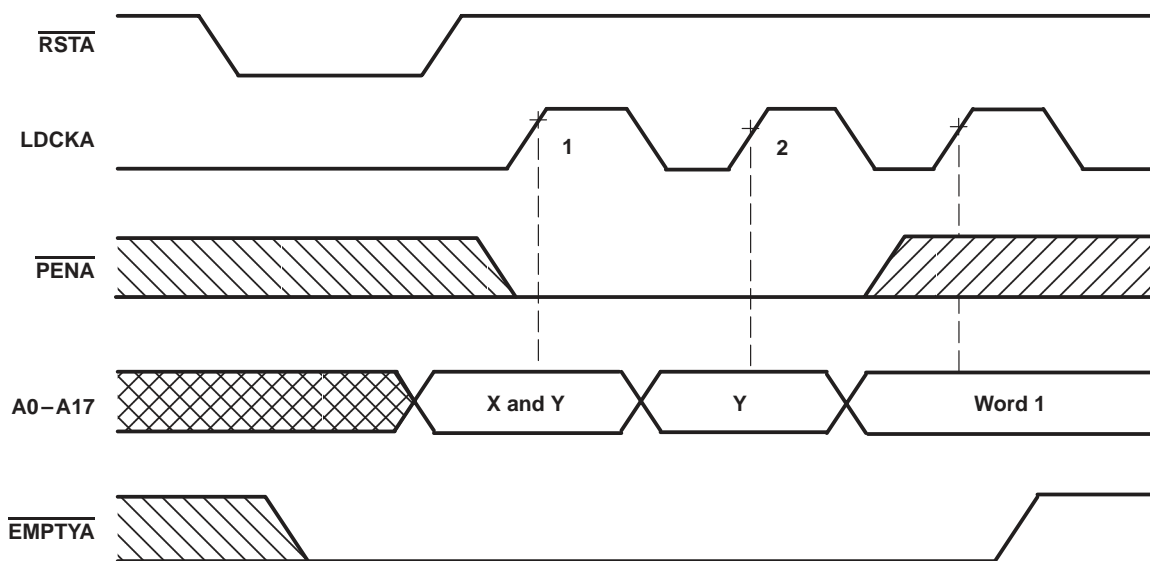


Figure 3. Programming X and Y Separately for AF/AEA

SN74ABT7820

512 × 18 × 2

STROBED BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	48 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): PH package	76°C/W
PN package	62°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_I Input voltage	0		V_{CC}	V
I_{OH} High-level output current			–12	mA
I_{OL} Low-level output current			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate			5	ns/V
T_A Operating free-air temperature	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2			
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 24\text{ mA}$			0.55	V
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND			±5	μA
I_{OZH}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			50	μA
I_{OZL}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$			-50	μA
I_O^\S		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-40	-100	-180	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		15	mA
			Outputs low		95	
			Outputs disabled		15	
C_i	Control inputs	$V_I = 2.5\text{ V}$ or 0.5 V		6		pF
C_o	Flags	$V_O = 2.5\text{ V}$ or 0.5 V		4		pF
C_{io}	A or B ports	$V_O = 2.5\text{ V}$ or 0.5 V		8		pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

		'ABT7820-15		'ABT7820-20		'ABT7820-25		'ABT7820-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	67		50		40		33		MHz
t_w	Pulse duration	LDCKA, LDCKB high	4	6	9	11	ns			
		LDCKA, LDCKB low	4	6	9	11				
		UNCKA, UNCKB high	4	6	9	11				
		UNCKA, UNCKB low	4	6	9	11				
		$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$ low	6	8	10	12				
t_{su}	Setup time	A0–A17 before LDCKA \uparrow and B0–B17 before LDCKB \uparrow	3	4	4	4	ns			
		$\overline{\text{PENA}}$ before LDCKA \uparrow and $\overline{\text{PENB}}$ before LDCKB \uparrow	5	5	5	5				
		LDCKA inactive before $\overline{\text{RSTA}}$ high and LDCKB inactive before $\overline{\text{RSTB}}$ high	3	3	4	4				
t_h	Hold time	A0–A17 after LDCKA \uparrow and B0–B17 after LDCKB \uparrow	0	0	0	0	ns			
		$\overline{\text{PENA}}$ after LDCKA low and $\overline{\text{PENB}}$ after LDCKB low	2	2	2	2				
		LDCKA inactive after $\overline{\text{RSTA}}$ high and LDCKB inactive after $\overline{\text{RSTB}}$ high	3	3	4	4				

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512 × 18 × 2

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7820-15			'ACT7820-20		'ACT7820-25		'ACT7820-30		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK, UNCK		67			50		40		33.3		MHz
t_{pd}	LDCKA↑, LDCKB↑	B/A	4		14	4	15	4	18	4	20	ns
	UNCKA↑, UNCKB↑		4	9	12	4	13.5	4	15	4	17	
$t_{pd}‡$	UNCKA↑, UNCKB↑	B/A	8									ns
t_{PLH}	LDCKA↑, LDCKB↑	EMPTYA, EMPTYB	4		14	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑		4		13	4	14	4	16	4	18	
t_{PHL}	RSTA low, RSTB low	EMPTYA, EMPTYB	6		16	6	16	6	18	6	20	ns
t_{PHL}	LDCKA↑, LDCKB↑	FULLA, FULLB	6		13	6	14	6	16	6	18	ns
t_{PLH}	UNCKA↑, UNCKB↑	FULLA, FULLB	6		15	6	15	6	17	6	19	ns
	RSTA low, RSTB low		8		20	8	20	8	22	8	22	
t_{pd}	LDCKA↑, LDCKB↑	AF/AEA, AF/AEB	8		16	8	17	8	18	8	20	ns
	UNCKA↑, UNCKB↑		8		16	8	17	8	18	8	20	
t_{PLH}	RSTA low, RSTB low	AF/AEA, AF/AEB	2		12	2	14	2	16	2	18	ns
t_{PLH}	LDCKA↑, LDCKB↑	HFA, HFB	8		15	8	15	8	17	8	19	ns
t_{PHL}	UNCKA, UNCKB	HFA, HFB	8		15	8	15	8	17	8	19	ns
	RSTA low, RSTB low		2		12	2	14	2	16	2	18	
t_{pd}	SAB/SBA§	B/A	2		10	2	11	2	12	2	14	ns
	A/B		2		9	2	10	2	11	2	13	
t_{en}	GBA/GAB	A/B	2		6.5	2	8	2	10	2	12	ns
t_{dis}	GBA/GAB	A/B	2		11	2	12	2	13	2	14	ns

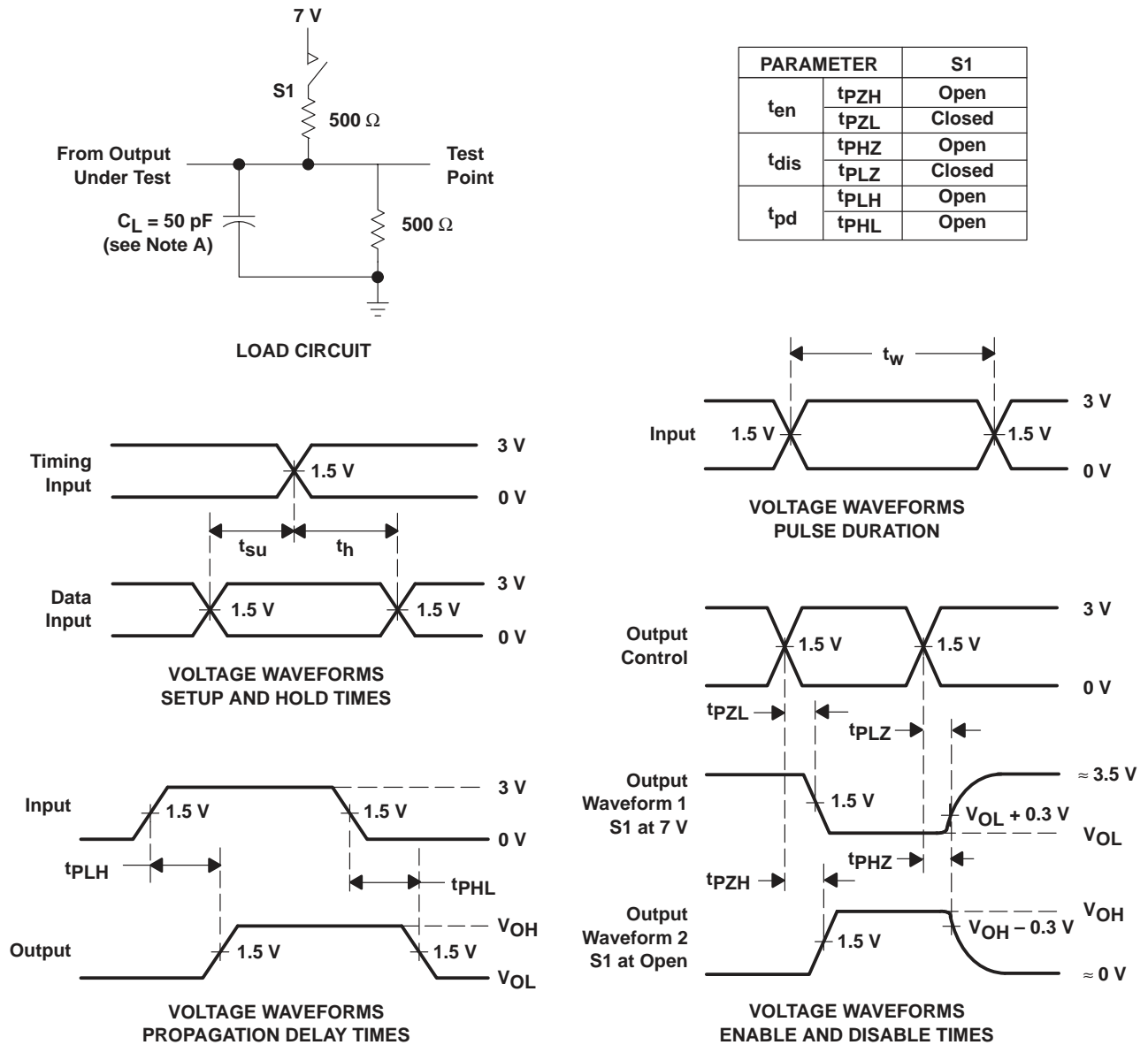
† All typical values are at 5 V, $T_A = 25^\circ\text{C}$.

‡ This parameter is measured with a 30-pF load (see Figure 5).

§ These parameters are measured with the internal output state of the storage register opposite that of the bus input.



PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

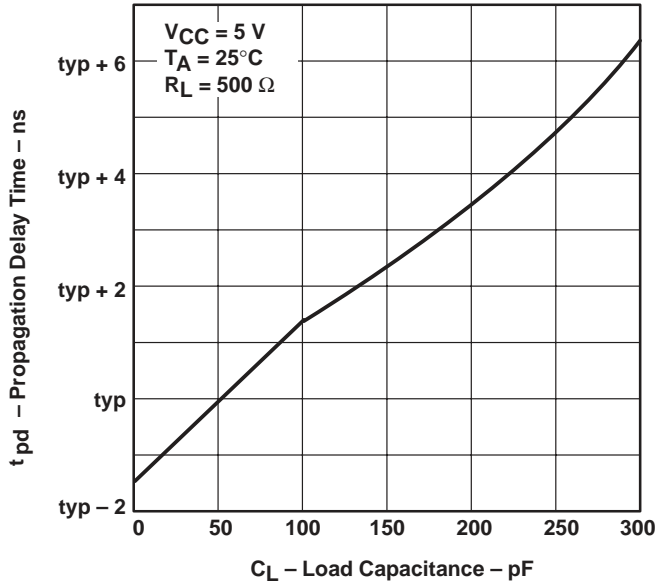


Figure 5

SUPPLY CURRENT
vs
CLOCK FREQUENCY

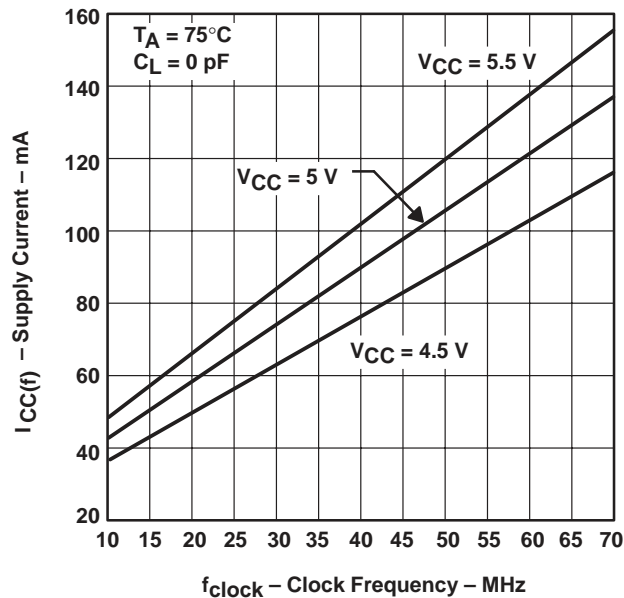


Figure 6

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