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# P-Channel NexFET™ Power MOSFET

Check for Samples: CSD25213W10

### **FEATURES**

- · Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- Gate-Source Voltage Clamp
- Gate ESD Protection
- RoHS Compliant
- Halogen Free

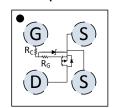
### **APPLICATIONS**

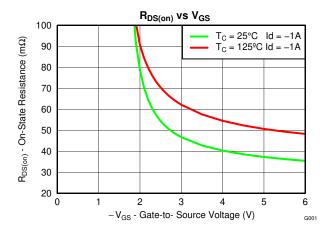
- Battery Management
- · Load Switch
- Battery Protection

### **DESCRIPTION**

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

**Top View** 





### **PRODUCT SUMMARY**

$V_{DS}$	Drain to Source Voltage	-20	V	
$Q_g$	Gate Charge Total (4.5V)	2.2	nC	
$Q_{gd}$	Gate Charge Gate to Drain	0.14	nC	
D	Drain to Source On	$V_{GS} = -2.5V$	54	mΩ
R <sub>DS(on)</sub>	Resistance	$V_{GS} = -4.5V$	39	mΩ
$V_{GS(th)}$	Threshold Voltage	-0.85	٧	

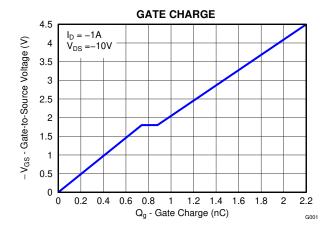
### **ORDERING INFORMATION**

Device	ce Package Media		Qty	Ship	
CSD25213W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel	

### **ABSOLUTE MAXIMUM RATINGS**

T <sub>A</sub> = 25°C	unless otherwise stated	VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	-20	٧
V <sub>GS</sub>	Gate to Source Voltage	-6.0	٧
I <sub>D</sub>	Continuous Drain Current, $T_A = 25^{\circ}C^{(1)}$	-1.6	Α
I <sub>DM</sub>	Pulsed Drain Current, T <sub>A</sub> = 25°C <sup>(2)</sup>	-16	Α
I <sub>G</sub>	Continuous Gate Clamp Current <sup>(3)</sup>	-5	mA
$P_D$	Power Dissipation <sup>(1)</sup>	1	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1)  $R_{\theta JA} = 75^{\circ}\text{C/W}$  on  $1\text{in}^2$  Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300µs, duty cycle ≤2%
- (3) Limited by gate resistance.





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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Ch	aracteristics				•	
BV <sub>DSS</sub>	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
BV <sub>GSS</sub>	Gate to Source Voltage;	$V_{DS} = 0V, I_{G} = -250\mu A$	-6.0			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -10V			-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -6V$			-100	nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.60	-0.85	-1.10	V
	Drain to Source On Resistance	$V_{GS} = -2.5V, I_D = -1A$		54	67	mΩ
R <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -1A$		39	47	mΩ
9 <sub>fs</sub>	Transconductance	$V_{DS} = -10V, I_{D} = -1A$		6.2		S
Dynamic	Characteristics				•	
C <sub>ISS</sub>	Input Capacitance			368	478	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 10kHz$		148	192	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			7.8	10.1	pF
R <sub>G</sub>	Series Gate Resistance			20		Ω
R <sub>C</sub>	Series Clamp Resistance			5000		Ω
Qg	Gate Charge Total (-4.5V)			2.2	2.9	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	V 10V I 1A		0.14		nC
Q <sub>gs</sub>	Gate Charge Gate to Source	$V_{GS} = -2.5V, I_D = -1A$ $V_{GS} = -4.5V, I_D = -1A$ $V_{DS} = -10V, I_D = -1A$ $V_{DS} = 0V, V_{DS} = -10V, f = 10kHz$ $V_{DS} = -10V, I_D = -1A$ $V_{DS} = -10V, V_{GS} = 0V$ $V_{DS} = -10V, I_F = -1A,$		0.74		nC
Q <sub>g(th)</sub>	Gate Charge at Vth			0.43		nC
Q <sub>OSS</sub>	Output Charge	$V_{DS} = -10V, V_{GS} = 0V$		2.5		nC
t <sub>d(on)</sub>	Turn On Delay Time			510		ns
t <sub>r</sub>	Rise Time	$V_{DS} = -10V$ , $V_{GS} = -2.5V$ , $I_{D} = -1A$		520		ns
t <sub>d(off)</sub>	Turn Off Delay Time			1000		ns
t <sub>f</sub>	Fall Time			970		ns
Diode Ch	naracteristics					
V <sub>SD</sub>	Diode Forward Voltage	$I_S = -1A$ , $V_{GS} = 0V$		-0.77	-1	V
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{DS} = -10V, I_F = -1A,$ di/dt = 200A/ $\mu$ s		4.0		nC
t <sub>rr</sub>	Reverse Recovery Time	$V_{DS} = -10V, I_F = -1A,$ di/dt = 200A/ $\mu$ s		11		ns

## THERMAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

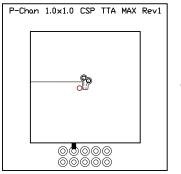
	PARAMETER	MIN	TYP	MAX	UNIT
В	Junction to Ambient Thermal Resistance <sup>(1)</sup>		75		°C/W
$R_{\theta JA}$	Junction to Ambient Thermal Resistance (2)		265		°C/W

- (1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.
   (2) Device mounted on FR4 material with minimum Cu mounting area.

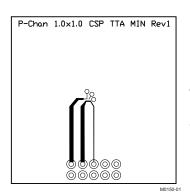
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Max  $R_{\theta JA} = 90^{\circ}C/W$ when mounted on 1inch<sup>2</sup> of 2 oz. Cu.



Max  $R_{\theta JA} = 333^{\circ}C/W$  when mounted on minimum pad area of 2 oz. Cu.

## TYPICAL MOSFET CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

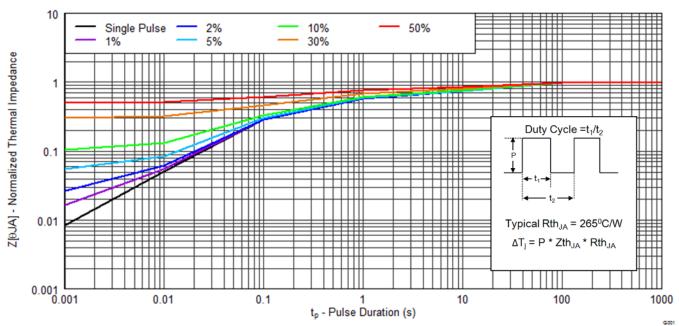


Figure 1. Transient Thermal Impedance

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1.1

-V<sub>GS(th)</sub> - Threshold Voltage (V)



## TYPICAL MOSFET CHARACTERISTICS (continued)

## (T<sub>A</sub> = 25°C unless otherwise stated)

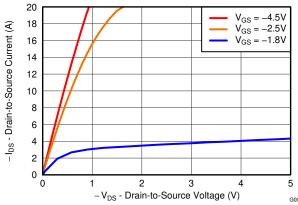
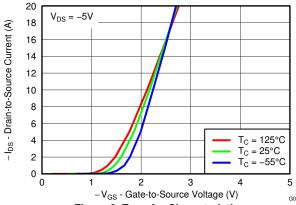


Figure 2. Saturation Characteristics



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Figure 3. Transfer Characteristics

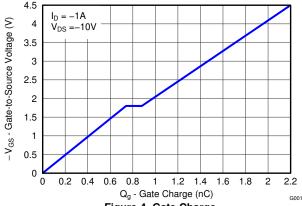
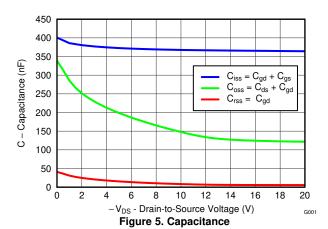


Figure 4. Gate Charge

 $I_D = -250uA$ 



100  $T_C = 25^{\circ}C$  Id = -1A $R_{DS(on)}$  - On-State Resistance  $(m\Omega)$ 90  $T_C = 125^{\circ}C \text{ Id} = -1A$ 80 70 60 50 40 30 20 3 4 -V<sub>GS</sub> - Gate-to- Source Voltage (V)

Figure 7. On-State Resistance vs. Gate-to-Source Voltage



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## TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

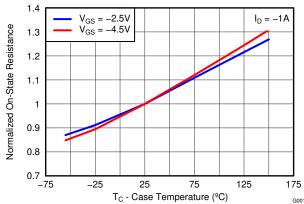


Figure 8. Normalized On-State Resistance vs. Temperature

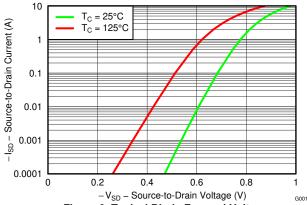


Figure 9. Typical Diode Forward Voltage

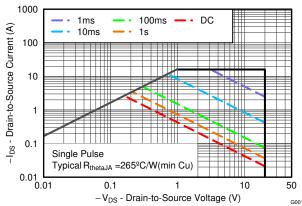


Figure 10. Maximum Safe Operating Area

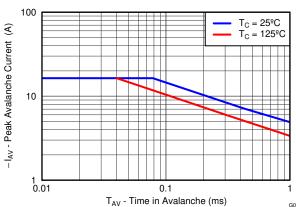


Figure 11. Single Pulse Unclamped Inductive Switching

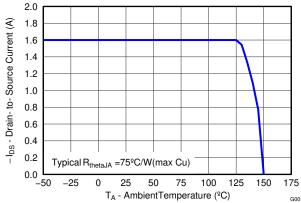


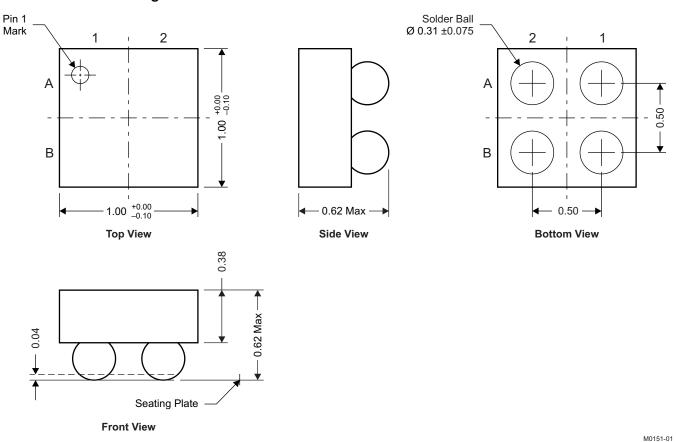
Figure 12. Maximum Drain Current vs. Temperature

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**MECHANICAL DATA** 

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## CSD25213W10 Package Dimensions

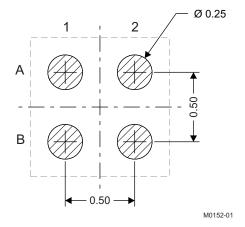


NOTE: All dimensions are in mm (unless otherwise specified)

## **Pin Configuration Table**

<u> </u>							
POSITION	DESIGNATION						
A1	Gate						
B1	Drain						
A2, B2	Source						

### **Land Pattern Recommendation**



NOTE: All dimensions are in mm (unless otherwise specified)

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## PACKAGE OPTION ADDENDUM

10-Dec-2020

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25213W10	ACTIVE	DSBGA	YZB	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	213	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25213W10	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	2.0	8.0	Q1

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### \*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
CSD25213W10	DSBGA	YZB	4	3000	182.0	182.0	20.0	

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