# CDP1858/3, CDP1858C/3

## High-Reliability 4-Bit Latch and Decoder Memory Interface

**Features:**

- *Provides easy connection of memory devices to CDP1802 microprocessor*
- *Non-inverting fully buffered data transfer*

The RCA-CDP1858/3 and CDP1858C/3 are CMOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the 1800-series microprocessor multiplexed address bus at maximum clock frequency.

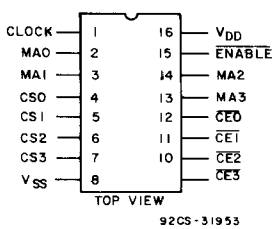
The CDP1858/3 is functionally identifed to the CDP1858C/3. The CDP1858/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1858C/3 has a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1858/3 interfaces the 1800-series microprocessor address bus and up to 32 CDP1822 256 x 4 RAM's to provide a 4K byte RAM system. No additional components are required. The CDP1858/3 generates the chip selects required by the CDP1822 RAM. The chip select outputs are a function of the address bits connected to inputs MA0 through MA3.

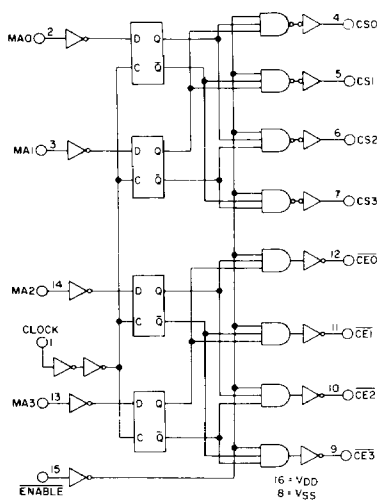
The MA0-MA3 address bits are latched at the trailing edge of TPA (generated by the CDP1802). When $\overline{ENABLE}$ = 1 ($V_{DD}$), the $\overline{CS}$ outputs = 0 ($V_{SS}$), and the CE outputs = 1. When $\overline{ENABLE}$ = 0, the outputs are enabled and correspond to the binary decode of the inputs. The $\overline{ENABLE}$ input can be used for memory system expansion.

The CDP1858/3 is also compatible with non-multiplexed address bus microprocessors. By connecting the CLOCK input to 1 ($V_{DD}$), the latches are in the data following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1858/3 and CDP1858C/3 are supplied in 16-lead, dual-in-line side-brazed ceramic packages (D suffix) that conform to the requirements and dimensions specified in MIL-38510 Case Outline D-2. Other package styles may be available on a special order basis.

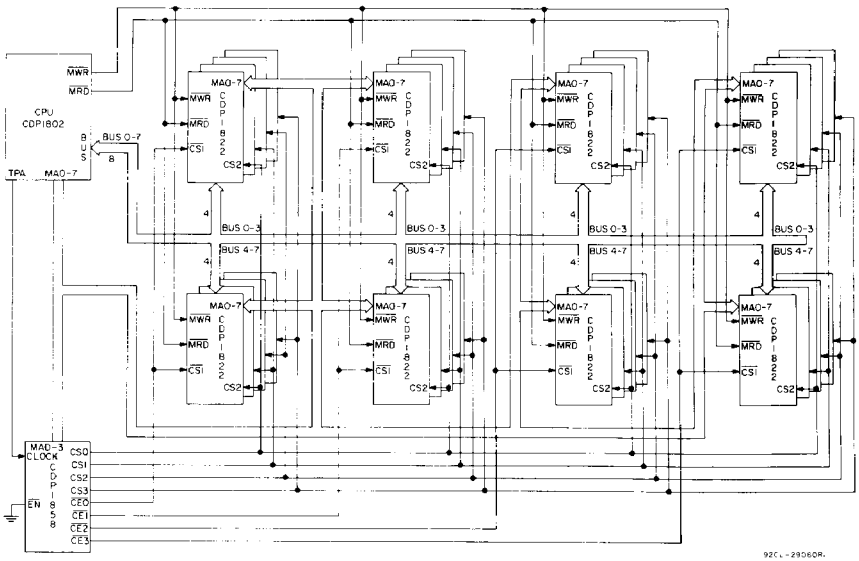



**TERMINAL ASSIGNMENT**




*Functional diagram.*

# CDP1858/3, CDP1858C/3




*4K byte RAM system using the CDP1858 and CDP1822.*

**STATIC ELECTRICAL CHARACTERISTICS**
**5-V Data Apply to the CDP1858 and the CDP1858C.**
**10-V Data Apply to the CDP1858 only.**

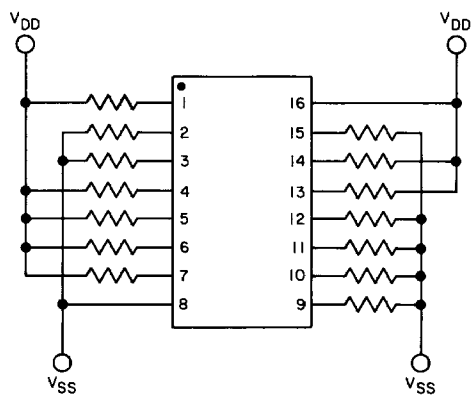
| CHARACTERISTIC | | TEST CONDITIONS | | | LIMITS CDP1858 CDP1858C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | +25/-55° C | | +125° C | | |
| | | $V_{DD}$ (V) | $V_I$ (V) | $V_O$ (V) | Min. | Max. | Min. | Max. | |
| Quiescent Device Current, | $I_L$ | 5 | 0, 5 | — | — | 100 | — | 1000 | μA |
| | | 10 | 0, 10 | — | — | 100 | — | 1000 | |
| Output Low Drive (Sink) Current | $I_{OL}$ | 5 | 0, 5 | 0.4 | 1.6 | — | 1 | — | mA |
| | | 10 | 0, 10 | 0.5 | 3.6 | — | 2.2 | — | |
| Output High Drive (Source) Current, | $I_{OH}$ | 5 | 0, 5 | 4.6 | -1.6 | — | -1 | — | |
| | | 10 | 0, 10 | 9.5 | -3.6 | — | -2.2 | — | |
| Input Leakage Current, | $I_{IN}$ | 5 | 0, 5 | — | — | ±1 | — | ±5 | μA |
| | | 10 | 0, 10 | — | — | ±1 | — | ±5 | |

# CDP1858/3, CDP1858C/3

**DECODE TRUTH TABLE**

| $\overline{\text{ENABLE}}$ | DATA INPUTS | | CS0 | CS1 | CS2 | CS3 | $\overline{\text{CE0}}$ | $\overline{\text{CE1}}$ | $\overline{\text{CE2}}$ | $\overline{\text{CE3}}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | MA1 | MA0 | | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | NOT AFFECTED BY MA1, MA0 | | | |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | | | | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | | | | |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | | | | |
| | MA3 | MA2 | | | | | | | | |
| 0 | 0 | 0 | NOT AFFECTED BY MA3, MA2 | | | | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | | | | | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | | | | | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | | | | | 1 | 1 | 1 | 0 |
| 1 | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

X = MA3, MA2, MA1, MA0 DON'T CARE




ALL RESISTORS 47 kΩ (± 20%)

92CS-39671

| TYPE NO. | $V_{DD}$ | TEMP. | TIME |
|---|---|---|---|
| CDP1858/3 | 11 V ± 0.5 V | + 125°C | 160 Hrs. MIN. |
| CDP1858C/3 | 7 V ± 0.5 V | + 125°C | 160 Hrs. MIN. |

*Static burn-in circuit.*