User's Guide

ADS8332EVMV2-PDK Evaluation Module

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ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS8332 evaluation module (EVM) performance demonstration kit (PDK). The ADS8332 is a low-power, 16-bit, 500k samples per-second (SPS) successive approximation (SAR) analog-to-digital converter (ADC) with an 8-to-1 multiplexer (mux) input. Each input channel on the device supports unipolar input ranges of 0 V to 4.096 V with single-supply operation. The EVM-PDK eases the evaluation of ADS8332 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

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1 Overview

The ADS8332EVMV2-PDK is a platform for evaluating the performance of the ADS8332 SAR ADC, which is an 8-channel, 16-bit, 4.096-V, multiplexed input ADC device. The evaluation kit includes the ADS8332EVMV2 board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS8332EVMV2 board includes the ADS8332 SAR ADC, all the peripheral analog circuits, and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

1. Provides a communication interface from the EVM to the computer through a USB port
2. Provides the digital input and output signals necessary to communicate with the ADS8332EVMV2
3. Supplies power to all active circuitry on the ADS8332EVMV2 board

Along with the ADS8332EVMV2 and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS8332	SBAS363
OPA320	SBOS513
REF6041	SBOS708
TPS7A4700	SBVS204

1.1 ADS8332EVMV2-PDK Features

The ADS8332EVMV2-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8332 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS8332 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Windows 7® and Windows 8®, 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS8332EVMV2 Features

The ADS8332EVMV2 includes the following features:

- Onboard SMA connectors and RC input filters
- Jumper-selectable onboard 0.2-V common pin supply
- Jumper-selectable buffer between the multiplexer and the ADC
- Onboard ultralow-noise low-dropout (LDO) regulator for excellent 5.2-V single-supply regulation of the ADC and onboard voltage reference.

2 EVM Analog Interface

The ADS8332EVMV2 is designed for easy interfacing to analog sources. The Samtec™ connector provides a convenient 16-pin, single-row, header J1 accessing channels IN0-IN7 of the device. In addition, four SMA connectors, J-1 to J-4, provide a high quality connection to channels IN0, IN1, IN6, and IN7. Figure 2-1 shows the ADS8332EVMV2 analog input connections, input buffers, and input RC filters for channels IN0 to IN7. Table 2-1 lists the analog interface connections for header J1 and Table 2-2 lists the analog interface connections for the SMA connectors.

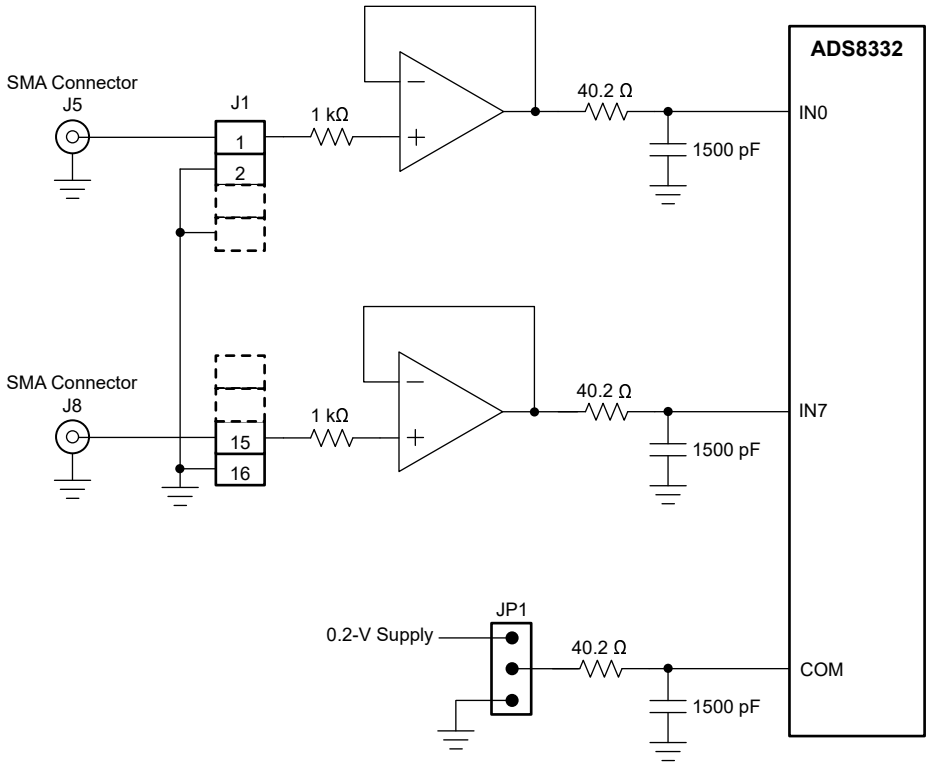

Figure 2-1. ADS8332EVMV2 Analog Input Connections for Channels IN0 to IN7

Table 2-1. J1 Header Analog Interface Connections

Header Pin Number	Signal	Description
J1.1	IN0	Positive analog input for channel IN0
J1.3	IN1	Positive analog input for channel IN1
J1.5	IN2	Positive analog input for channel IN2
J1.7	IN3	Positive analog input for channel IN3
J1.9	IN4	Positive analog input for channel IN4
J1.11	IN5	Positive analog input for channel IN5
J1.13	IN6	Positive analog input for channel IN6
J1.15	IN7	Positive analog input for channel IN7
J1.2, J1.4, J1.6, J1.8, J1.10, J1.12, J1.14, J1.16	GND	Ground connections

Table 2-2. SMA Analog Interface Connections

SMA Connector	Signal	Description
J5	IN0	Analog input for channel IN0
J6	IN1	Analog input for channel IN1
J7	IN6	Analog input for channel IN6
J8	IN7	Analog input for channel IN7

2.1 ADS8332EVMV2 Onboard Reference

The ADS8332EVMV2 incorporates an onboard 4.096-V reference, REF6041 (U9). With a reference of 4.096-V the full-scale range of the ADS8332 is 0 V to 4.096 V. The output of the REF6041 is buffered internally. Testpoint REF allows the reference voltage to be monitored. The schematic for the reference circuit is shown in Figure 2-2.

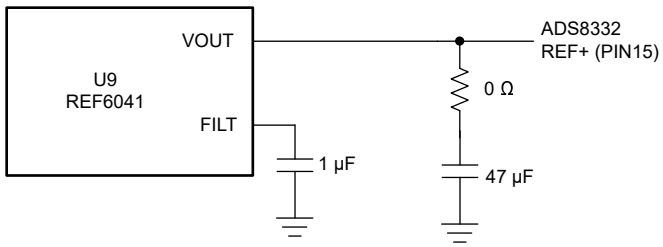

Figure 2-2. REF6041 4.096-V Onboard Reference Source

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS8332 ADC (over serial interface) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS8332EVMV2-PDK platform. After the hardware is initialized, the EEPROM is no longer used.

3.1 ADS8332 Digital Interface

The ADS8332EVMV2-PDK communicates with the PHI controller through SPI connections. The PHI controller is configured to operate at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

Socket strip connector J2 provides the digital I/O connections between the ADS8332EVMV2 board and the PHI controller.

Table 3-1 summarizes the pin-outs for connector J2.

Table 3-1. Digital I/O Connections for Connector J2

Pin Number	Signal	Description
J2.1	EVM_REG_5V5	5.5-V power supply from the PHI to the ADS8332EVMV2
J2.3	GND	Ground connection
J2.18	SDI	Serial data input connection
J2.20	CONVST	Active high logic input to control start of conversion
J2.22	CS	Chip select, active low
J2.24	SCLK	Clock input for serial interface
J2.50	DVDD	3.3-V digital supply from the PHI controller board
J2.56	EVM_ID_SDA	Serial data for the EEPROM (U10)
J2.58	EVM_ID_SCL	Serial clock for the EEPROM (U10)
J2.59	EVM_ID_PWR	Power supply used only to power the EEPROM (U10) on the EVM board
J2.60	GND	Ground connection

4 Power Supplies

The ADS8332 ADC analog supply (AVDD) is provided by a low-noise linear regulator (TPS7A4700). The regulator uses a 5.5-V supply out of a switching regulator from the PHI controller to generate a quiet and stable 5.2-V supply output. The 3.3-V supply to the digital supply of the ADS8332 is provided directly by an LDO from the PHI controller. The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper filled areas where possible between bypass capacitors and their loads to minimize inductance along the load current path.

When using the ADS8332EVMV2 in conjunction with the PHI controller, the PHI controller supplies the AVDD and DVDD supply. Do not supply external power supply voltages.

5 ADS8332EVMV2-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS8332EVMV2-PDK.

5.1 Default Jumper Settings

Make sure jumpers JP1, JP2, and J4 are in the default configuration while interfacing the ADS8332EVMV2 board with the PHI controller as described in Table 5-1. The jumpers can be reconfigured to allow for different types of operation.

Figure 5-1 details the default jumper settings.Table 5-1 explains the configuration for these jumpers.

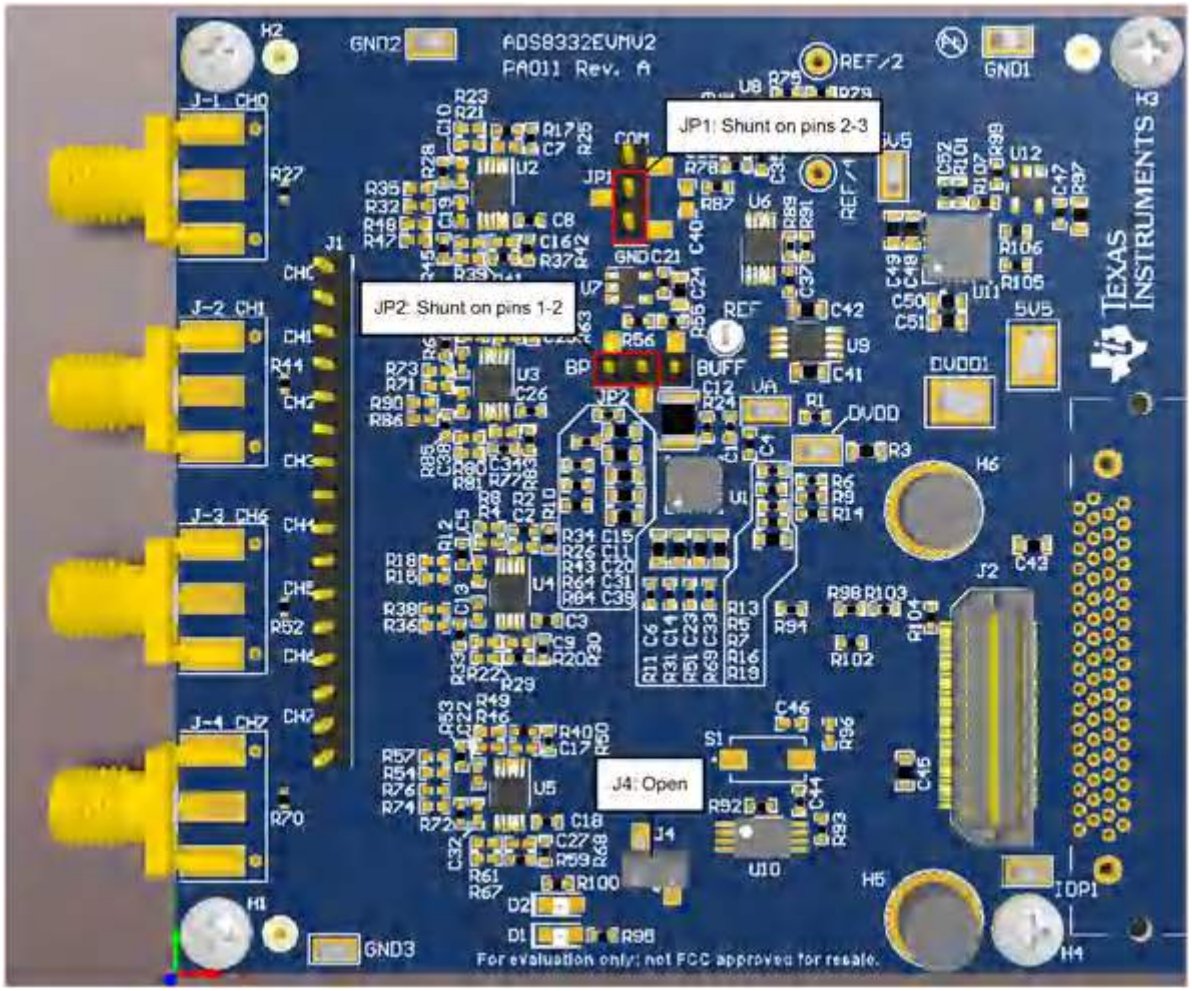

Figure 5-1. ADS8332EVMV2 Default Jumper Settings

Table 5-1. Default Jumper Configuration

Jumper	Function	Default Position	Description
JP1	Common pin voltage	Shunt on pins 2-3	Shunt on pins 2-3 select ground as the common pin voltage
JP2	Multiplexer output buffer	Shunt on pins 1-2	Shunt on pins 1-2 selects to bypass the buffer between MUXOUT and ADCIN
J4	EEPROM write enable	Open	Open enables write protect for the EEPROM

5.2 EVM Graphical User Interface (GUI) Software Installation

The following steps list the directions to install the software.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS8332EVMV2-PDK, and run the GUI installer to install the EVM GUI software. Administrator privileges on the PC are required in order to install the EVM software. Accept the license agreements and follow the on-screen instructions shown in Figure 5-2 in order to complete the installation.

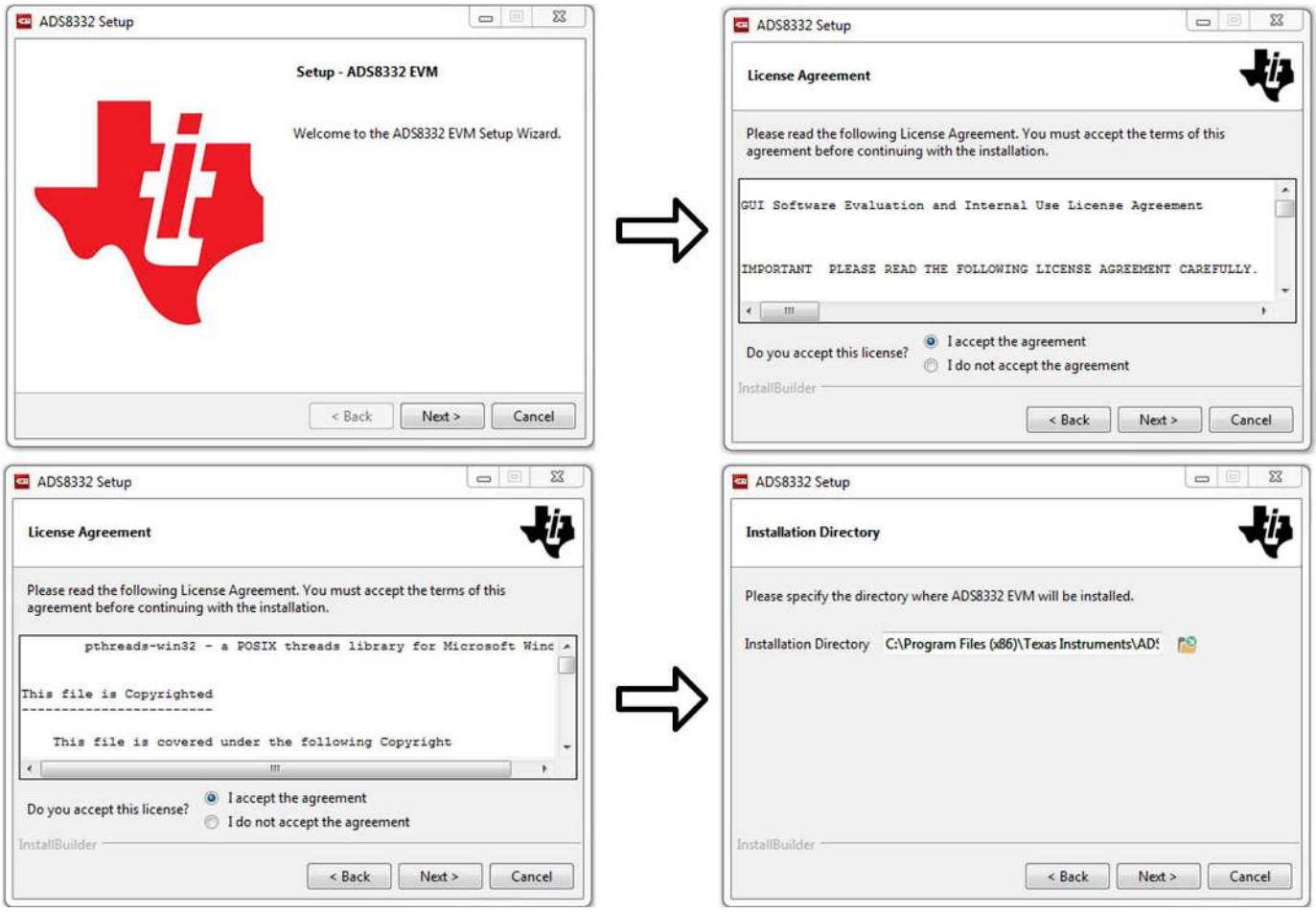

Figure 5-2. Software Installation Prompts

As a part of the ADS8332EVMV2 GUI installation, a prompt with a *Device Driver Installation* appears on the screen, as shown in Figure 5-3. Click *Next* to proceed.

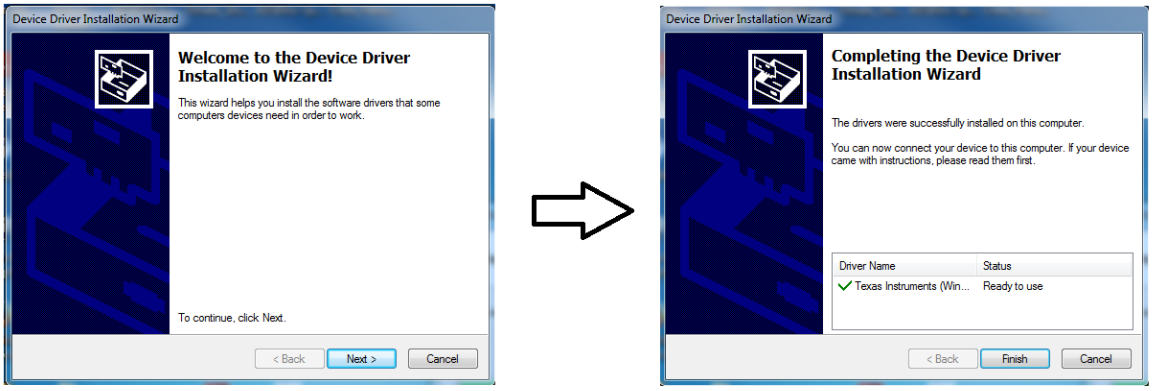

Figure 5-3. ADS8332 Device Driver Installation Wizard Prompts

Note

A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS8332EVMV2-PDK requires LabVIEW™ Run-Time Engine, and may prompt for the installation of this software, as shown in Figure 5-4, if not already installed.

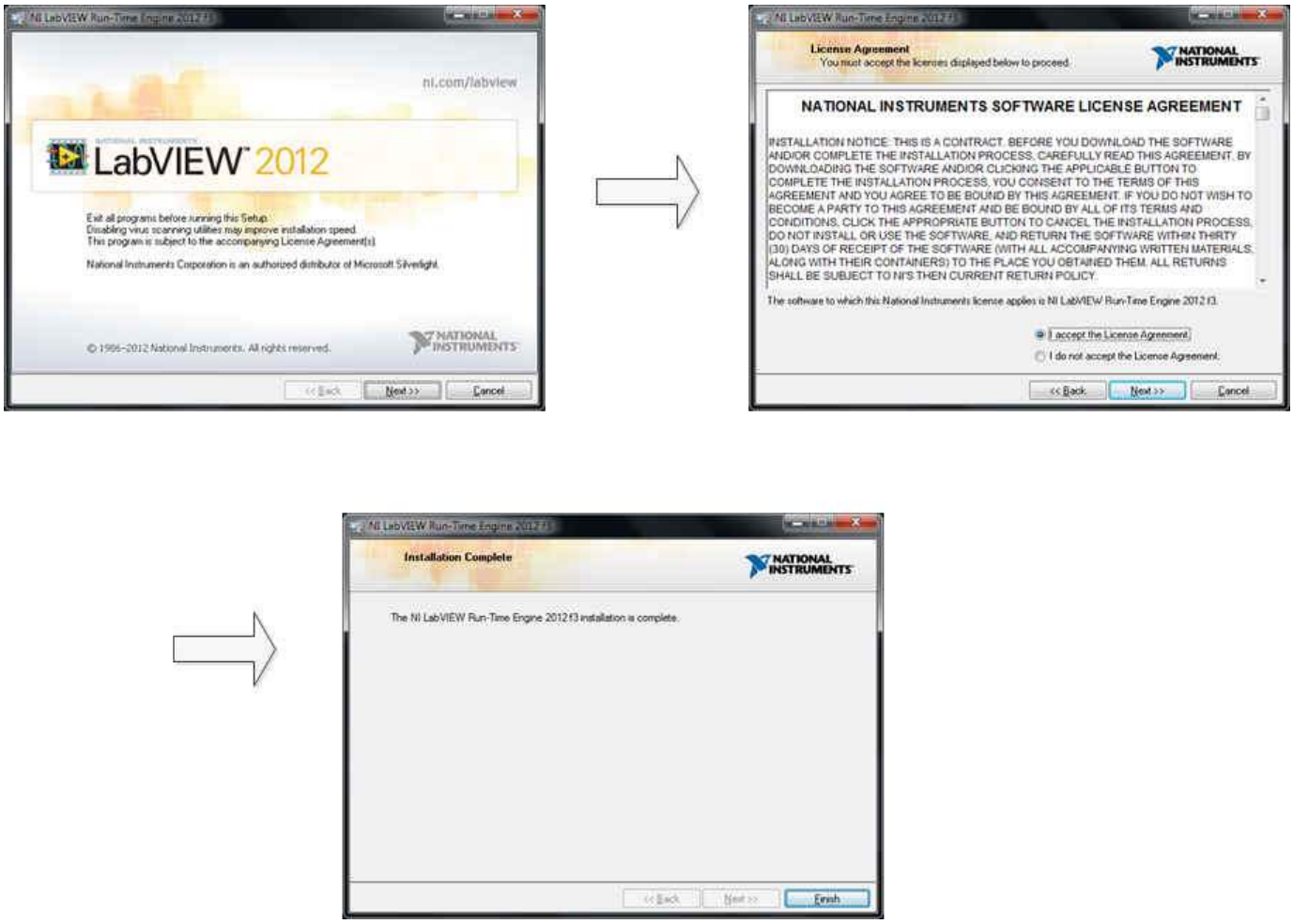

Figure 5-4. LabVIEW Run-Time Engine Installation

After these installations, verify that *C:\Program Files (x86)\Texas Instruments\ADS8332EVM* is as shown in Figure 5-5.

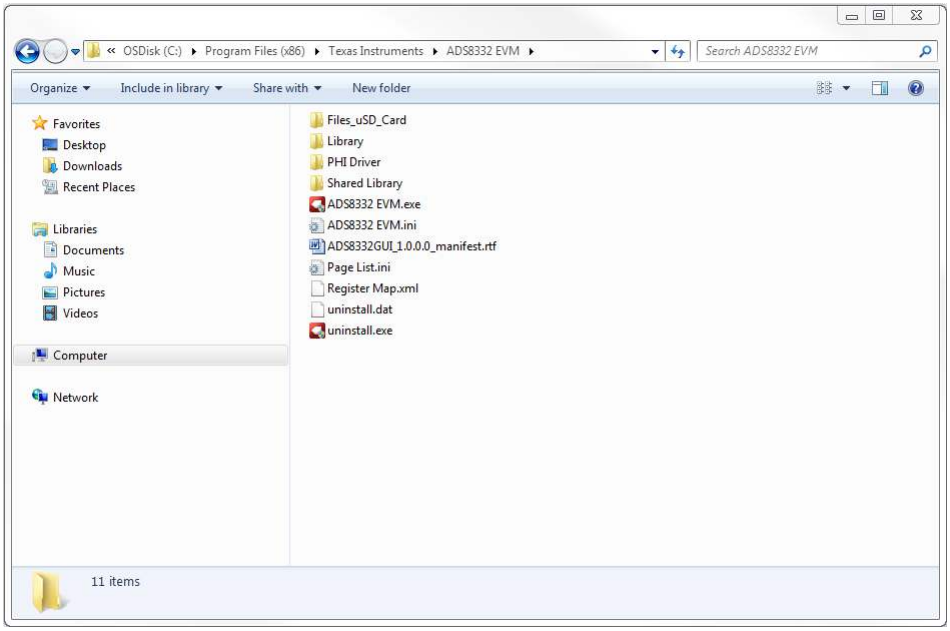

Figure 5-5. ADS8332EVM Folder Post-Installation

6 ADS8332EVMV2-PDK Operation

The following instructions are a step-by-step guide to connecting the ADS8332EVMV2 to the computer and evaluating the performance of the ADS8332:

1. Connect the ADS8332EVMV2 to the PHI. Install the two screws as indicated in Figure 6-1.
2. Use the USB cable provided to connect the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI starts blinking to indicate that the PHI is booted up and communicating with the PC. The resulting LED indicators are shown in Figure 6-1.

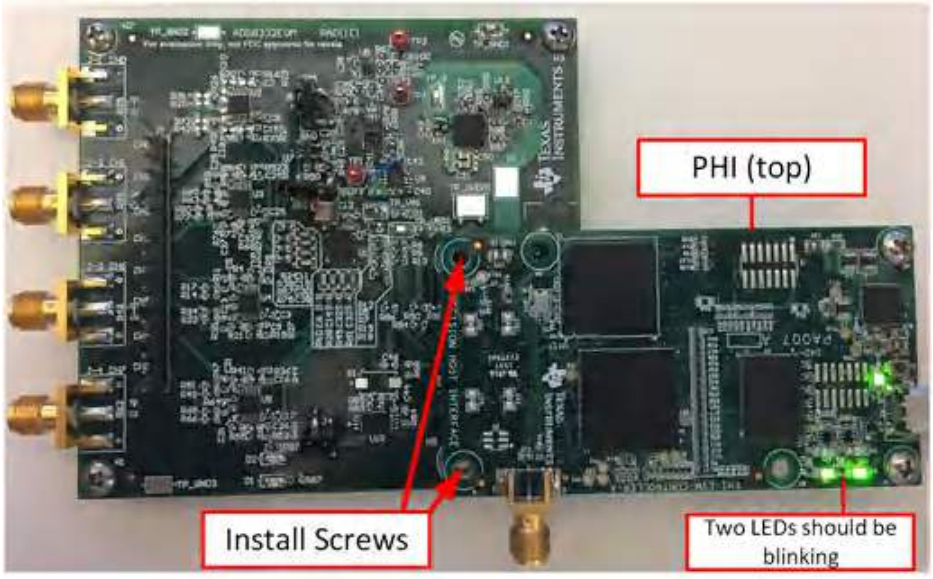

Figure 6-1. ADS8332EVMV2-PDK Hardware Setup and LED Indicators

3. Double click on the ADS8332 EVM.exe file to launch the EVM GUI, as shown in Figure 6-2.

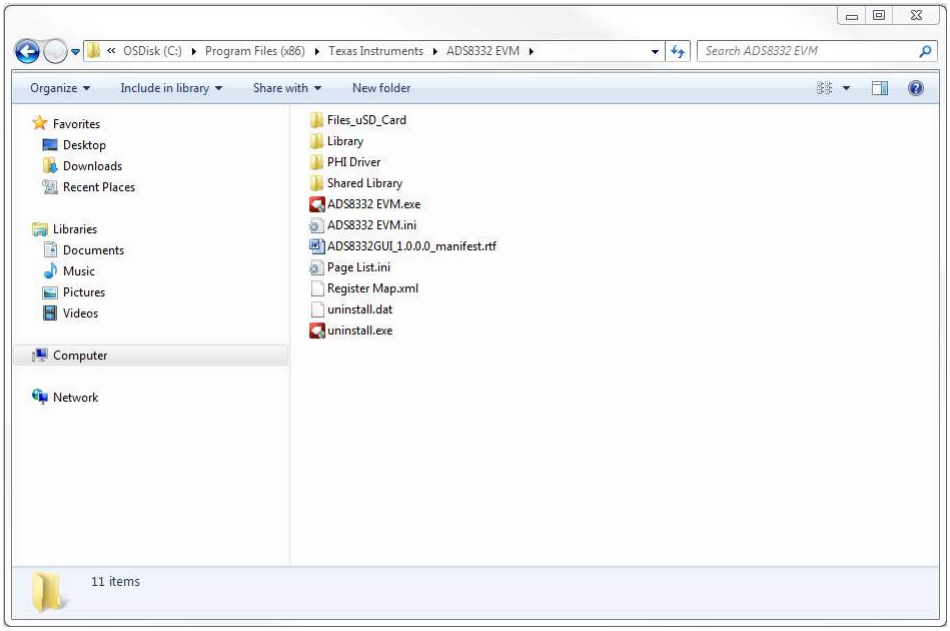

Figure 6-2. Launch the ADS8332EVMV2 GUI Software

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the voltage levels and timing configuration of the ADC digital interface, the EVM GUI provides users with high-level control over the ADS8332 sampling rate, channel selection, and channel scanning.

Figure 6-3 shows the interface configuration pane at the left, through which various functions of the ADS8332 are exercised. These are global settings, and persist across the different GUI testing tools, and the GUI pages listed in the top left pane.

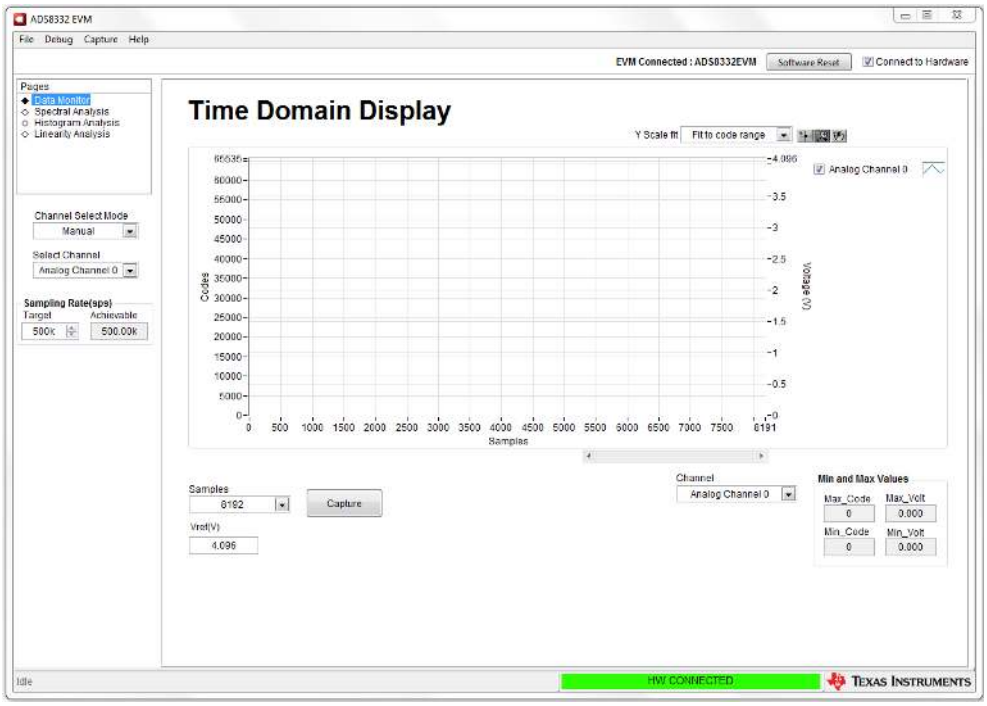

Figure 6-3. EVM GUI Global Input Parameters

The *Channel Select Mode* field allows the user to choose to capture data from a single channel or to automatically scan through the channels.

The *Select Channel* drop-down menu allows the user to select the single channel to sample (if in manual channel select mode) or to select the start channel for the automatic scanning (if in auto channel select mode).

The ADS8332EVMV2 device supports sampling rates from 500 kSPS down to 20 kSPS. The *Sampling Rate* field allows the user to type in the desired sampling rate in samples per second (SPS).

6.2 Time Domain Display Tool

The time domain display tool allows visualization of the time domain conversion results given a set of analog input signals.

The GUI *Time Domain Display* shows the time domain voltage plot for a single channel or for multiple channels if in auto channel select mode. The sample indices are on the x-axis and there are two y-axes showing the codes and the corresponding converted analog voltages. The user can choose to select any combination of desired channels using the *Analog Channel X* selection buttons at the top right side of the display.

The software captures a contingent number of samples as selected in the *Samples* field when the user presses the *Capture* button as shown in Figure 6-4. In addition, the bottom right side of the GUI provides information about the converted signals such as the selected channel maximum and minimum code and maximum and minimum voltage for each channel using the channel drop down in the bottom right. Figure 6-5 shows the time domain display when all eight channels are captured in auto channel select mode.

Figure 6-4. Time Domain Display: Manual

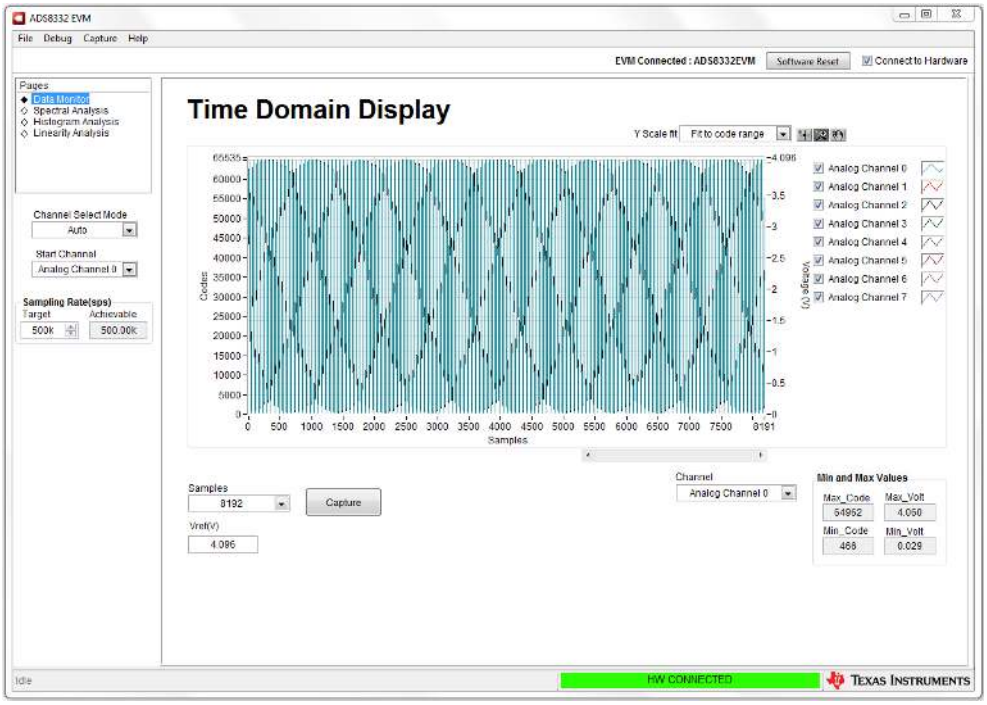

Figure 6-5. Time Domain Display: Auto

6.3 Spectral Analysis Tool

The spectral analysis tool, shown in Figure 6-6, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of ADS8332 SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting.

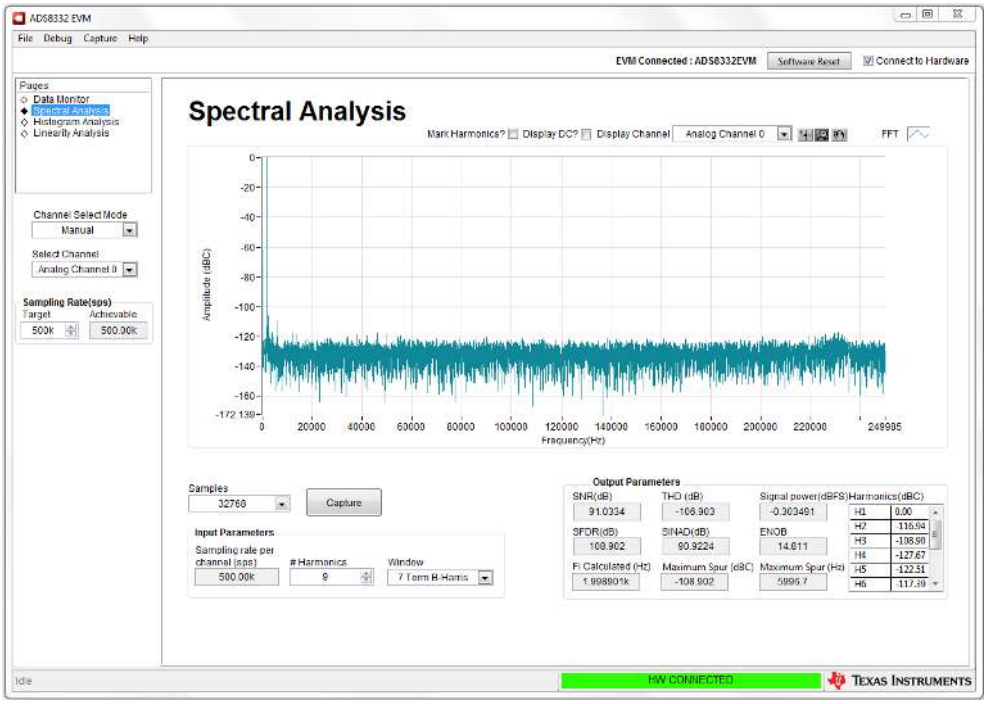

Figure 6-6. Spectral Analysis Tool

For dynamic performance evaluation, the external single-ended source must have better specifications than the ADS8332 to make sure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 6-1.

Table 6-1. External Source Requirements for Evaluation of the ADS8332

Specification Description	Specification Value
Signal frequency	2 kHz (OSR=0)
External source type	Single-ended
External source common-mode	2.048 V
Maximum SNR	100 dB
Maximum THD	–110 dB

For 2-kHz SNR and ENOB evaluation at a maximum throughput of 500 kSPS, the optimal number of samples is 32768. More samples brings the noise floor so low that the external source phase noise can dominate the SNR and ENOB calculations.

Finally, the FFT tool includes windowing options that are required to mitigate the effects of noncoherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

6.4 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking on the *Capture* button, as shown in Figure 6-7:

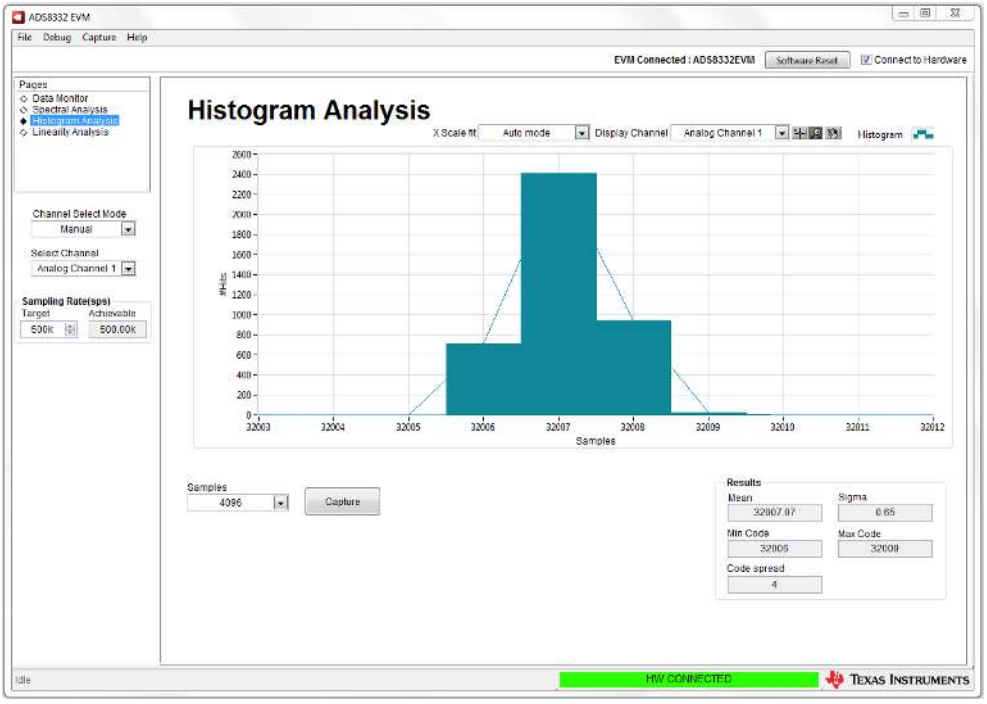

Figure 6-7. Histogram Analysis Tool

6.5 Linearity Analysis Tool

The linearity analysis tool, shown in Figure 6-8, measures and generates the performance differential nonlinearity (DNL) and integral nonlinearity (INL) plots over the entire code range for the ADS8332. A 1-kHz sinusoidal input signal is required, which is slightly saturated (100 mV to 200 mV outside the full-scale range) at the input with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. Jumper JP1 *must* be put into position with the shunt on pins 1-2 to allow for a common voltage of 0.2 V to be applied, thus allowing the inputs to be fully saturated. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Table 6-2.

Table 6-2. External Source Requirements for ADS8332 Evaluation

Specification Description	Specification Value
Signal frequency	1 kHz
External source type	Single ended, referred to GND
External source common mode	2.25-V
Signal amplitude	4.2-V_{PP}
Maximum noise	35 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–110 dB

The number-of-hits setting depends on the external noise source. For a 100-dB SNR external source with approximately 30 µVrms of noise, the total number of hits must be 256.

Note

This analysis can take a couple of minutes to run and the evaluation board must remain undisturbed during the complete duration of the analysis.

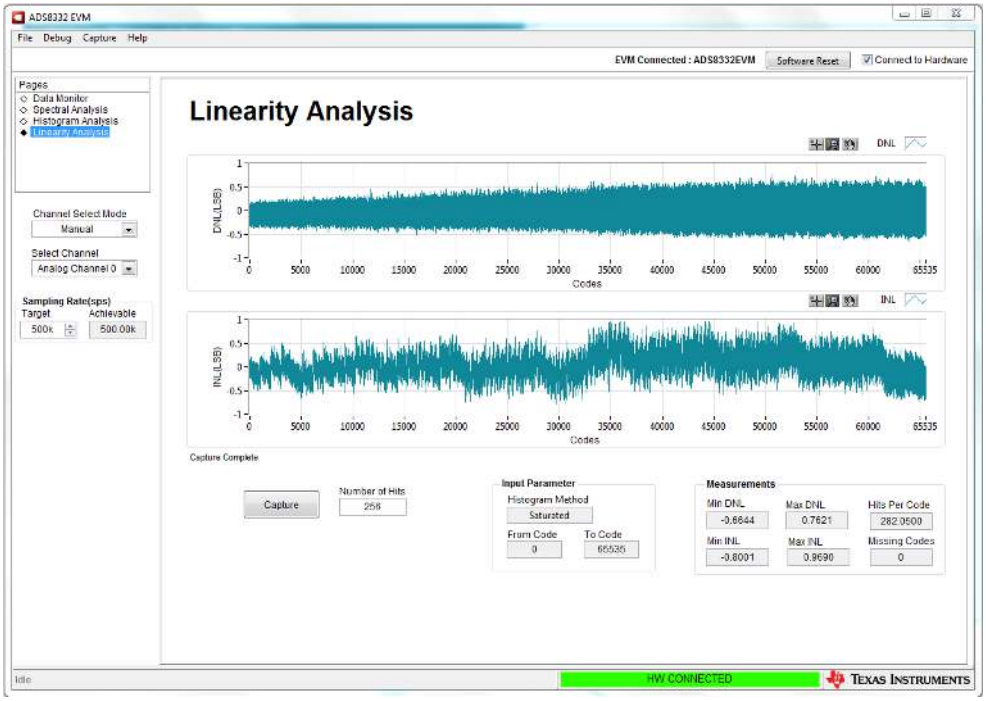

Figure 6-8. Linearity Analysis Tool

6.6 Input Amplifier Configurations

The ADS8332EVMV2 is designed so the user can configure the input amplifier in many different topologies. The EVM comes with the input as a unity gain buffer because this is applicable to the majority of SAR ADC designs. All eight of the input amplifiers have unpopulated components that allow for configurability.

Figure 6-9 shows three different input amplifier options for the ADS8332EVMV2. First, is the buffer configuration and this is how the EVM will initially be populated. Next, is an inverting configuration for when the dc offset of the input signal is zero. This topology will superimpose the input signal onto the voltage REF/2. Lastly, the bottom inverting configuration should be used for an input signal with the dc offset of VREF/2. This amplifier will maintain the dc offset of VREF/2.

The input amplifiers can be adjusted in many different ways to produce gains, filters, and a number of other functions. These input configurations are not tested and may require a higher bandwidth amplifier than what is populated on the ADS8332EVMV2.

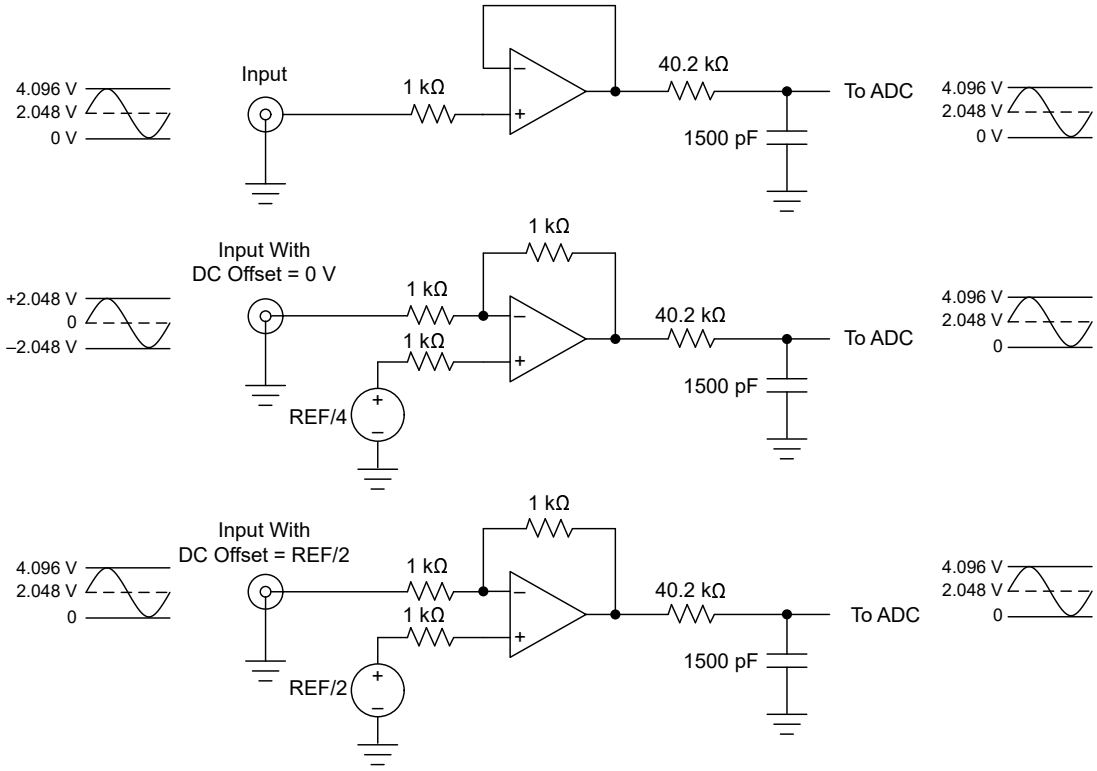

Figure 6-9. Input Amplifier Configuration Examples

7 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS8332EVMV2 bill of materials, PCB layout, and the EVM schematics.

7.1 Bill of Materials

Table 7-1 lists ADS8332 EVM BOM. Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts can be substituted with equivalents.

Table 7-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
PCB1	1		Printed Circuit Board		PA011	Any
C1, C4, C28, C36, C52	5	1uF	CAP, CERM, 1 µF, 10 V, + /- 10%, X7 S, 0402	0402	C1005X7 S1A105K050BC	TDK
C3, C8, C18, C21, C26	5	0.1uF	CAP, CERM, 0.1 µF, 50 V, + /- 10%, X7R, 0402	0402	C1005X7R1 H104K050BB	TDK
C6, C11, C14, C15, C20, C23, C31, C33, C39	9	1500 pF	CAP, CERM, 1500 pF, 50 V, + /- 5%, C0 G/NP0, 0603	0603	GRM1885C1 H152 JA01 J	MuRata
C12	1	47uF	CAP, CERM, 47 µF, 10 V, + /- 20%, X7R, 1210	1210	LMK325B7476MM-TR	Taiyo Yuden
C24	1	1000 pF	CAP, CERM, 1000 pF, 50 V, + /- 5%, C0 G/NP0, 0603	0603	C0603C102 J5 GAC	Kemet
C29, C35, C37	3	0.1uF	CAP, CERM, 0.1 µF, 50 V, + /- 10%, X7R, 0402	0402	C1005X7R1 H104K050BB	TDK
C41, C43, C45, C48, C49	5	10uF	CAP, CERM, 10 µF, 16 V, + /- 20%, X5R, 0603	0603	EMK107BBJ106MA-T	Taiyo Yuden
C42	1	1uF	CAP, CERM, 1 µF, 10 V, + /- 10%, X7R, 0603	0603	885012206026	Wurth Elektronik
C44, C47	2	0.1uF	CAP, CERM, 0.1 µF, 50 V, + /- 10%, X7R, 0402	0402	C1005X7R1 H104K	TDK
C50, C51	2	22uF	CAP, CERM, 22 µF, 10 V, + /- 20%, X5R, 0603	0603	C1608X5R1A226M080AC	TDK
D1, D2	2	Green	LED, Green, SMD	LED_0805	APT2012 LZGCK	Kingbright
H1, H2, H3, H4	4		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4"	PMSSS 440 0025 PH	B&F Fastener Supply
H5, H6	2		ROUND STANDOFF, M3 STEEL 5MM		9774050360R	WURTH ELECTRONICS INC
H7, H8	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H9, H10, H11, H12	4		3/16 Hex Female Standoff	3/16 Hex Female Standoff	1891	Keystone
H13	1		PHI-EVM Controller	USB Cable	Edge# 6591636 rev. B	Texas Instruments
J1	1		Header, 100 mil, 16x1, Gold, TH	16x1 Header	68000-416 HLF	Amphenol FCI
J2	1		Header(Shrouded), 19.7 mil, 30x2, Gold, SMT	Header (Shrouded), 19.7 mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J4	1		Header, 100 mil, 2x1, Gold with Tin Tail, SMT	2x1 Header	TSM-102-01-L-SV	Samtec
J5, J6, J7, J8	4		Connector, End launch SMA, 50 ohm, SMT	End Launch SMA	142-0701-801	Johnson
JP1, JP2	2		Header, 100 mil, 3x1, Gold, SMT	Samtec_TSM-103-01-X-SV	TSM-103-01-L-SV	Samtec
R1, R2, R10, R17, R20, R24, R25, R27, R30, R37, R40, R42, R44, R50, R52, R56, R58, R59, R63, R65, R68, R70, R75, R77, R83, R87, R99, R101, R105, R106, R107	31	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2 GE0R00X	Panasonic
R3, R97	2	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R5, R6, R7, R9, R13, R14, R16	7	47	RES, 47, 5%, 0.063 W, 0402	0402	CRCW040247R0 JNED	Vishay-Dale

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R11, R26, R31, R34, R43, R51, R64, R69, R84	9	40.2	RES, 40.2, 1%, 0.063 W, 0402	0402	CRCW040240R2FKED	Vishay-Dale
R12, R28, R33, R45, R53, R66, R72, R78, R85, R91	10	1.00k	RES, 1.00 k, 0.1%, 0.063 W, 0402	0402	ERA-2AEB102X	Panasonic
R19	1	100k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R55	1	30.1	RES, 30.1, 1%, 0.063 W, 0402	0402	CRCW040230R1FKED	Vishay-Dale
R79, R89	2	20.0k	RES, 20.0 k, 0.1%, 0.0625 W, 0402	0402	RT0402BRD0720KL	Yageo America
R82, R88	2	10.0k	RES, 10.0 k, 0.1%, 0.0625 W, 0402	0402	RT0402BRD0710KL	Yageo America
R92, R93, R94, R98, R102, R103, R104	7	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0 JNED	Vishay-Dale
R95, R100	2	20k	RES, 20 k, 5%, 0.063 W, 0402	0402	CRCW040220K0 JNED	Vishay-Dale
SH-J1, SH-J2	2		Shunt, 100 mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity
TP1, TP10	2	SMT	Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
TP2, TP4, TP5, TP6, TP7, TP11, TP12	7	SMT	Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
TP8	1		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1		2.7 V-5.5 V, 16 Bit 500KSPS Low-power Serial ADC, 8-Ch MUX and Breakout, RGE0024F (VQFN-24)	RGE0024F	ADS8332IBRGER	Texas Instruments
U2, U3, U4, U5, U6	5		Precision, 20 MHz, 0.9 pA, Low-Noise, RRIO, CMOS Operational Amplifier with Shutdown, DGS0010A	DGS0010A	OPA2320 SAIDGSR	Texas Instruments
U7	1		Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS and no Sb/Br)	DBV0005A	OPA320AIDBVT	Texas Instruments
U8	1		Precision, Low Noise, Low Iq Operational Amplifier, 2.2 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DCK0005A), Green (RoHS and no Sb/Br)	DCK0005A	OPA376AIDCKT	Texas Instruments
U9	1		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6041IDGKR	Texas Instruments
U10	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24 G32FVT-3AGE2	Rohm
U11	1		36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U12	1		Nanopower Supervisory Circuits for Automotive, DBV0005A (SOT-23-5)	DBV0005A	TPS3836E18DBVT	Texas Instruments

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C2, C5, C7, C9, C10, C13, C16, C17, C19, C22, C25, C27, C30, C32, C34, C38, C46	0	1uF	CAP, CERM, 1 µF, 10 V, + /- 10%, X7 S, 0402	0402	C1005X7 S1A105K050BC	TDK
C40	0	1500 pF	CAP, CERM, 1500 pF, 50 V, + /- 5%, C0 G/NP0, 0603	0603	GRM1885C1 H152 JA01 J	MuRata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J3	0		Receptacle, VHDCI, 68Pin, Gold, R/A, TH	Connector, 42.7x6x14.65 mm	71430-0013	Molex
R4, R8, R15, R18, R21, R22, R23, R29, R32, R35, R36, R38, R39, R41, R46, R47, R48, R49, R54, R57, R60, R61, R62, R67, R71, R73, R74, R76, R80, R81, R86, R90	0	1.00k	RES, 1.00 k, 0.1%, 0.063 W, 0402	0402	ERA-2AEB102X	Panasonic
R96	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2 GE0R00X	Panasonic
S1	0		Switch, Tactile, SPST-NO, 0.05A, 12 V, SMD	SMD, 2-Leads, Body 6x4 mm	EVQPNF04M	Panasonic
TP3, TP9	0		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone

7.2 PCB Layout

Figure 7-1 through Figure 7-6 illustrate the EVM PCB layout.

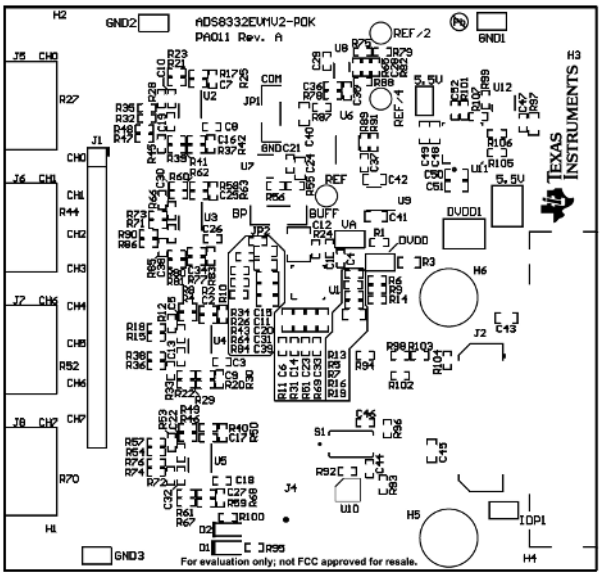

Figure 7-1. ADS8332EVMV2 PCB: Top Overlay

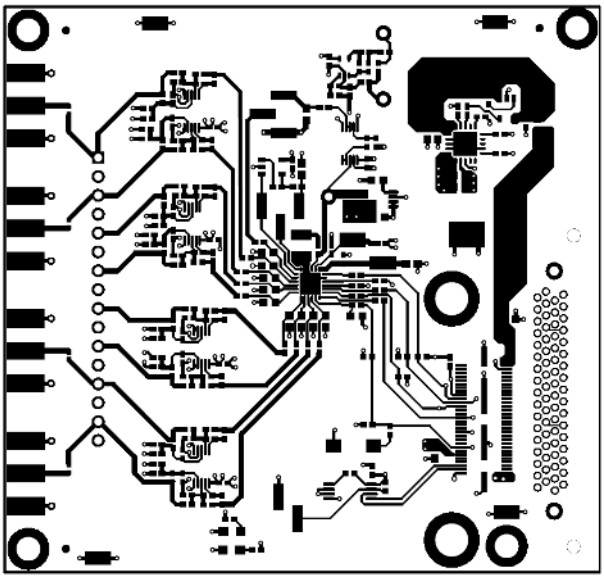

Figure 7-2. ADS8332EVMV2 PCB Layer 1: Top Layer

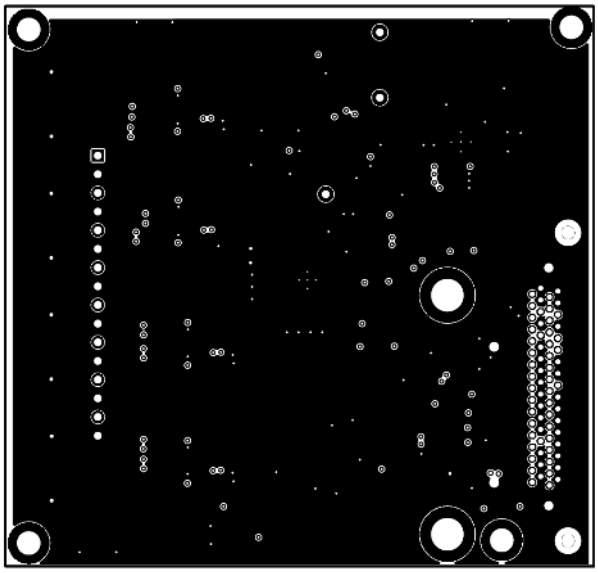

Figure 7-3. ADS8332EVMV2 PCB Layer 2: GND Plane

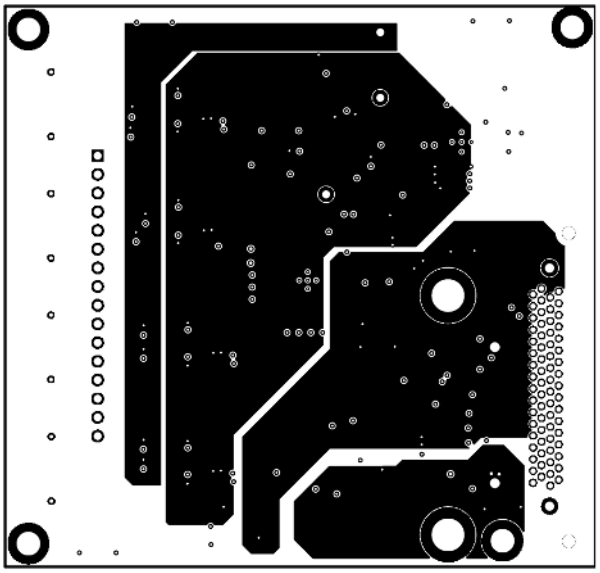

Figure 7-4. ADS8332EVMV2 PCB Layer 3: Power Planes

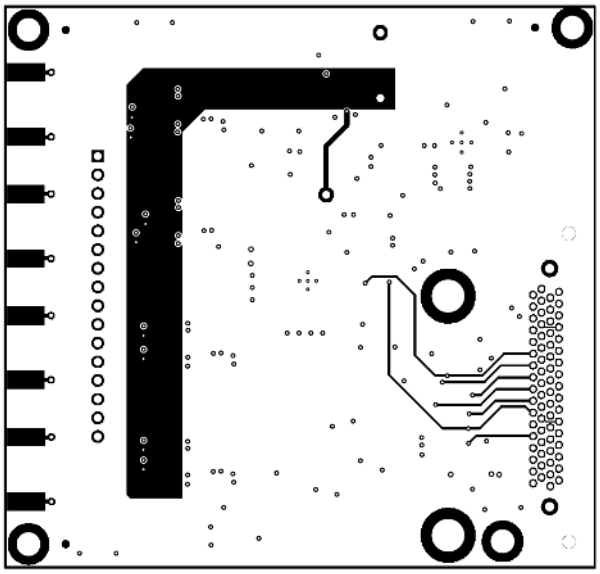

Figure 7-5. ADS8332EVMV2 PCB Layer 4: Bottom Layer

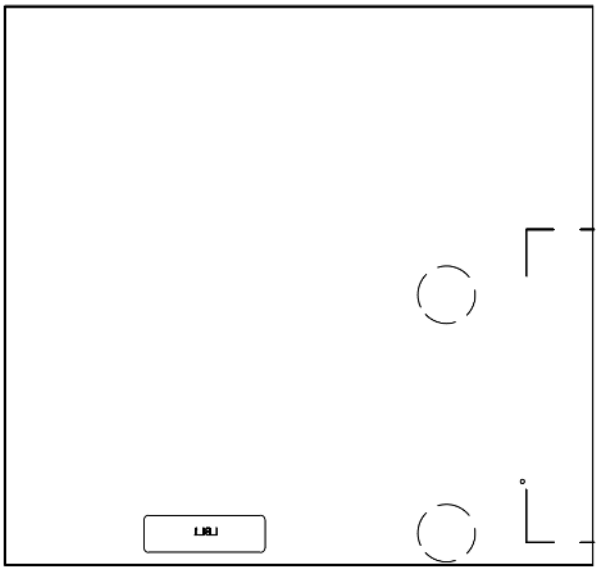

Figure 7-6. ADS8332EVMV2 PCB: Bottom Overlay

7.3 Schematics

Figure 7-7 through Figure 7-9 illustrate the EVM schematics.

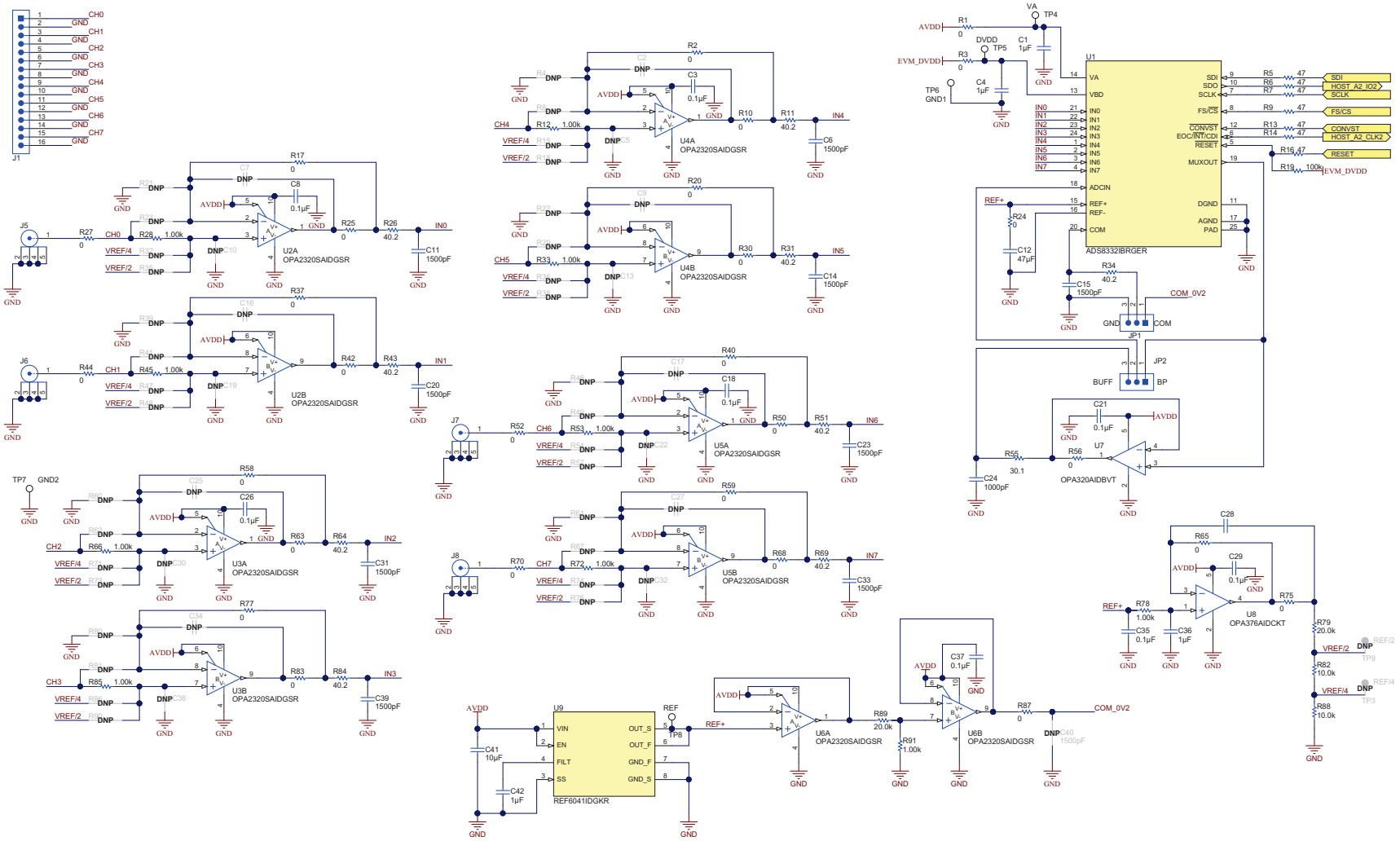

Figure 7-7. ADS8332EVMV2-PDK Schematic: ADC

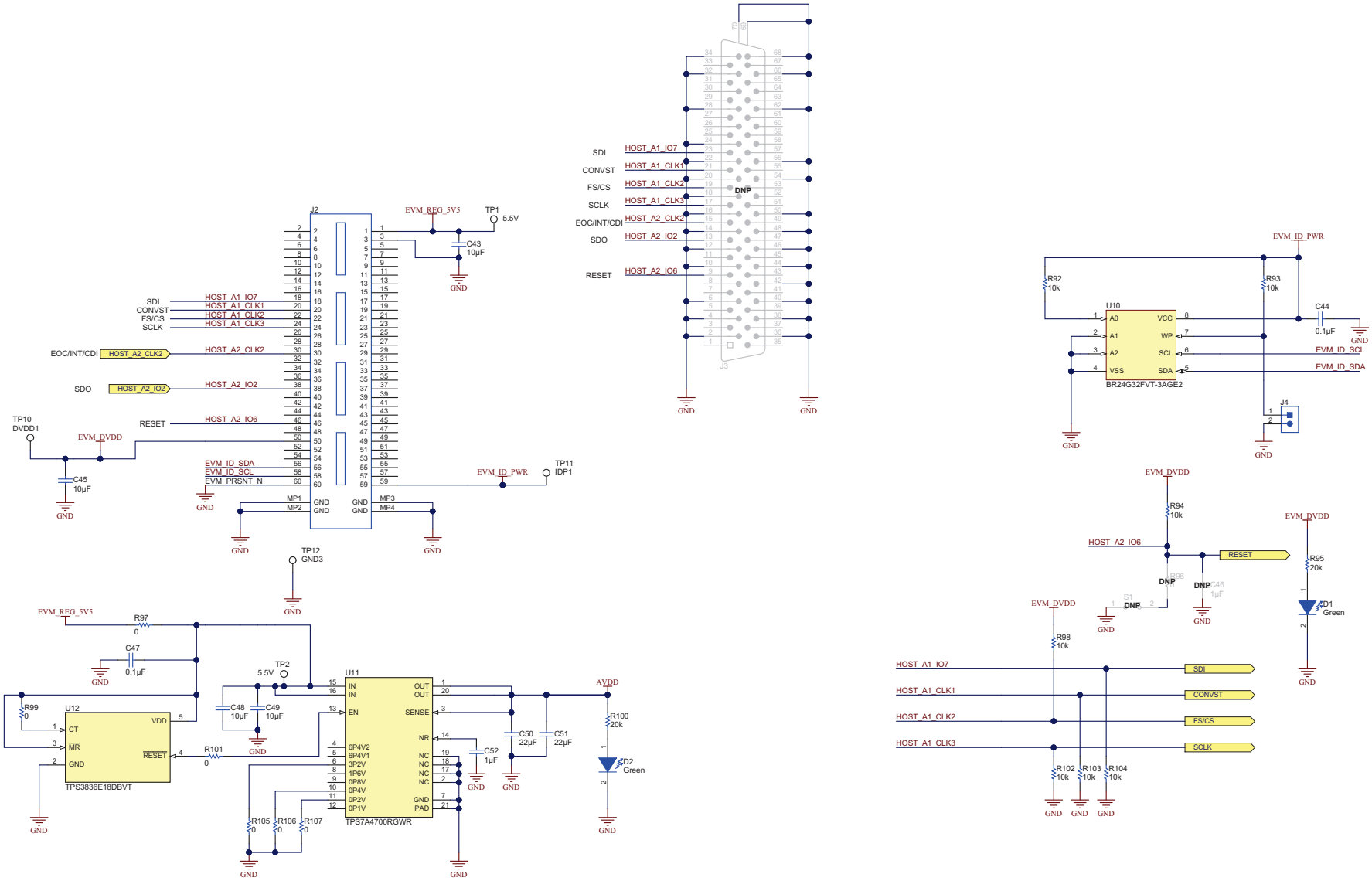

Figure 7-8. ADS8332EVMV2-PDK Schematic: Interface

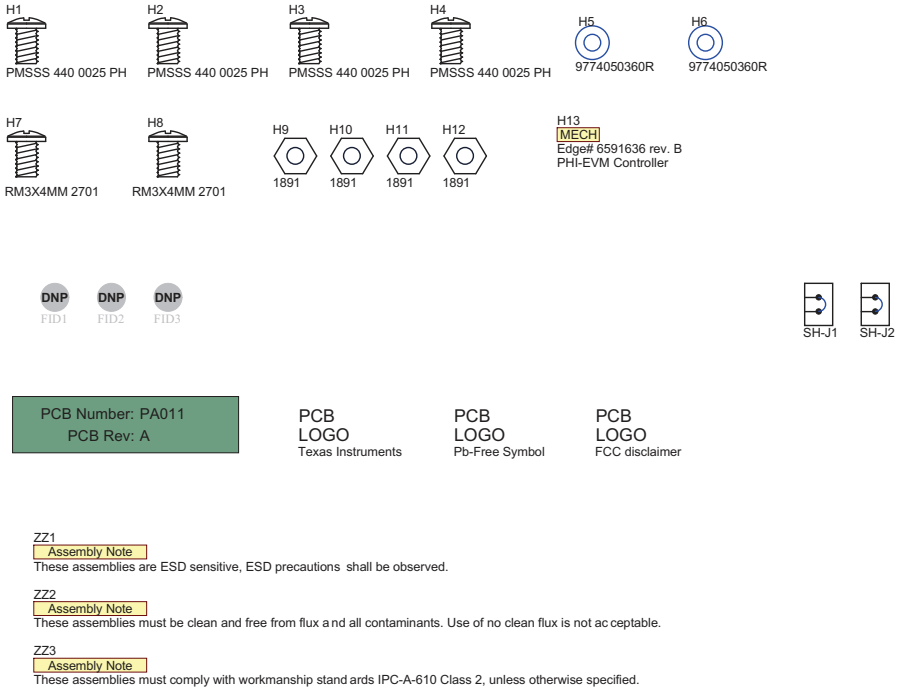

Figure 7-9. ADS8332EVMV2-PDK Schematic: Hardware

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2017) to Revision B (February 2023)	Page
• Changed *Input Amplifier Configuration Examples* figure	20

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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