# 700MHZ, LOW JITTER, CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

**ICS84329B-01**

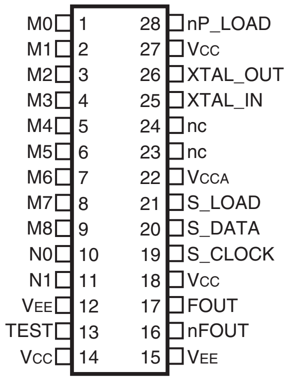
## General Description

The ICS84329B-01 is a general purpose, single output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the crystal frequency divided by 16. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The output can be configured to divide the VCO frequency by 1, 2, 4, and 8. Output frequency steps as small as 125kHz to 1MHz can be achieved using a 16MHz crystal depending on the output dividers.

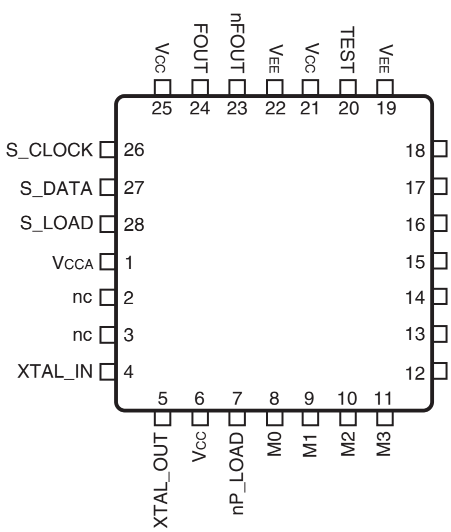
## Features

- Fully integrated PLL, no external loop filter requirements
- One differential 3.3V LVPECL output pair
- Crystal oscillator interface
- Output frequency range: 31.25MHz – 700MHz
- VCO range: 250MHz – 700MHz
- Parallel interface for programming counter and output dividers during power-up
- Serial 3 wire interface
- RMS period jitter: 5.5ps (maximum)
- Cycle-to-cycle jitter: 35ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Pin Assignments

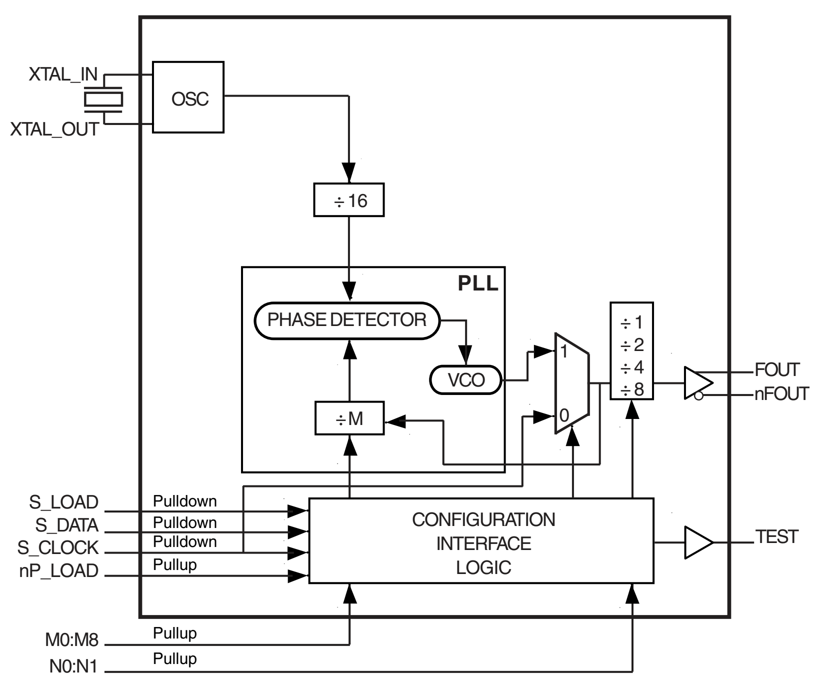



**ICS84329B-01**
**28 Lead SOIC**
**7.5mm x 18.05mm x 2.25mm package body**
**M Package**
**Top View**




**ICS84329B-01**
**28 Lead PLCC**
**11.6mm x 11.4mm x 4.1mm package body**
**V Package**
**Top View**

## Block Diagram



## Functional Description

*NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6, NOTE 1.*

The ICS84329B-01 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A parallel resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency ÷ 16 by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS84329B-01 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. The TEST output is Mode 000 (shift register out) when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fXTAL}{16} \times M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as $250 \le M \le 511$. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fXTAL}{16} \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T2:T0. The internal resistors T2:T0 determine the state of the TEST output as follows:

| T2 | T1 | T0 | TEST Output | fOUT |
|---|---|---|---|---|
| 0 | 0 | 0 | Shift Register Out | fOUT |
| 0 | 0 | 1 | HIGH | fOUT |
| 0 | 1 | 0 | PLL Reference XTAL ÷16 | fOUT |
| 0 | 1 | 1 | (VCO ÷ M) /2 (non 50% Duty Cycle M Divider) | fOUT |
| 1 | 0 | 0 | fOUT, LVCMOS Output Frequency < 200MHz | fOUT |
| 1 | 0 | 1 | LOW | fOUT |
| 1 | 1 | 0 | S_CLOCK ÷ M (non 50% Duty Cycle M Divider) | S_CLOCK ÷ N Divider |
| 1 | 1 | 1 | fOUT ÷ 4 | fOUT |

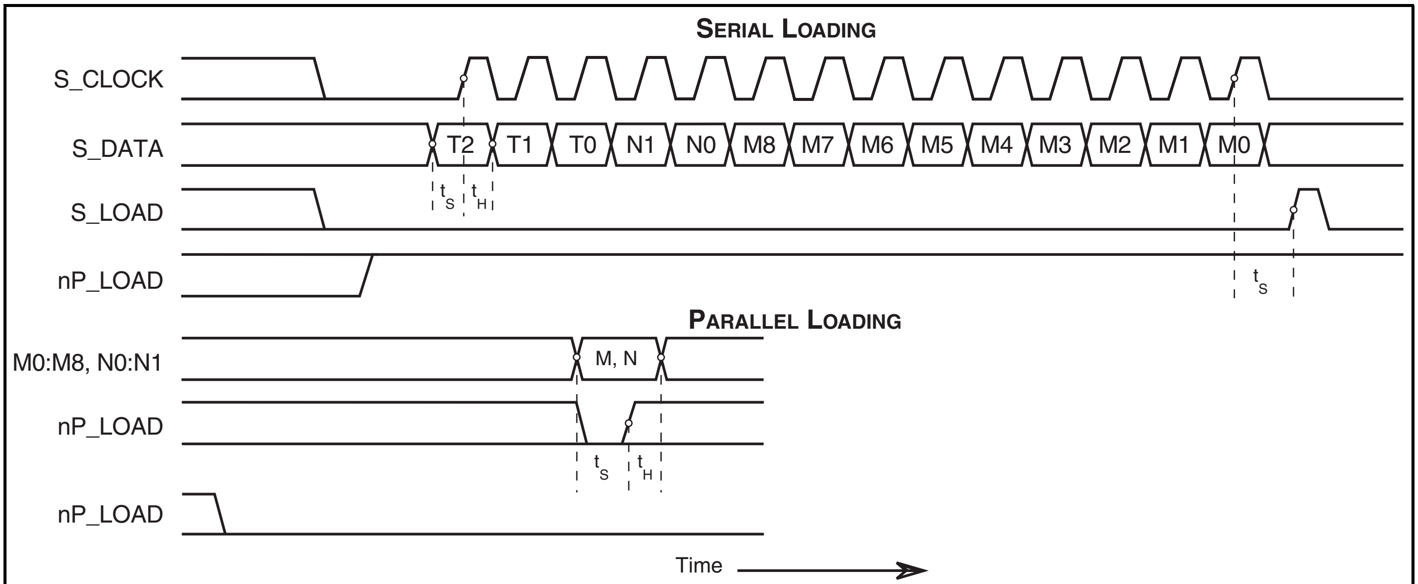



**Figure 1. Parallel & Serial Load Operations**

# Table 1. Pin Descriptions

| Name | Type | | Description |
|---|---|---|---|
| M0, M1, M2, M3, M4, M5, M6, M7, M8 | Input | Pullup | M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels. |
| N0, N1 | Input | Pullup | Determines N output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels. |
| $V_{EE}$ | Power | | Negative supply pins. |
| TEST | Output | | Test output which is used in the serial mode of operation. Single-ended LVPECL interface levels. |
| $V_{CC}$ | Power | | Core supply pins. |
| FOUT, nFOUT | Output | | Differential output pair for the synthesizer. LVPECL interface levels. |
| nc | Unused | | No connect. |
| S_CLOCK | Input | Pulldown | Clocks the serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels. |
| S_DATA | Input | Pulldown | Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels. |
| S_LOAD | Input | Pulldown | Controls transition of data from shift register into the M divider. LVCMOS/LVTTL interface levels. |
| $V_{CCA}$ | Power | | Analog supply pin. |
| XTAL_IN<br>XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| nP_LOAD | Input | Pullup | Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

# Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Tables

### Table 3A. Parallel and Serial Mode Function Table

| Inputs | | | | | | Conditions |
|---|---|---|---|---|---|---|
| nP_LOAD | M | N | S_LOAD | S_CLOCK | S_DATA | |
| X | X | X | X | X | X | Reset. M and N bits are all set HIGH. |
| L | Data | Data | X | X | X | Data on M and N inputs passed directly to the M divider and N output divider. TEST mode 000. |
| ↑ | Data | Data | L | X | X | Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs. |
| H | X | X | L | ↑ | Data | Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK. |
| H | X | X | ↑ | L | Data | Contents of the shift register are passed to the M divider and N output divider. |
| H | X | X | ↓ | L | Data | M divider and N output divider values are latched. |
| H | X | X | L | X | X | Parallel or serial input do not affect shift registers. |

NOTE:L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

### Table 3B. Programmable VCO Frequency Function Table

| VCO Frequency (MHz) | M Divide | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 250 | 250 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 251 | 251 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 252 | 252 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 253 | 253 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • |
| 509 | 509 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 510 | 510 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 511 | 511 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTE 1: These M divide values and the resulting frequencies correspond to a crystal frequency of 16MHz.

### Table 3C. Programmable Output DividerFunction Table

| Inputs | | N Divider Value | Output Frequency (MHz) | |
|---|---|---|---|---|
| N1 | N0 | | Minimum | Maximum |
| 0 | 0 | 1 | 250 | 700 |
| 0 | 1 | 2 | 125 | 350 |
| 1 | 0 | 4 | 62.5 | 175 |
| 1 | 1 | 8 | 31.25 | 87.5 |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$+ 0.5V |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$<br>28 Lead SOIC<br>28 Lead PLCC | <br>46.2°C/W (0 lfpm)<br>37.8°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = 3.3V±5%, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{CC}$ | Power Supply Current | | | | 125 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 15 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC}$ = 3.3V±5%, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | S_CLOCK, S_DATA, S_LOAD | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | nP_LOAD, M0:M8, N0, N1 | $V_{CC} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | S_CLOCK, S_DATA, S_LOAD | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nP_LOAD, M0:M8, N0, N1 | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage | TEST; NOTE 1 | $V_{CC}$ = 3.3V±5% | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage | TEST; NOTE 1 | $V_{CC}$ = 3.3V±5% | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$/2. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

**Table 4C. LVPECL DC Characteristics,** $V_{CC}$ = 3.3V±5%, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Current; NOTE 1 | | $V_{CC}$ – 1.4 | | $V_{CC}$ – 0.9 | µA |
| $V_{OL}$ | Output Low Current; NOTE 1 | | $V_{CC}$– 2.0 | | $V_{CC}$ – 1.7 | µA |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$ – 2V.

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 10 | | 25 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

**Table 6. Input Frequency Characteristics,** $V_{CC}$ = 3.3V±5%, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | XTAL_IN, XTAL_OUT; NOTE 1 | | 10 | | 25 | MHz |
| | | S_CLOCK | | | | 50 | MHz |

NOTE 1: For the crystal frequency range, the M value must be set to achieve the minimum or maximum VCO frequency range of 250MHz to 700MHz range. Using the minimum input frequency of 10MHz, valid values of M are 400 ≤ M ≤ 511. Using the maximum input frequency of 25MHz, valid values of M are 160 ≤ M ≤ 448.

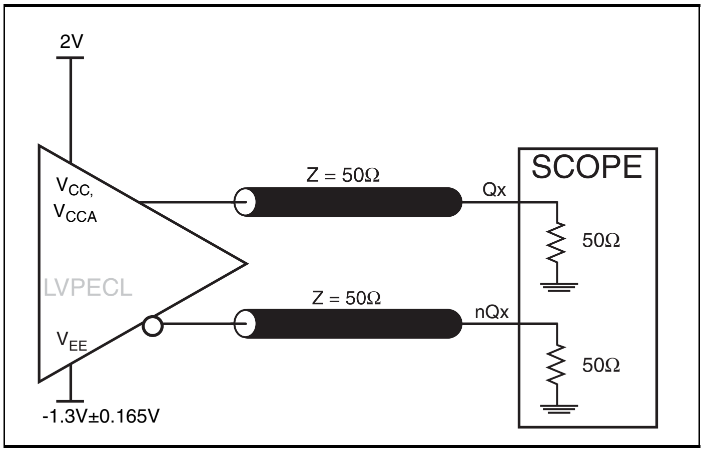
# AC Electrical Characteristics

**Table 7. AC Characteristics,** $VV_{CC}$ = 3.3V±5%, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C

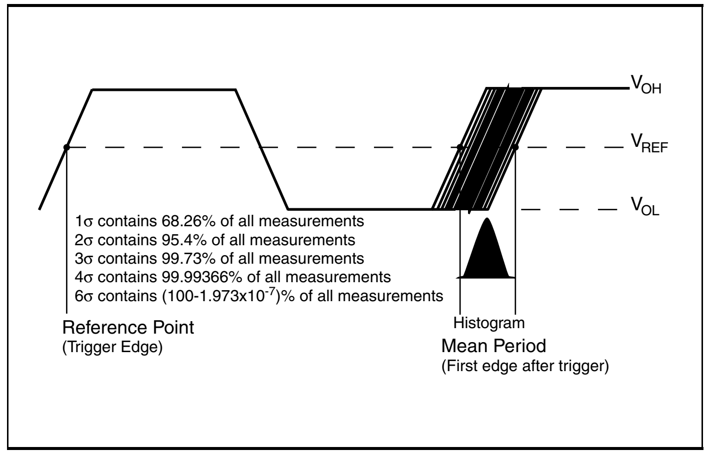
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | | 700 | MHz |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 1, 2 | $f_{OUT}$ ≥ 50MHz | | | 35 | ps |
| | | $f_{OUT}$ < 50MHz | | | 50 | ps |
| *t*jit(per) | Period Jitter, RMS; NOTE 1, 2 | $f_{OUT}$ ≥ 65MHz | | | 5.5 | ps |
| | | $f_{OUT}$ < 65MHz | | | 12 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 800 | ps |
| $t_S$ | Setup Time | | 5 | | | ns |
| $t_H$ | Hold Time | | 5 | | | ns |
| odc | Output Duty Cycle | | 45 | 50 | 55 | % |
| $t_{LOCK}$ | PLL Lock Time | | | | 10 | ms |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
See Parameter Measurement Information section.
Characterized using XTAL inputs.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: See Applications Section.

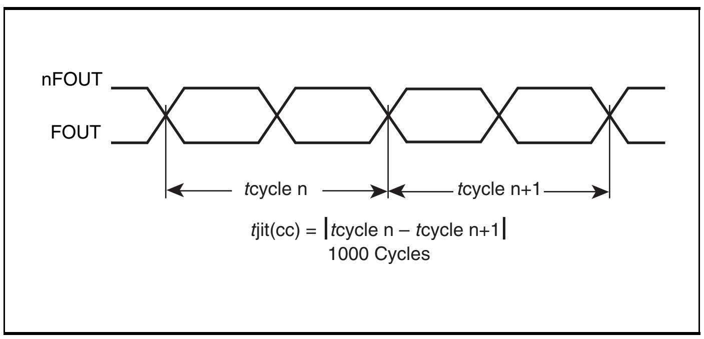
# Parameter Measurement Information



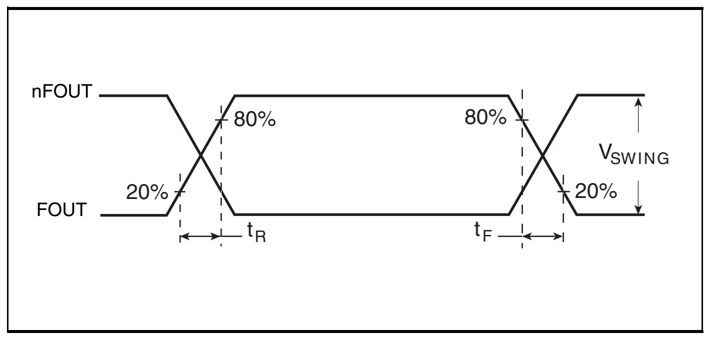

**3.3 LVPECL Output Load AC Test Circuit**



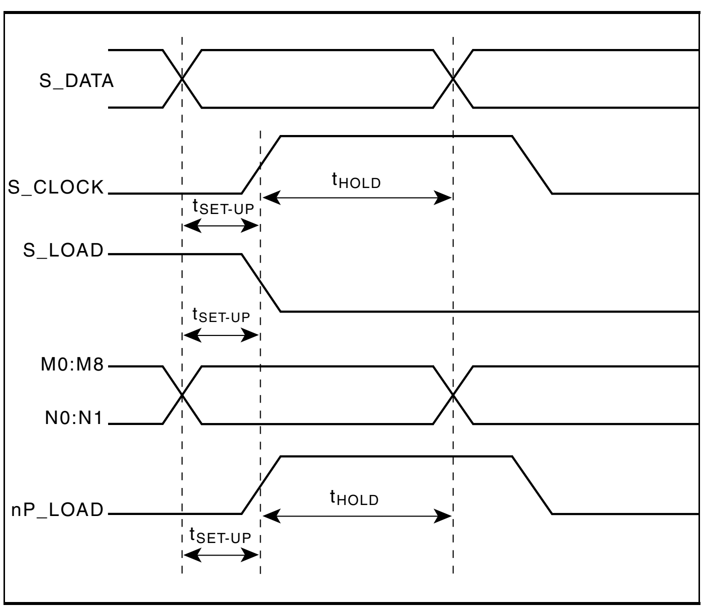

**Period Jitter**



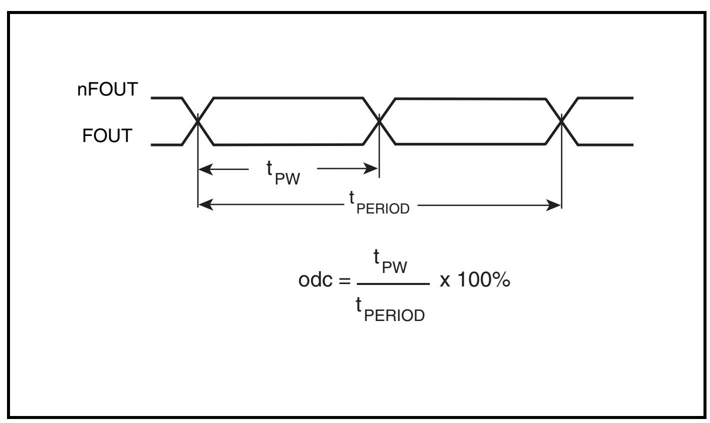

**Cycle-to-Cycle Jitter**




**Output Rise/Fall Time**




**Setup and Hold Time**




**Output Duty Cycle/Pulse Width/Period**

# Application Information

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS84329B-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$ and $V_{CCA}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic $V_{CC}$ pin and also shows that $V_{CCA}$ requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{CCA}$ pin.

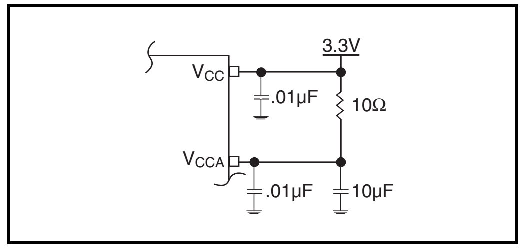



**Figure 2. Power Supply Filtering**

## Recommendations for Unused Input and Output Pins

### Inputs:

**LVCMOS Control Pins**
All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

**TEST Output**
The unused TEST output can be left floating. There should be no trace attached.

**LVPECL Outputs**
The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The ICS84329B-01 has been characterized for either series or parallel mode operation. The ICS84329B-01 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate frequencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in Figure 3.

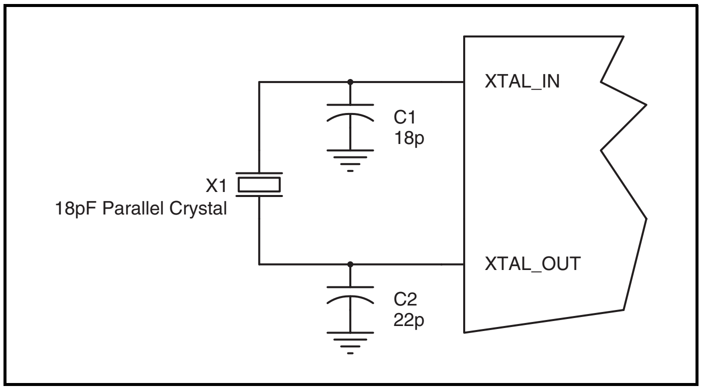



**Figure 3. Crystal Input Interface**

## LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

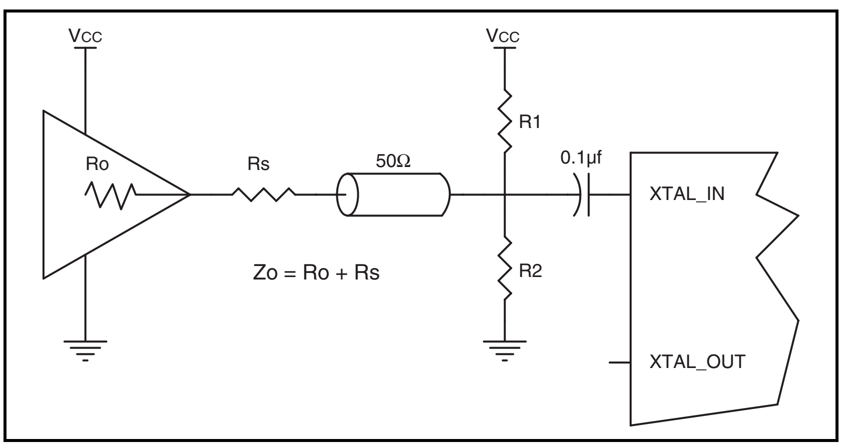



**Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface**

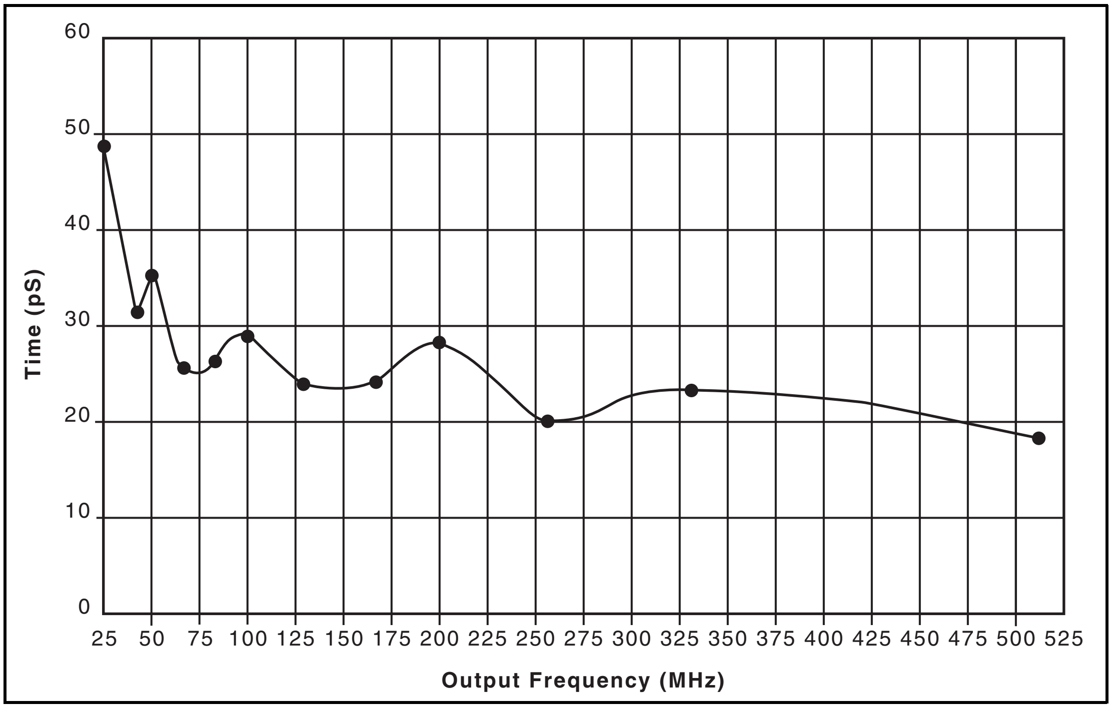



**Figure 5A. Cycle-to-Cycle Jitter vs. fOUT (using a 16MHz crystal)**

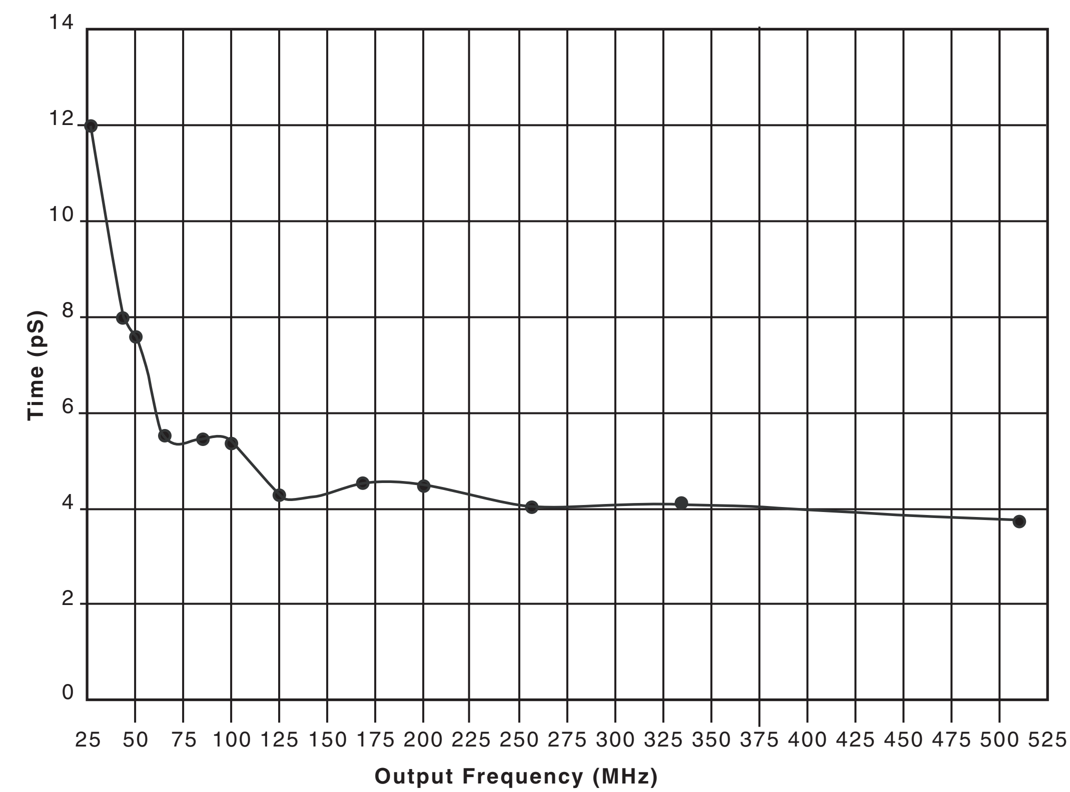



**Figure 5B. RMS Jitter vs. $f_{OUT}$ (using a 16MHz crystal)**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

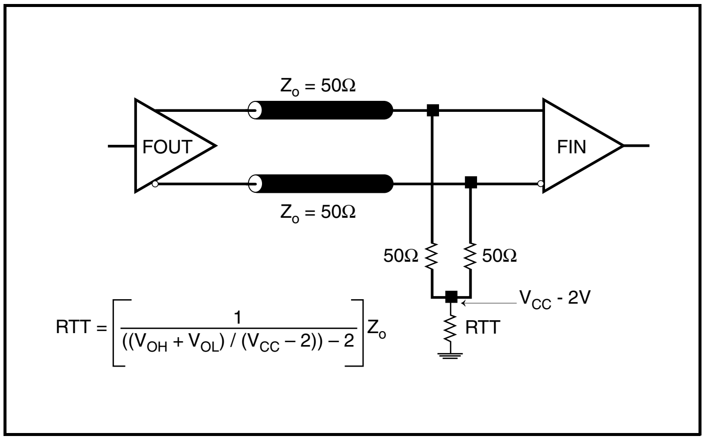



**Figure 6A. 3.3V LVPECL Output Termination**

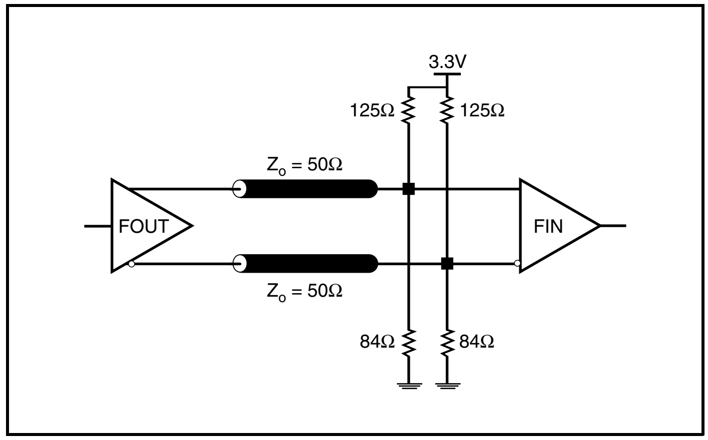



**Figure 6B. 3.3V LVPECL Output Termination**

## Layout Guideline

The schematic of the ICS84329B-01 layout example used in this layout guideline is shown in *Figure 7A.* The ICS84329B-01 recommended PCB board layout for this example is shown in *Figure 7B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

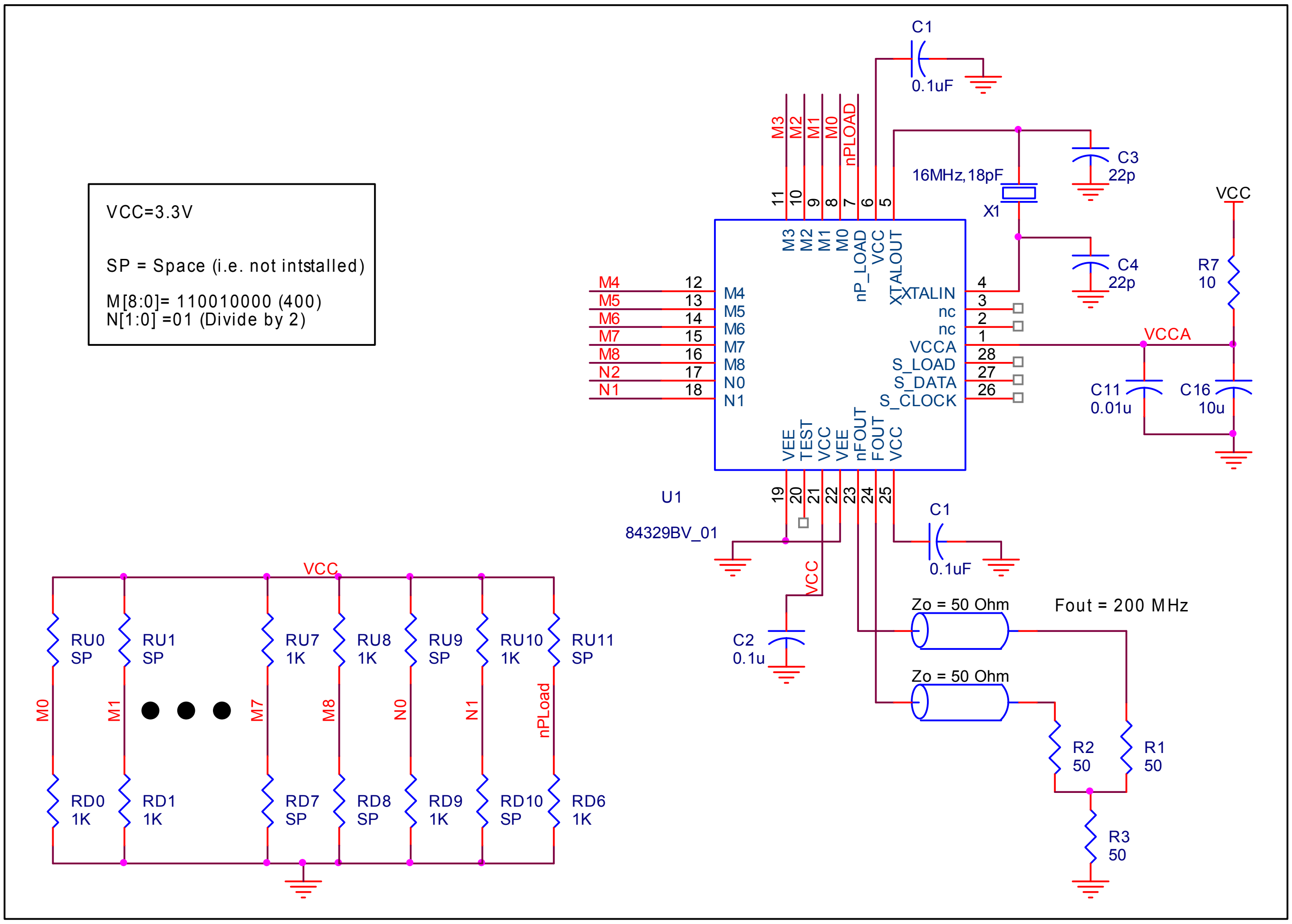



**Figure 7A. ICS84329B-01 Schematic of Recommended Layout**

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

### Power and Grounding

Place the decoupling capacitors C1, C2 and C3, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the $V_{CCA}$ pin as possible.

### Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

### Crystal

The crystal X1 should be located as close as possible to the pins 4 (XTAL_IN) and 5 (XTAL_OUT). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

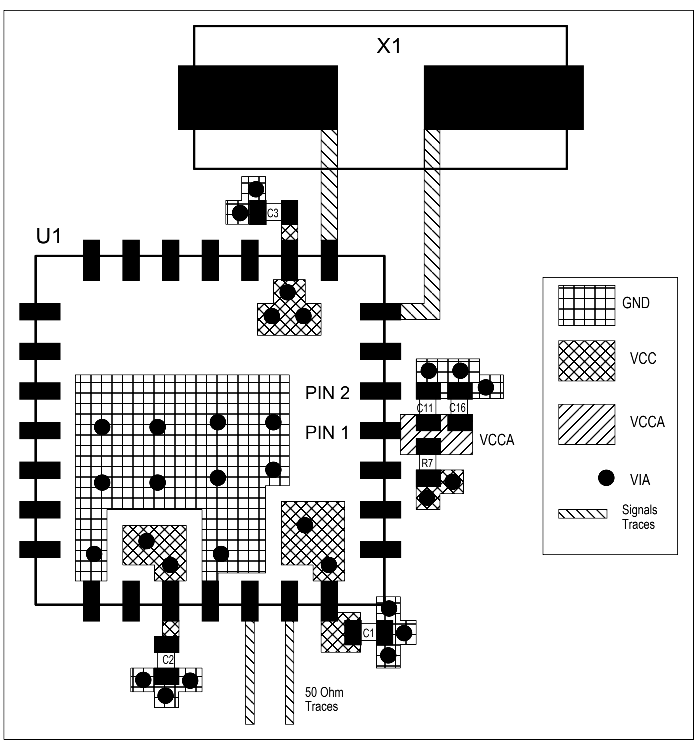



**Figure 7B. PCB Board Layout for ICS84314-02**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS84329B-01.
Equations and example calculations are also provided.

**1. Power Dissipation.**

The total power dissipation for the ICS84329B-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 140mA = **485mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

**Total Power**$_{\_MAX}$ (3.3V, with all outputs switching) = 485mW + 30mW = **515mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 31.1°C/W per Table 8A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.515W * 31.1°C/W = 86°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

### Table 8A. Thermal Resistance $\theta_{JA}$ for 28 Lead PLCC, Forced Convection

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.8°C/W | 31.1°C/W | 28.3°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

### Table 8B. Thermal Resistance $\theta_{JA}$ for 28 Lead SOIC, Forced Convection

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 76.2°C/W | 60.8°C/W | 53.2°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 46.2°C/W | 39.7°C/W | 36.8°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

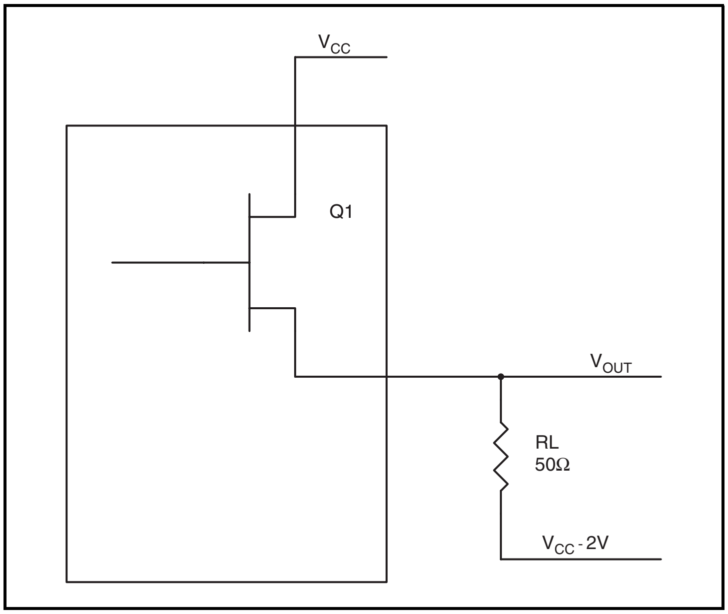



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX})$ = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX})$ = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V$ = **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V$ = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

## Reliability Information

**Table 9A. $\theta_{JA}$ vs. Air Flow Table for a 28 Lead SOIC**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 76.2°C/W | 60.8°C/W | 53.2°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 46.2°C/W | 39.7°C/W | 36.8°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

**Table 9B. $\theta_{JA}$ vs. Air Flow Table for a 28 Lead PLCC**

| Linear Feet per Minute | **0** | **200** | **500** |
|---|---|---|---|
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.8°C/W | 31.1°C/W | 28.3°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

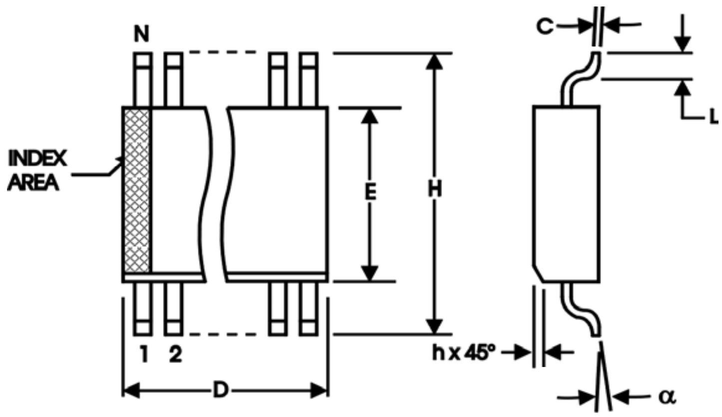
## Transistor Count

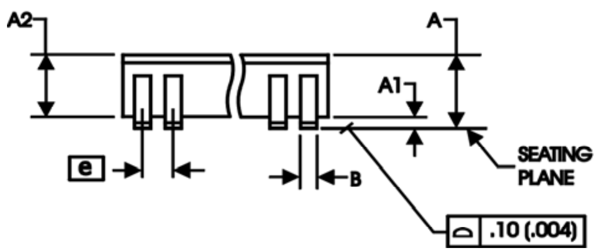
The transistor count for ICS84329B-01 is: 4408

Pin compatible with the SY89429

# Package Outline and Package Dimensions

### Package Outline - M Suffix for 28 Lead SOIC



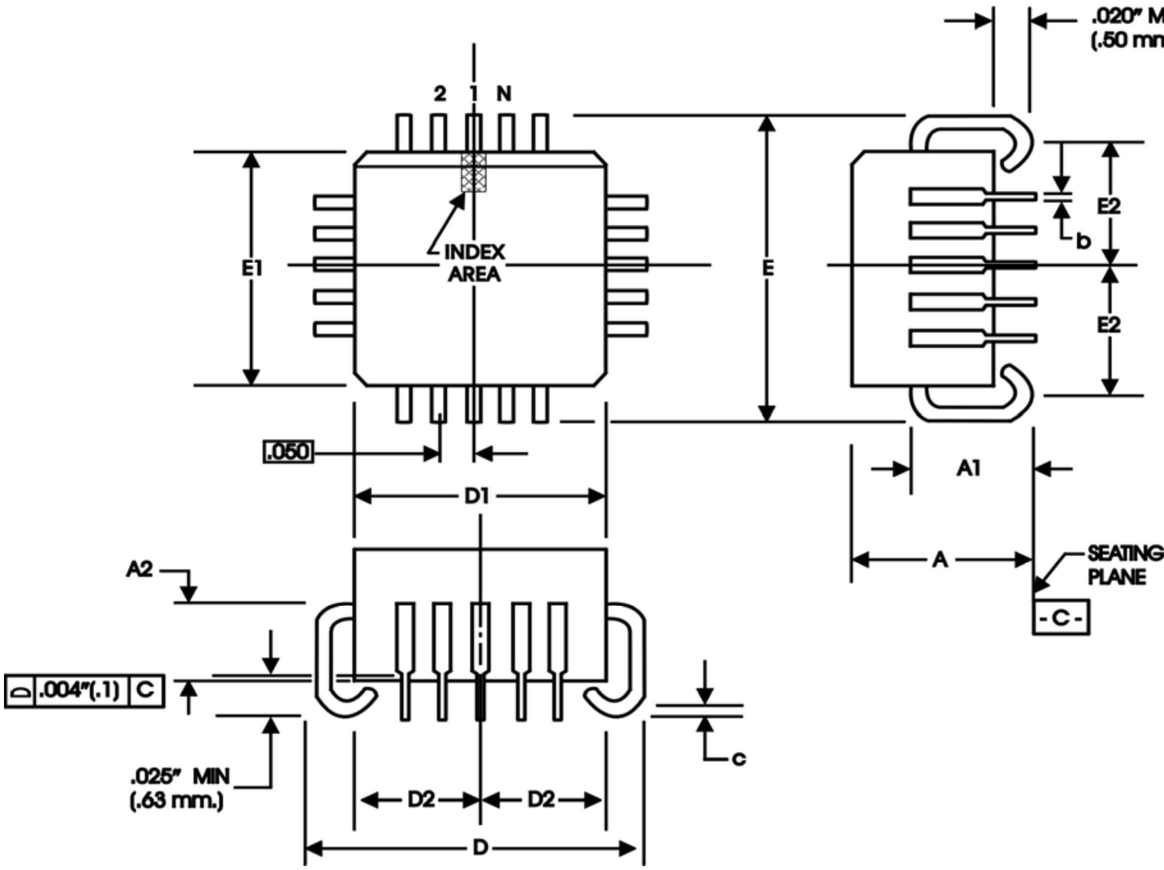




### Table 10A. Package Dimensions for 28 Lead SOIC

| JEDEC: 300 MIL<br>All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 28 | |
| **A** | | 2.65 |
| **A1** | 0.10 | |
| **A2** | 2.05 | 2.55 |
| **B** | 0.33 | 0.51 |
| **C** | 0.18 | 0.32 |
| **D** | 17.70 | 18.40 |
| **E** | 7.40 | 7.60 |
| **e** | 1.27 Basic | |
| **H** | 10.00 | 10.65 |
| **h** | 0.25 | 0.75 |
| **L** | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-013, MS-119

## Package Outline - V Suffix for 28 Lead PLCC




## Table 10B. Package Dimensions for 28 Lead PLCC

| JEDEC<br>All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 28 | |
| **A** | 4.19 | 4.57 |
| **A1** | 2.29 | 3.05 |
| **A2** | 1.57 | 2.11 |
| **b** | 0.33 | 0.53 |
| **c** | 0.19 | 0.32 |
| **D & E** | 12.32 | 12.57 |
| **D1 & E1** | 11.43 | 11.58 |
| **D2 & E2** | 4.85 | 5.56 |

Reference Document: JEDEC Publication 95, MS-018

# Ordering Information

### Table 11. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 84329BV-01 | ICS84329BV-01 | 28 Lead PLCC | Tube | 0°C to 70°C |
| 84329BV-01T | ICS84329BV-01 | 28 Lead PLCC | 500 Tape & Reel | 0°C to 70°C |
| 84329BM-01 | ICS84329BM-01 | 28 Lead SOIC | Tube | 0°C to 70°C |
| 84329BM-01T | ICS84329BM-01 | 28 Lead SOIC | 1000 Tape & Reel | 0°C to 70°C |
| 84329BM-01LF | ICS84329BM-01LF | “Lead-Free” 28 Lead SOIC | Tube | 0°C to 70°C |
| 84329BM-01LFT | ICS84329BM-01LF | “Lead-Free” 28 Lead SOIC | 1000 Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | <br>T11 | 2<br>18 | Paragraph 2 changed series resonant crystal to parallel resonant crystal.<br>Ordering Information Table - added ""ICS"" to the marking. | 11/1/04 |
| A | <br><br>T3A<br><br>T5<br>T11 | 1<br>2<br>4<br><br>6<br>18 | Features Section - added Lead-Free bullet.<br>Updated Parallel & Serial Load Operations diagram.<br>Parallel & Serial Mode Function Table - corrected S_LOAD column 3rd row, from X to L.<br>Crystal Table - added Drive Level.<br>Ordering Information Table - added Lead-Free part numbers and note. | 5/23/05 |
| A | | 1 | Features Section - corrected Output frequency range from 25MHz to 31.25MHz. | 6/10/05 |
| B | | 1 | PLCC Pin Assignment, corrected pin 5 typo from XTAL2_OUT to XTAL_OUT.<br>Converted datasheet format. | 3/26/09 |
| | | | | |

## Contact Information:

# www.IDT.com

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support**
netcom@idt.com
+480-763-2056

**Corporate Headquarters**
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)