CY7S1061G/CY7S1061GE Military

16-Mbit (1M words × 16 bit) Static RAM with PowerSnooze™ and ECC

Features

- High speed
  - t_{AA} = 10 ns
- Ultra-low power PowerSnooze™[1] device
  - Deep Sleep (DS) current I_{DS} = 45 µA maximum
- Low active and standby currents
  - I_{CC} = 90-mA typical
  - I_{SB2} = 20-mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- Embedded error-correcting code (ECC) for single-bit error correction
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free and Sn/Pb 48-ball VFBGA packages

Functional Description

The CY7S1061G/CY7S1061GE is a high-performance CMOS fast static RAM organized as 1,048,576 words by 16 bits. This device features fast access times (10 ns) and a unique ultra-low power Deep Sleep mode. With Sleep mode currents as low as 45 µA, the CY7S1061G device combines the best features of fast and low-power SRAM in industry-standard package options. The device also features embedded ECC[2]. ECC logic can detect and correct single-bit error in the accessed location. The CY7S1061GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

To access devices with a single-chip enable input, assert the chip enable input ($\overline{CE}$) LOW. To access dual chip enable devices, assert both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH for single chip enable devices and $\overline{CE}_1$ HIGH and CE_2 LOW for dual chip enable devices), or the control signals ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$) are de-asserted.

The device is placed in a low power Deep Sleep mode when the Deep Sleep pin ($\overline{DS}$) is LOW. In this state, the device is disabled for normal operation and is placed in a data retention mode. The device can be activated by de-asserting the Deep Sleep pin ($\overline{DS}$ HIGH).

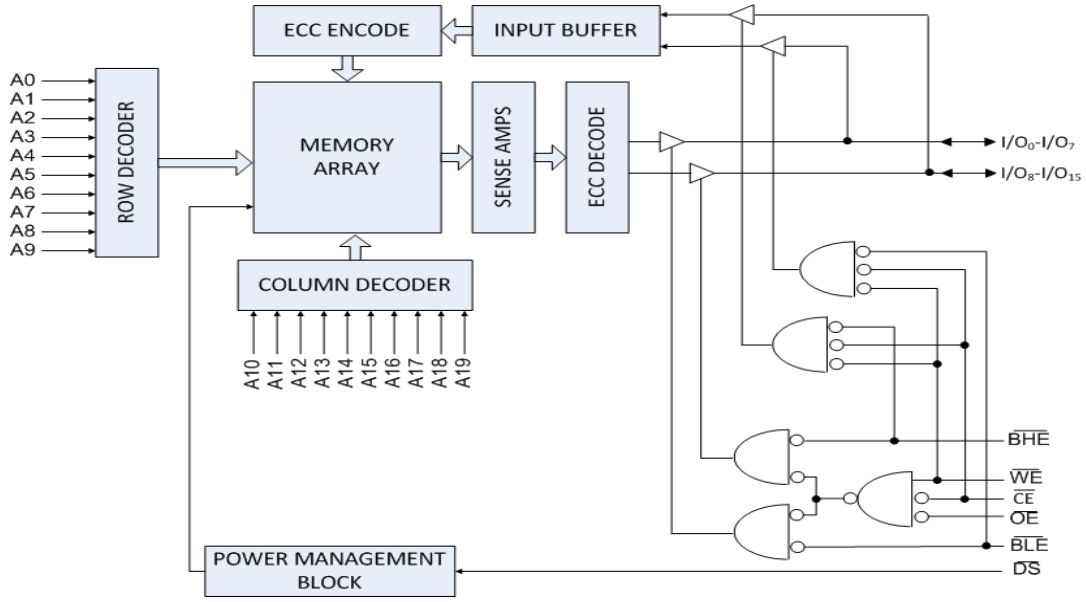
The CY7S1061G/CY7S1061G is available in 48-ball VFBGA packages.

Product Portfolio

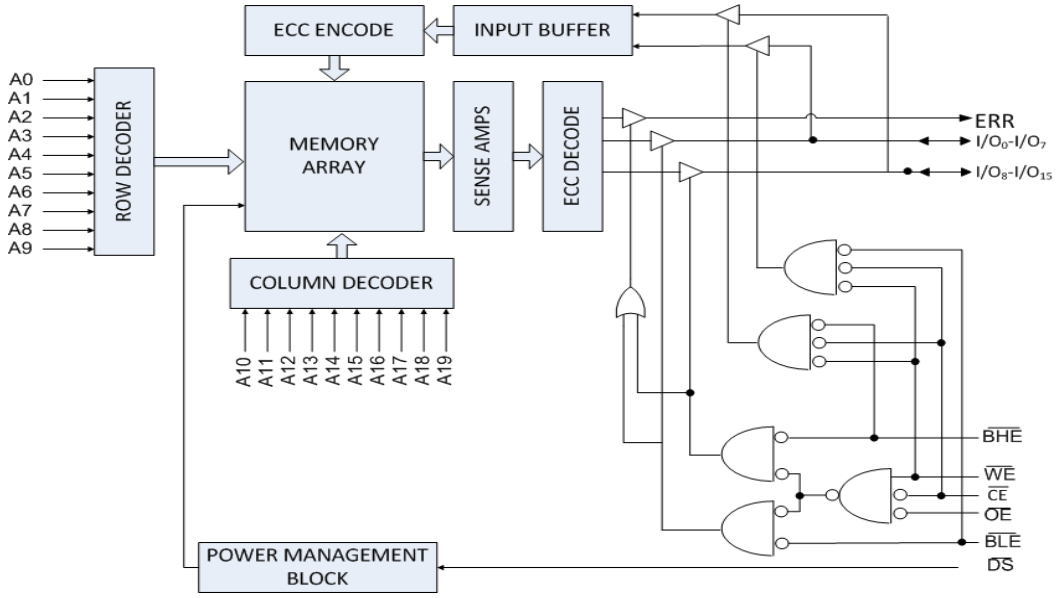
Product	Range	V_{CC} Range (V)	Speed (ns)	Current Consumption					
				Operating I_{CC} (mA) f = f_{max}		Standby, I_{SB2} (mA)		Deep-Sleep Current (µA)	
				Typ [3]	Max	Typ [3]	Max	Typ [1]	Max
CY7S1061G18	Military	1.65 V–2.2 V	15	70	120	20	60	8	45
CY7S1061G(E)30		2.2 V–3.6 V	10	90	160				
CY7S1061G		4.5–5.5 V	10	90	160				

Notes
1. Refer to AN89371 for details on PowerSnooze™ feature of this device.
2. This device does not support automatic write-back on error detection.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7S1061G



Logic Block Diagram – CY7S1061GE



Contents

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout (Top View) [4]

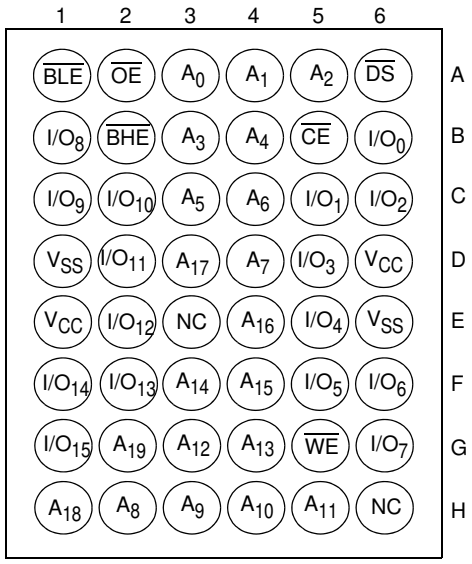
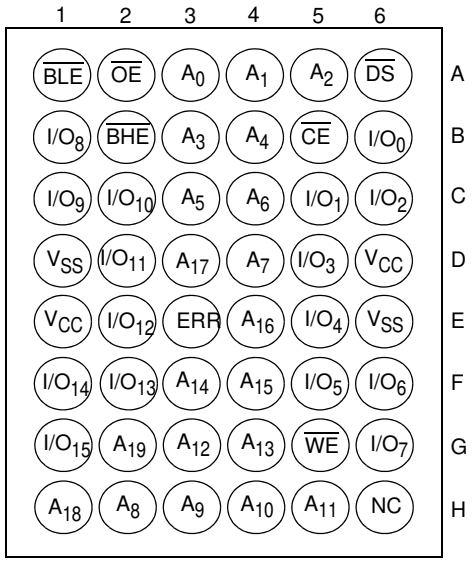


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout with ERR (Top View) [4]



Note
4. NC pins are not connected internally to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Case temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [5] ..... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in High Z State [5] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [5] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military	–55 °C to +125 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –55 °C to +125 °C

Parameter	Description		Test Conditions	10 ns / 15 ns			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA	1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.0	–	–	
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA	V_{CC} – 0.4 [7]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA	–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA	–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
V_{IH}[5, 8]	Input HIGH voltage	1.65 V to 2.2 V	–	1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V	–	2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–	2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V	–	2.2	–	V_{CC} + 0.5	
V_{IL}[5, 8]	Input LOW voltage	1.65 V to 2.2 V	–	–0.2	–	0.4	V
		2.2 V to 2.7 V	–	–0.3	–	0.6	
		2.7 V to 3.6 V	–	–0.3	–	0.8	
		4.5 V to 5.5 V	–	–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}(for all pins except $\overline{DS}$) V_{IN} = GND (or) V_{IN} ≥ V_{IH} (for DS pin only)	–5.0	–	+5.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–5.0	–	+5.0	µA

Notes

5. V_{IL} (min) = –2.0 V and V_{IH} (max) = V_{CC} + 2 V for pulse durations of less than 20 ns.
6. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
7. This parameter is guaranteed by design and is not tested.
8. For $\overline{DS}$ pin, V_{IH} (min) is V_{CC} – 0.2 V and V_{IL} (max) is 0.2 V.

DC Electrical Characteristics (continued)

Over the operating range of –55 °C to +125 °C

Parameter	Description	Test Conditions		10 ns / 15 ns			Unit
				Min	Typ [6]	Max	
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	160.0	mA
			f = 66.7 MHz	–	70.0	140.0	
I_{SB1}	Standby current – TTL inputs	Max V_{CC}, $\overline{CE}$[9] ≥ V_{IH}, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		–	–	60.0	mA
I_{SB2}	Standby current – CMOS inputs	Max V_{CC}, $\overline{CE}$[9] ≥ V_{CC} – 0.2 V, $\overline{DS} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0		–	20.0	50.0	mA
I_{DS}	Deep-Sleep current	Max V_{CC}, $\overline{CE}$[9] ≥ V_{CC} – 0.2 V, $\overline{DS} \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0		–	8.0	45.0	µA

Note

9. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Capacitance

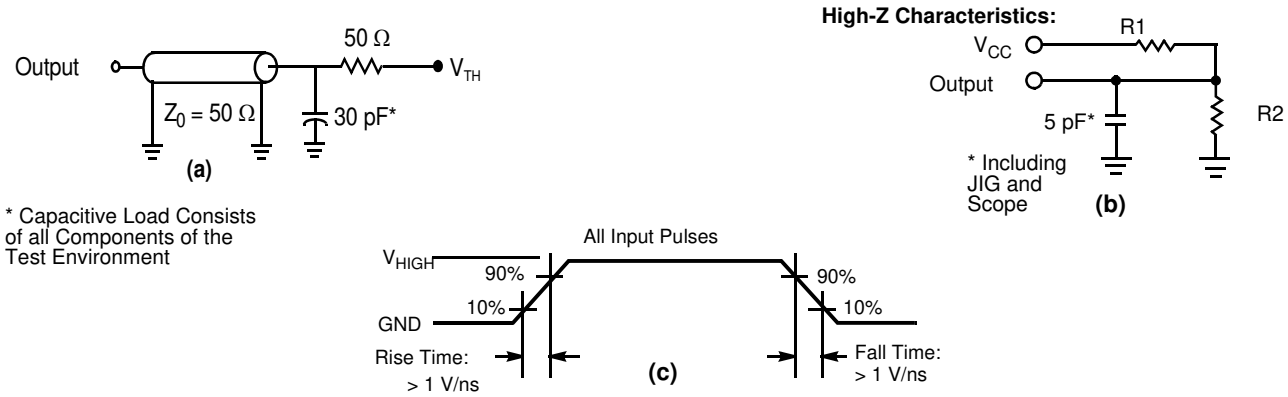
Parameter [10]	Description	Test Conditions	All packages	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC(typ)}$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.50	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [11]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	V_{CC}/2	1.5	1.5	V
V_{HIGH}	1.8	3.0	3.0	V

Notes
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and100-µs wait time after V_{CC} stabilizes to its operational value.

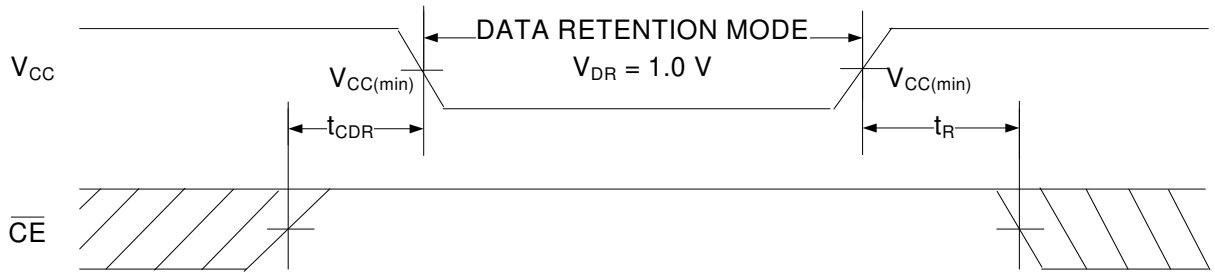
Data Retention Characteristics

Over the Operating Range of –55°C to +125 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	50.0	mA
t_{CDR} [12]	Chip deselect to data retention time		0	–	ns
t_R [12]	Operation recovery time	2.2 V < $V_{CC} \leq$ 5.5 V	10.0	–	ns
		$V_{CC} \leq$ 2.2 V	15.0	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [13, 14]



Notes

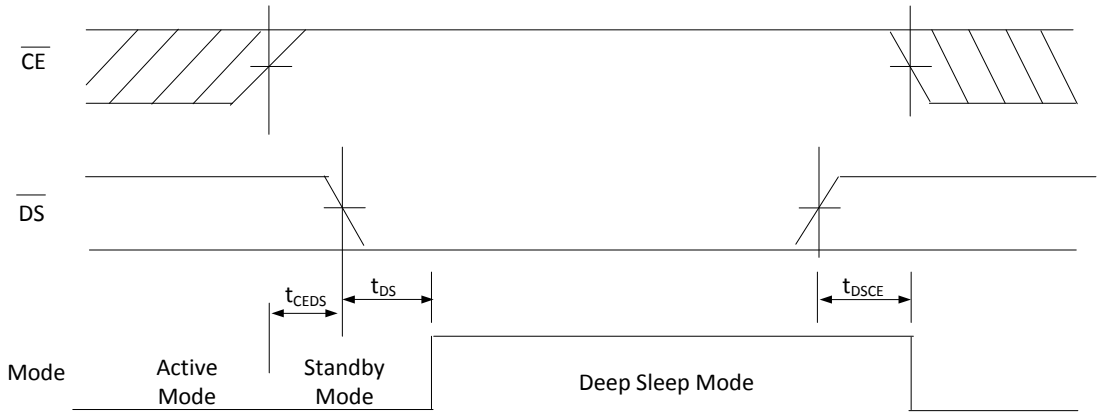
12. These parameters are guaranteed by design and are not tested.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC} (min) ≥ 100 µs or stable at V_{CC} (min) ≥ 100 µs.
14. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Deep-Sleep Mode Characteristics

Over the Operating Range of –55 °C to +125 °C

Parameter	Description	Conditions	Min	Max	Unit
I_{DS}	Deep Sleep Mode current	$V_{CC} = V_{CC}$ (max), $\overline{CE}$[15] $\geq V_{CC} - 0.2$ V, $\overline{DS} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	45	µA
t_{CEDS} [15, 16]	Time between de-assertion of $\overline{CE}$[15] and assertion of $\overline{DS}$		100	–	ns
t_{DS} [15, 16]	$\overline{DS}$ assertion to Deep Sleep mode transition time		–	1	ms
t_{DSCE} [15, 16]	Time between de-assertion of $\overline{DS}$ and assertion of $\overline{CE}$[15]		1	–	ms

Figure 5. Active, Standby, and Deep-Sleep Operation Modes [17]



Notes
15. Address, data, and control lines should not toggle within t_{DS}. They should be fixed to one of the logic levels - V_{IH} or V_{IL}.
16. These parameters are guaranteed by design and are not tested.
17. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

AC Switching Characteristics

Over the operating range of –55°C to +125 °C

Parameter [18, 19]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}	V_{CC} (stable) to the first access [20, 21]	100.0	–	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	15.0	–	ns
t_{AA}	Address to data valid / ERR valid	–	10.0	–	15.0	ns
t_{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid / ERR valid	–	10.0	–	15.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid / ERR valid	–	5.0	–	8.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [22, 23, 24]	0	–	1.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [22, 23, 24]	–	5.0	–	8.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [22, 23, 24, 25]	3.0	–	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [22, 23, 24, 25]	–	5.0	–	8.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [21]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [21]	–	10.0	–	15.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	–	8.0	ns
t_{LZBE}	Byte enable to low Z [22, 23]	0	–	1.0	–	ns
t_{HZBE}	Byte disable to high Z [22, 23]	–	5.0	–	8.0	ns
Write Cycle [26, 27]						
t_{WC}	Write cycle time	10.0	–	15.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [25]	7.0	–	12.0	–	ns
t_{AW}	Address setup to write end	7.0	–	12.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
t_{SD}	Data setup to write end	5.0	–	8.0	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [22, 23, 24]	3.0	–	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [22, 23, 24]	–	5.0	–	8.0	ns
t_{BW}	Byte Enable to End of Write	7.0	–	12.0	–	ns

Notes

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V), and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading shown in part (a) of Figure 3 on page 7, unless specified otherwise
19. $\overline{DS}$ must be HIGH for chip access. Refer to AN89371 for details.
20. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.
21. These parameters are guaranteed by design and are not tested.
22. t_{HZOE}, t_{HZCE}, t_{HZWE},and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 3 on page 7. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.
23. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
24. Tested initially and after any design or process changes that may affect these parameters.
25. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
27. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 6. Read Cycle No. 1 of CY7S1061G (Address Transition Controlled) [28, 29]

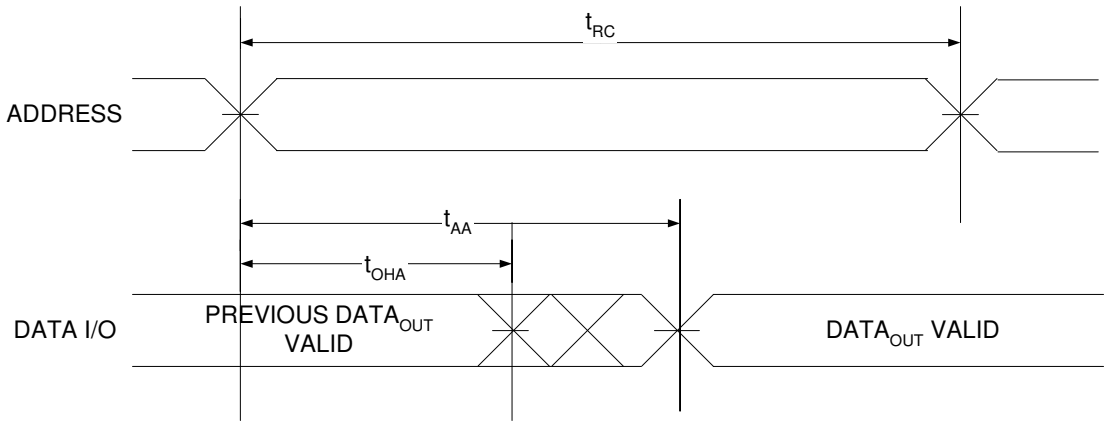
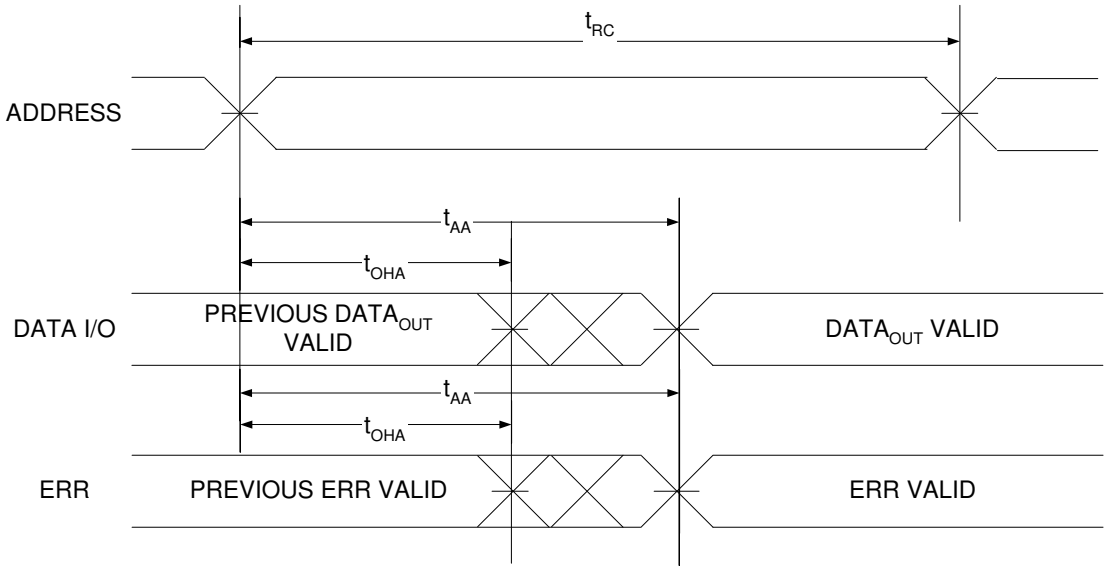


Figure 7. Read Cycle No. 2 of CY7S1061GE (Address Transition Controlled) [28, 29]



Notes
28. The device is continuously selected. $\overline{OE}$= V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
29. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 8. Read Cycle No. 3 ($\overline{OE}$ Controlled) [30, 31, 32]

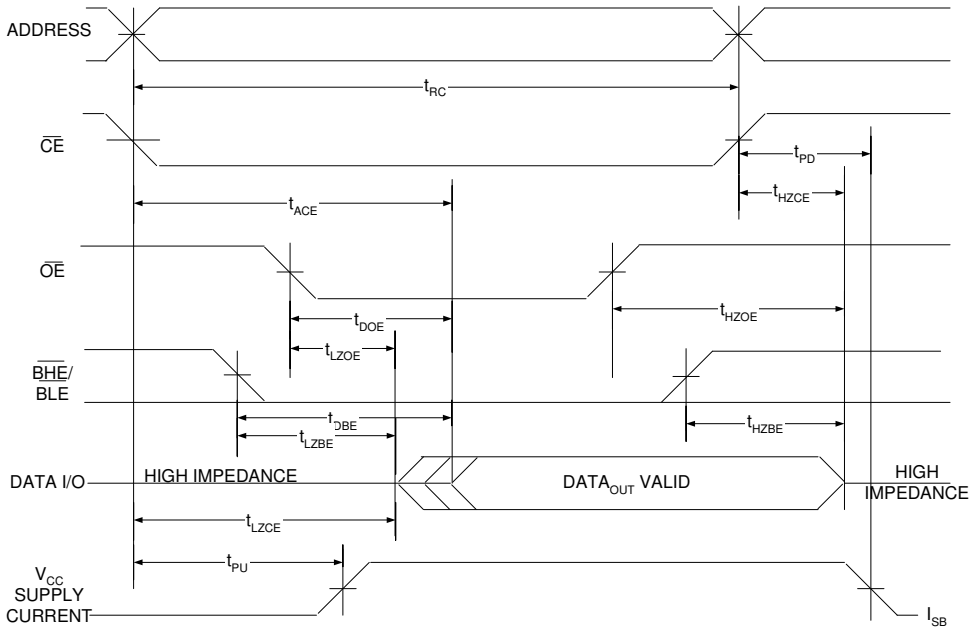
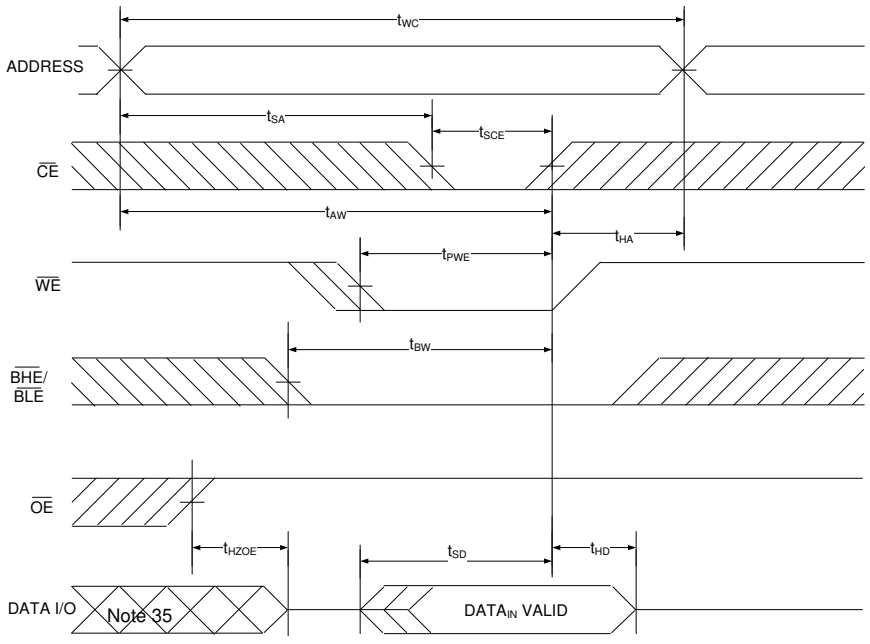


Figure 9. Write Cycle No. 1 ($\overline{CE}$ Controlled) [31, 33, 34]



Notes

30. $\overline{WE}$ is HIGH for read cycle.
31. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
32. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
33. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
34. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
35. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [36, 37, 38, 39]

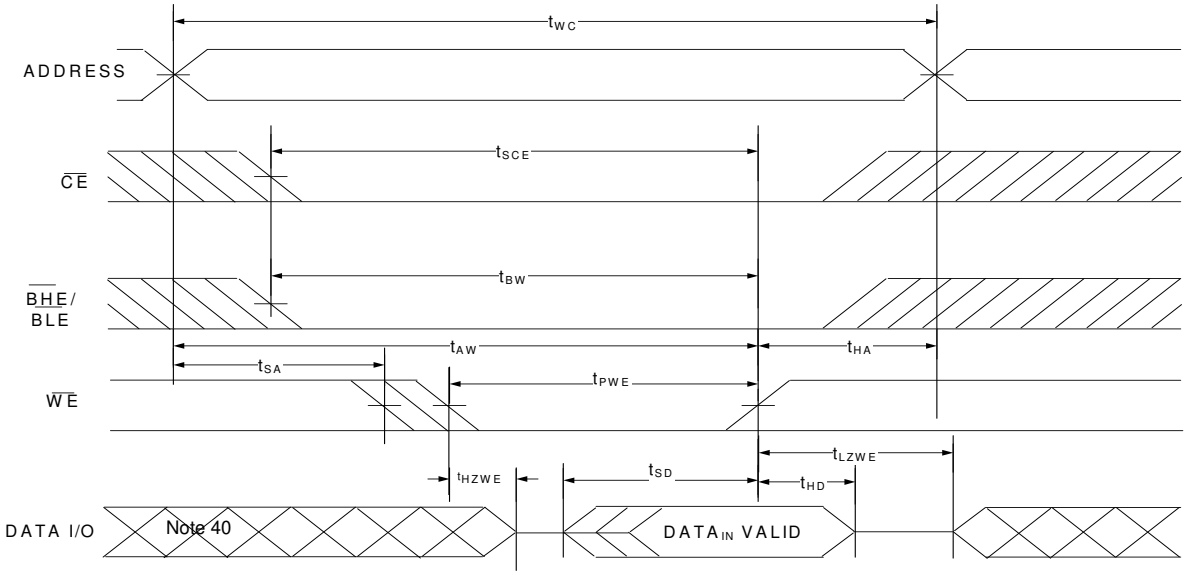
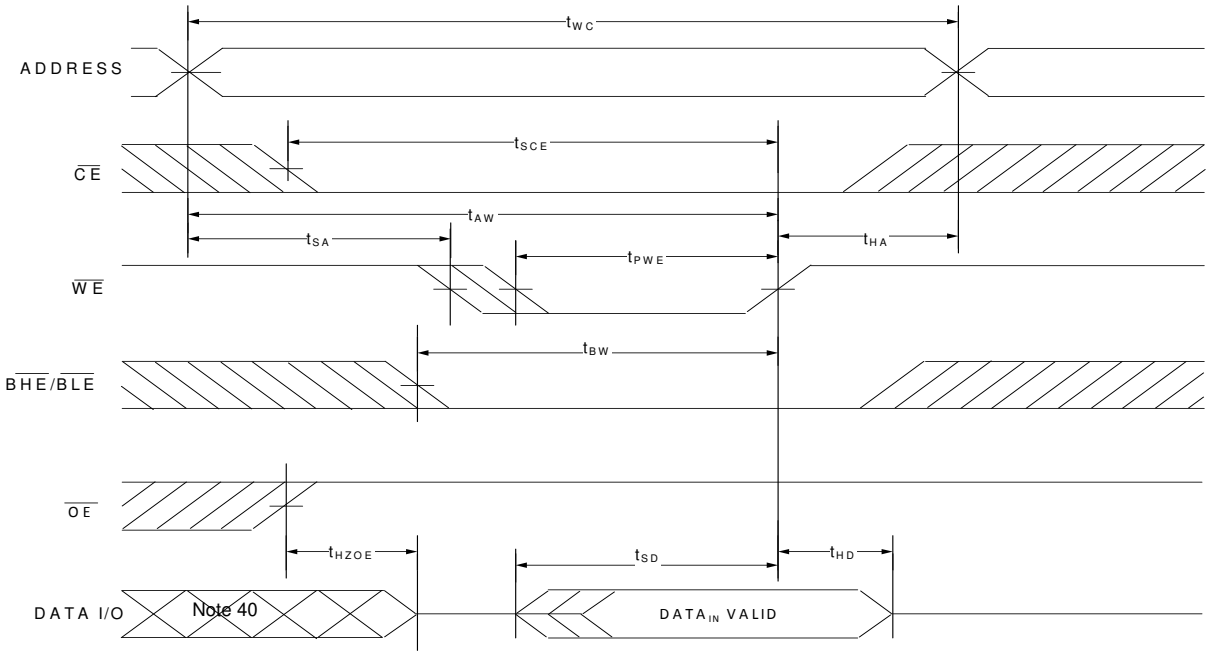


Figure 11. Write Cycle No. 3 ($\overline{WE}$ controlled) [36, 38, 39]

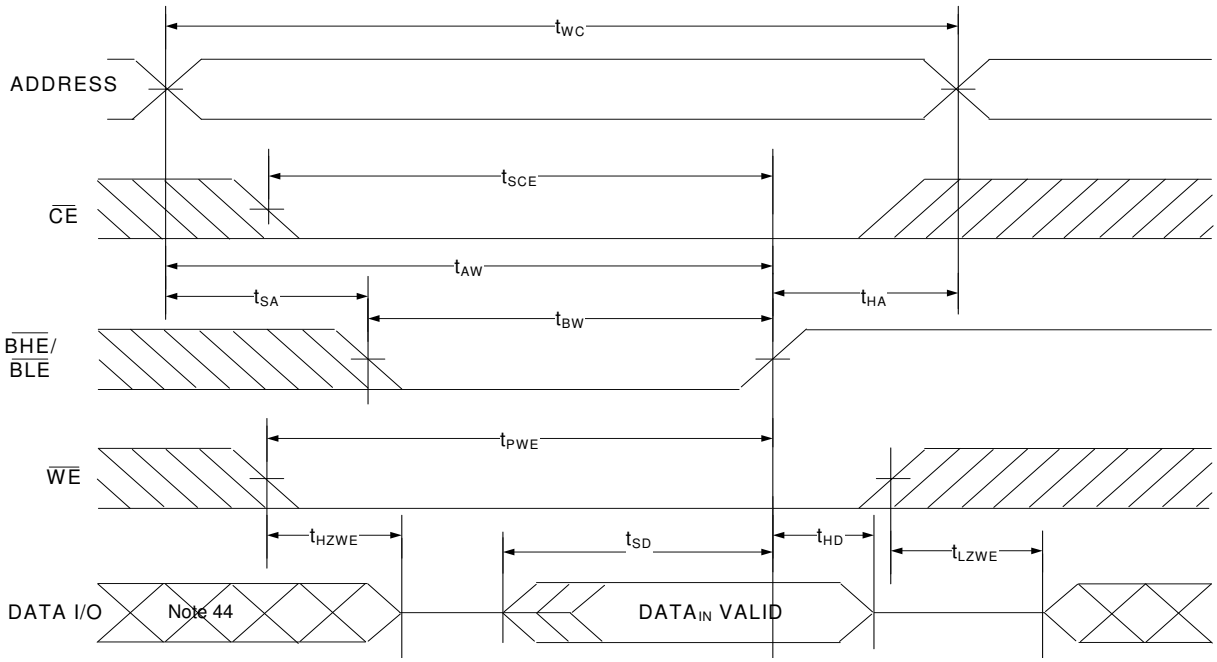


Notes

36. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
37. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.
38. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
39. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
40. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 12. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [41, 42, 43]



Notes

41. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
42. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
43. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
44. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{DS}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	H	X[45]	X[45]	X[45]	X[45]	High-Z	High-Z	Standby	Standby (I_{SB})
H	L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
H	L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I_{CC})
H	L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I_{CC})
H	L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
H	L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I_{CC})
H	L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I_{CC})
H	L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})
L[46]	H	X	X	X	X	High-Z	High-Z	Deep Sleep	Deep-Sleep Ultra Low Power (I_{DS})
L	L	X	X	X	X	–	–	Invalid mode[47]	–
H	L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7S1061GE

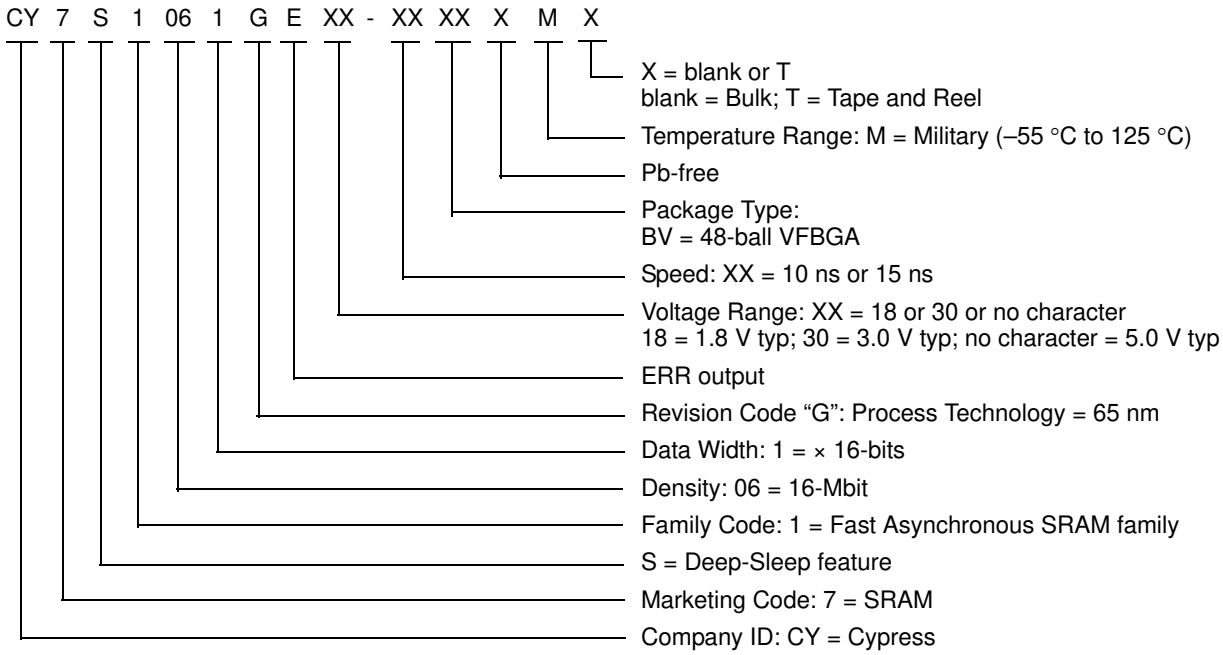
Output [48]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

Notes
45. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
46. V_{IL} on $\overline{DS}$ must be $\leq$ 0.2 V.
47. This mode does not guarantee data retention. Power cycling needs to be performed for the device to return to normal operation.
48. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

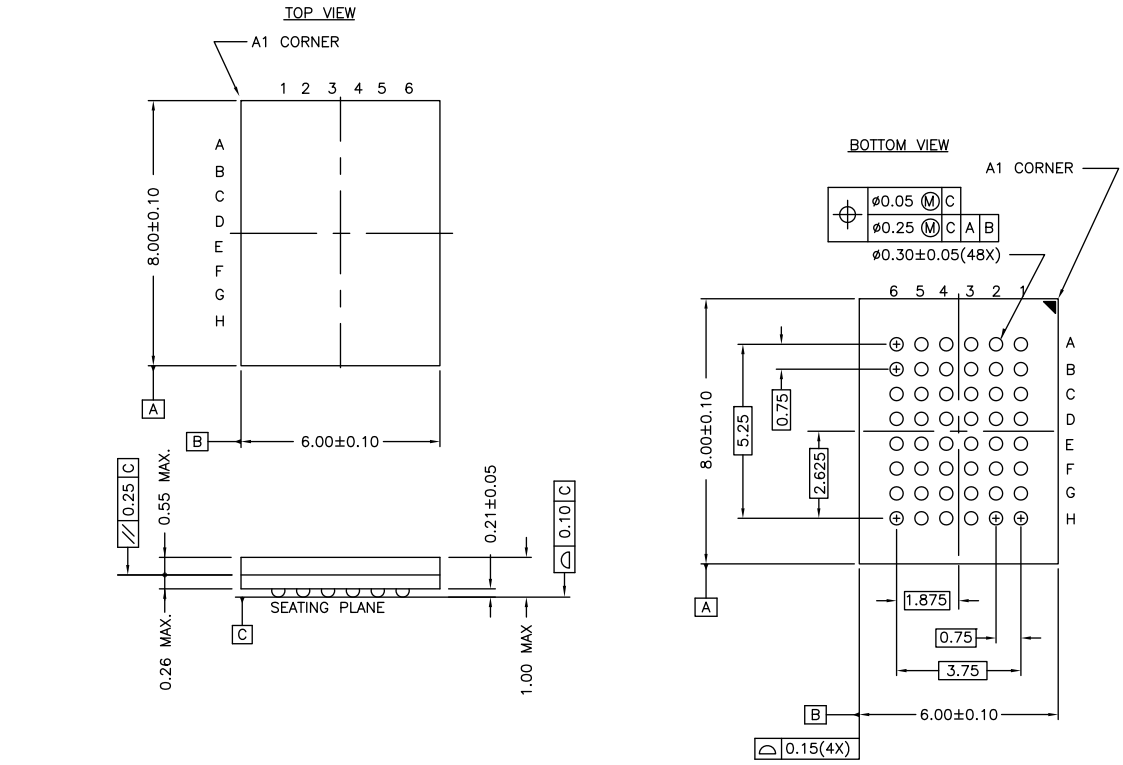
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	ERR Pin/ Ball	Operating Range
10	2.2 V–3.6 V	CY7S1061GE30-10BVM	51-85150	48-ball VFBGA (Sn/Pb)	Yes	Military

Ordering Code Definitions



Package Diagrams

Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/output
$\overline{OE}$	Output Enable
SRAM	Static random access memory
TTL	Transistor-transistor logic
VFBGA	Very fine-pitch ball grid array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7S1061G/CY7S1061GE Military, 16-Mbit (1M words × 16 bit) Static RAM with PowerSnooze™ and ECC Document Number: 002-18749				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5652976	VINI	03/20/2017	New datasheet.
*A	5899947	VINI	10/03/2017	Changed datasheet status to Final. Removed the following MPNs: CY7S1061G18-15BVXM, CY7S1061GE18-15BVXM, CY7S1061G18-15BVM, CY7S1061GE18-15BVM, CY7S1061G30-10BVXM, CY7S1061GE30-10BVXM, CY7S1061G30-10BVM, CY7S1061G-10BVXM, CY7S1061GE-10BVXM, CY7S1061G-10BVM, CY7S1061GE-10BVM

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