Analog System Lab Kit PRO

MANUAL

Texas Instruments


Texas Instruments

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Introduction

What you need to know before you get started

Analog System Lab

Although digital signal processing is the most common form of processing signals, analog signal processing cannot be completely avoided since the real world is analog in nature. Consider a typical signal chain (Figure below).

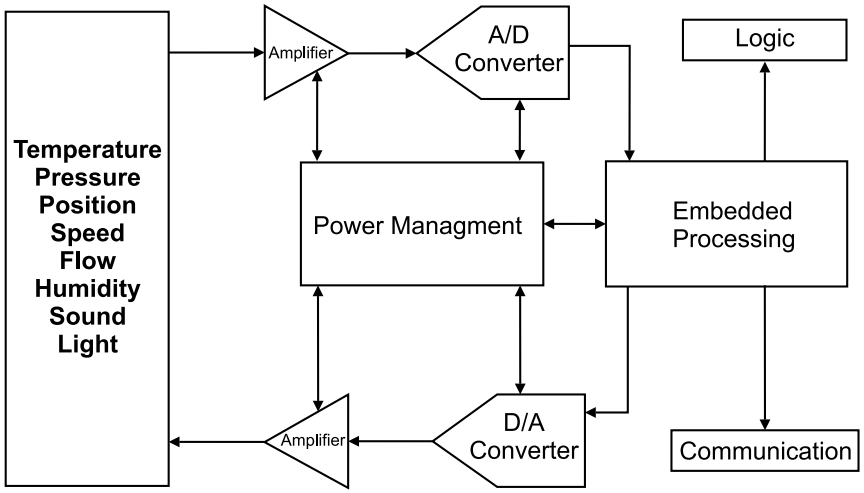


Figure: Signal Chain in an Electronic System

Typical signal chain

1. A sensor converts the real-world signal into an analog electrical signal. This analog signal is often weak and noisy.
2. Amplifiers are needed to strengthen the signal. Analog filtering may be necessary to remove noise from the signal. This "front end" processing improves the signal-to-noise ratio. Three of the most important building blocks used in this stage are (a) Operational Amplifiers, (b) Analog multipliers and (c) Analog Comparators.
3. An analog-to-digital converter transforms the analog signal into a stream of 0s and 1s.
4. The digital data is processed by a CPU, such as a DSP, a microprocessor, or a microcontroller. The choice of the processor depends on how intensive the computation is. A DSP may be necessary when real-time signal processing is needed and the computations are complex. Microprocessors and microcontrollers may suffice in other applications.
5. Digital-to-analog conversion (DAC) is necessary to convert the stream of 0s and 1s back into analog form.
6. The output of the DAC has to be amplified before the analog signal can drive an external actuator.

It is evident that analog circuits play a crucial role in the implementation of an electronic system.

The goal of the Analog System Lab Course is to provide students an exposure to the fascinating world of analog and mixed-signal signal processing. The course can be adapted for an undergraduate or a postgraduate curriculum. As part of the lab course, the student will build analog systems using analog ICs and study their macro models, characteristics and limitations. Our philosophy in designing this lab course has been to focus on system design rather than circuit design. We feel that many Analog Design classes in the colleges focus on the circuit design aspect, ignoring the issues encountered in system design. In the real world, a system designer uses the analog ICs as building blocks. The focus of the system designer are to optimize system-level cost, power, and performance. IC manufacturers such as Texas Instruments offer a large number of choices of integrated circuits keeping in mind the diverse requirements of system designers. As a student, you must be aware of these diverse offerings of semiconductors and select the right IC for the right application. We have tried to emphasize this aspect in designing the experiments in this manual.

Organization of the Course

In designing the lab course, we have assumed that there are about 12 during a semester. We have designed 14 experiments which can be carried out either individually or by groups of two students. The experiments in Analog System Lab can be categorized as follows.

Part I - Learning the basics

In the first part, the student will be exposed to the operation of the basic building blocks of analog systems. Most of the experiments in the **Analog System Lab Course** are centered around the following two components.

- The OP-amp **TL082**, a general purpose JFET-input operational amplifier, made by Texas Instruments.
- Wide-bandwidth, precision analog multiplier **MPY634** from Texas Instruments.

Using these components, the student will build gain stages, buffers, instrumentation amplifiers and voltage regulators. These experiments bring out several important issues, such as measurement of gain- bandwidth product, slew-rate, and saturation limits of the operational amplifiers.

Part II - Building analog systems

Part-II concentrates on building analog systems using the blocks mentioned above.

First, we introduce **integrators** and **differentiators** which are essential for implementing filters that can band-limit a signal prior to the sampling process to avoid aliasing errors.

We then introduce the *analog comparator*, which is a mixed-mode device - its input is analog and output is digital. In a comparator, the rise time, fall time, and delay time are important apart from input offset.
A function generator is also a mixed-mode system that uses an integrator and a regenerative comparator as building blocks. The function generator is capable of producing a triangular waveform and square waveform as outputs. It is also useful in Pulse Width Modulation in DC-to-DC converters, switched-mode power supplies, and Class-D power amplifiers.

The analog multiplier, which is a voltage or current controlled amplifier, finds applications in communication circuits in the form of mixer, modulator, demodulator and phase detector. We use the multiplier in building Voltage Controlled Oscillators, Frequency Modulated waveform generators, or Frequency Shift Key waveform generators in modems, Automatic Gain Controllers, Amplitude Stabilized Oscillators, Self-tuned Filters and Frequency Locked Loop using voltage controlled phase generators and VCOs and multiplier as phase detector are built and their lock range and capture range.

In the Analog System Lab, the frequency range of all applications has been restricted to 1-10 kHz, with the following in mind - (a) The macromodels for the ideal device can be used in simulation, (b) A PC can be used in place of an oscilloscope. We have also included an experiment that can help the student use a PC as an oscilloscope. We also suggest an experiment on the development of macromodels for an OP-Amp.

What is our goal?

At the end of Analog System Lab, we believe you will have the following know-how about analog system design.

1. You will learn about the characteristics and specification of analog ICs used in electronic systems.
2. You will learn how to develop a macromodel for an IC based on its terminal characteristics, I/O characteristics, DC-transfer characteristics, frequency response, stability characteristic and sensitivity characteristic.
3. You will be able to make the right choice for an IC for a given application.
4. You will be able to perform basic fault diagnosis of an electronic system.

Lab Setup

The setup for the Analog System Lab is very simple and requires the following.

1. ASLK PRO and the associated Lab Manual from Texas Instruments India - the lab kit comes with required connectors. Refer to *Chapter 1.4* for an overview of the kit.
2. Oscilloscope. We provide an experiment that helps you build a circuit to directly interface analog outputs to an oscilloscope (See *Chapter C*).
3. Dual power supply with the operating voltages of ±10V.
4. Function generators which can operate in the range on 1 to 10 MHz and capable of generating sine, square and triangular waves.
5. A computer with installed circuit simulation software.

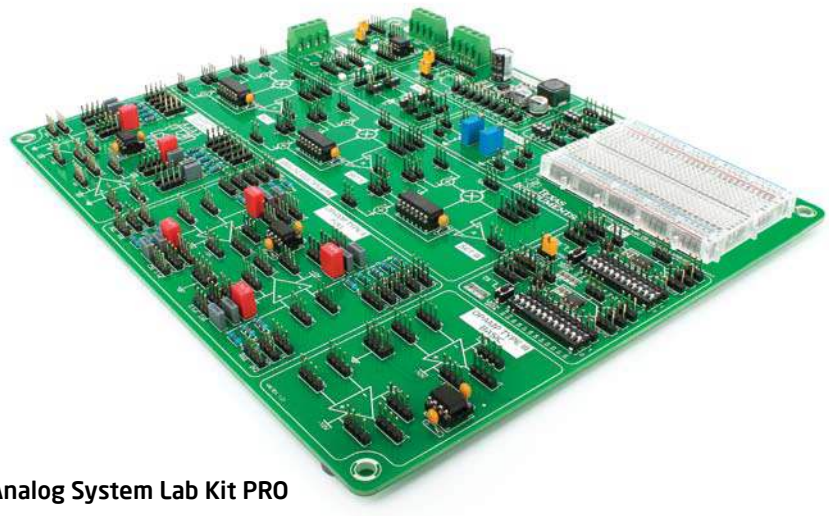
In all the experiments of Analog System Lab, please note the following.

1. When we do not explicitly mention the magnitude and frequency of the input waveform, please use 0 to 1V as the amplitude of the input and 1 kHz as the frequency.
2. Always use sinusoidal input when you plot the frequency response and use square wave input when you plot the transient response.
3. Precaution! Please note that **TL082** is a dual OP-Amp. This means that the IC has two OP-Amp circuits. If your experiment requires only one of the two ICs, do not leave the inputs and output of the other OP- Amp open; instead, place the second OP-Amp in unity-gain mode and ground the inputs.
4. Advisory to Students and Instructors. We strongly advise that the student performs the simulation experiments outside the lab hours. The student must bring a copy of the simulation results to the class and show it to the instructor at the beginning of the class. The lab hours must be utilized only for the hardware experiment and comparing the actual outputs with simulation results.

System Lab Kit overview

Hardware

ASLK PRO has been developed at Texas Instruments India. This kit is designed for undergraduate engineering students to perform analog lab experiments. The main idea behind ASLK PRO is to provide a cost efficient platform or test bed for students to realize almost any analog system using general purpose ICs such as OP-Amps and analog multipliers.



Analog System Lab Kit PRO

ASLK PRO comes with three general-purpose operational amplifiers (**TL082**) and three wide-bandwidth precision analog multipliers (**MPY634**) from Texas Instruments. We have also included two 12-bit parallel-input multiplying digital-to-analog converters **DAC7821**, a wide-input non-synchronous buck-type DC/DC controller **TPS40200**, and a low dropout regulator **TPS7250** from Texas Instruments. A portion of ASLK PRO is left for general-purpose prototyping which can be used for carrying out mini-projects.

The kit has a provision to connect ±10V DC power supply. The kit comes with the necessary short and long connectors.

This comprehensive user manual included with the kit gives complete insight of how to use ASLK PRO. The manual covers exercises of analog system design along with brief theory and simulation results.

Refer to *Appendix A* for the details of the integrated circuits that are included in ASLK PRO. Refer to *Appendix D* for additional details of ASLK PRO.

Software

The following software is necessary to carry out the experiments suggested in this manual.

1. **TINA** or **PSpice** or any powerful simulator based on the SPICE Simulation Engine
2. **FilterPro** - A software program for designing analog filters
3. **SwitcherPro** - A software program for designing power supplies

We will assume that you are familiar with the concept of simulation and are able to simulate a given circuit.

FilterPro is a program for designing active filters. At the time of writing this manual, **FilterPro** Version 3.1 is the latest. It supports the design of different types of filters, namely *Bessel*, *Butterworth*, *Chebychev*, *Gaussian*, and linear-phase filters. The software can be used to design low-pass filters, high-pass filters, band-stop filters, and band-pass filters with up to 10 poles. The software can be downloaded from **[9]**.

Getting to know ASLK PRO

The Analog System Lab kit ASLK PRO is divided into many sections. Refer to the photo of ASLK PRO when you read the following description.

1. **There are three TL082 OP-Amp** ICs labelled 1, 2, 3 on ASLK PRO. Each of these ICs has two amplifiers, which are labelled A and B. Thus 1A and 1B are the two OP-AMps on OP-AMP IC 1, etc. The six OP-amps are categorized as below.

OP-Amp	Type	Purpose
1A	TYPE I	Inverting Configuration only
1B	TYPE I	Inverting Configuration only
2A	TYPE II	Full Configuration
2B	TYPE II	Full Configuration
3A	TYPE III	Basic Configuration
3B	TYPE III	Basic Configuration

Thus, the OP-amps are marked TYPE I, TYPE II and TYPE III on the board. The OP-Amps marked TYPE I can be connected in the inverting configuration only. With the help of connectors, either resistors or capacitors can be used in the feedback loop of the amplifier. There are two such TYPE I amplifiers. There are two TYPE II amplifiers which can be configured to act as inverting or non-inverting. Finally, we have two TYPE III amplifiers which can be used as voltage buffers.

2. **Three analog multipliers** are included in the kit. These are wide-bandwidth precision analog multipliers from Texas Instruments (**MPY634**). Each multiplier is a 14-pin IC and operates on internally provided ±10V supply.

3. **There are two digital-to-analog converters (DAC)** provided in the kit, labeled **DAC I** and **DAC II**. Both the DACs are **DAC7821** from Texas Instruments. They are 12-bit, parallel-input multiplying DACs which can be used in place of analog multipliers in circuits like AGC/AVC. Ground and power supplies are provided internally to the DAC. **DAC Logic Supply Jumper** can be used to connect logic power supplies of both **DAC I** and **DAC II** to either **LDO** or **DC/DC** converter located on the board. Using **Tri-state switches** you can set 12-bits of input data for each DAC to desired value. Click the **Latch Data button** to trigger Digital-to-analog conversion.

4. We have included a **wide-input non-synchronous DC/DC buck converter** **TPS40200** from Texas Instruments on ASLK PRO. The converter provides an output of 3.3V over a wide input range of 5.5-15V at output currents ranging from 0.125A to 2.5A. Using **Vout SEL jumper** you can select output voltage to be either 5V or 3.3V. Another jumper allows you to select whether input voltage is provided from the board (+10V), or externally using screw terminals.

5. We have included **two transistor sockets** on the board, which are needed in designing an LDO regulator (*Experiment 10*), or custom experiments.

6. **A specialized LDO regulator IC** (**TPS7250**) has been included on the board, which can provide a constant output voltage for input voltage ranging from 5.5V to 11V. Ground connection is internally provided to the IC. Using **ON/OFF jumper** you can enable or disable LDO IC. Another jumper allows you to select whether input voltage is provided from the board (+10V), or externally using screw terminals.

7. **There are two 1kΩ trimmers** (potentiometer) in the kit to enable the designer to obtain a variable voltage if needed for a circuit. The potentiometers are labeled **P1** and **P2**. These operate respectively in the range 0V to +10V, and -10V to 0V.

8. The kit has a **screw terminals to connect ±10V power supply**. All the ICs on the board are internally connected to power supply. Please refer to *Appendix D* for schematics of ASLK PRO.

9. We have included **two diode sockets** on the board, which can be used as rectifiers in custom laboratory experiments.

10. The top right portion of the kit is a **general-purpose area which can be used as a proto-board**. ± 10V points and GND are provided for this area.

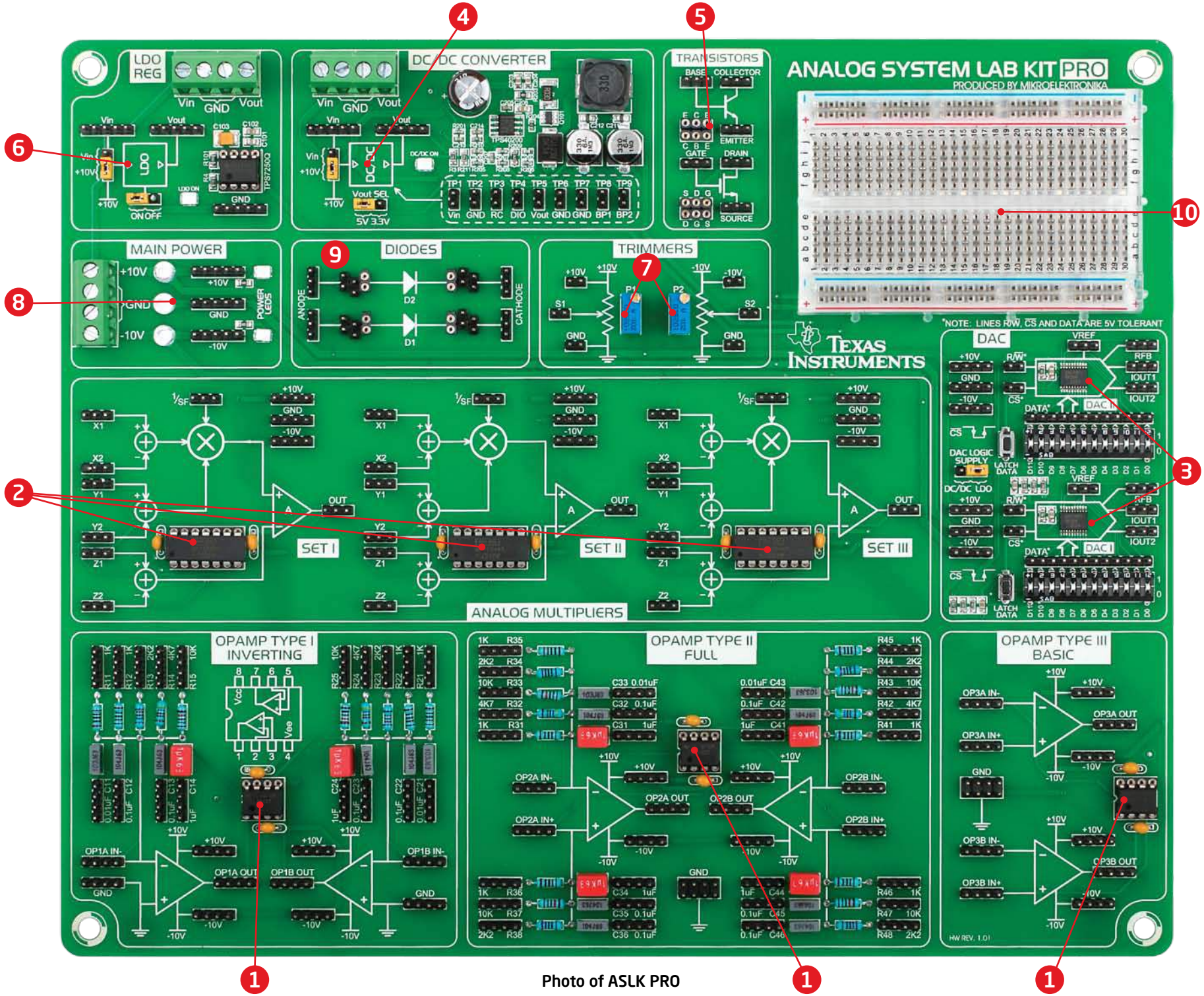


Photo of ASLK PRO

Organization of the Manual

There are *14 experiments* in this manual and the next *14 chapters* are devoted to them, We recommend that in the first cycle of experiments, the instructor introduces the ASLK PRO and ensure that all the students are familiar with a simulation software. A warm-up exercise can be included, where the students are asked to use the simulation software. For each of the experiments, we have clarified the goal of the experiment and provided the theoretical background. The Analog System Lab can be conducted parallel to a theory course on Analog Design or as a separate lab that follows a theory course.

The student should have the following skills to pursue Analog System Lab:

1. Basic understanding of electronic circuits
2. Basic computer skills required to run the simulation tools
3. Ability to use the oscilloscope
4. Concepts of gain, bandwidth, transfer function, filters, regulators and wave shaping

Chapter 1

Experiment 1

Study the characteristics of negative feedback amplifiers and design of an instrumentation amplifier

Goal of the experiment

The goal of this experiment is two-fold. In the first part, we will understand the application of negative feedback in designing amplifiers. In the second part, we will build an instrumentation amplifier.

1.1 Brief theory and motivation

1.1.1 Unity Gain Amplifier

An OP-Amp **[8]** can be used in negative feedback mode to build unity gain amplifiers, non-inverting amplifiers and inverting amplifiers. While an ideal OP-Amp is assumed to have infinite open-loop gain and infinite bandwidth, real OP-Amps have finite numbers for these parameters. Therefore, it is important to understand some limitations of real OP-Amps, such as finite Gain-Bandwidth Product (GB). Similarly, the slew rate and saturation limits of an operational amplifier are equally important. Given an OP-amp, how do we measure these parameters?

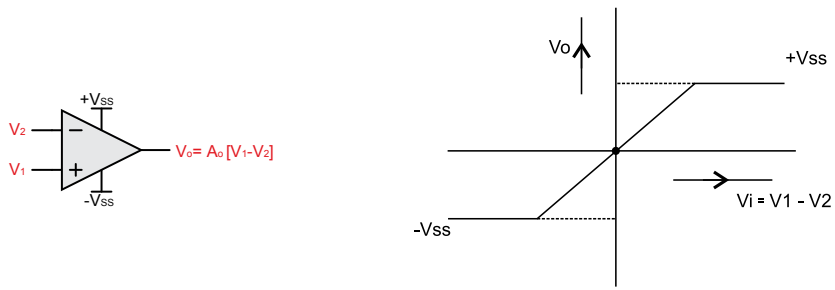


Figure 1.1: An ideal Dual-Input, Single-Output OP-Amp and its I-O characteristic

Since the frequency and transient response of an amplifier are impacted by these parameters, we can measure the parameters if we have the frequency and transient response of the amplifier; you can obtain these response characteristics by applying sinusoidal and square wave inputs respectively. We invite the reader to view the recorded lecture **[16]**.

An OP-Amp can be considered as a Voltage Controlled Voltage Source (VCVS) with the voltage gain tending towards infinity. For finite output voltage, the input voltage is practically zero. This is the basic theory of OP-Amp in the negative feedback configuration. Figure 1.1 shows a differential-input, single-ended-output OP-Amp which uses dual supply $\pm Vss$ for biasing.

$$V_0 = A_0 \cdot (V_1 - V_2) \tag{1.1}$$

$$V_1 - V_2 = \frac{V_0}{A_0} \tag{1.2}$$

In the above equations, A_0 is the open-loop gain; for real amplifiers, A_0 is in the range 10^5 to 10^6 and hence $V_1 \approx V_2$. A unity feedback circuit is shown in the Figure 1.2. It is easy to see that,

$$\frac{V_0}{V_s} = \frac{A_0}{1 + A_0} \tag{1.3}$$

$$\frac{V_0}{V_s} \to 1 \; as \; A_0 \to \infty \tag{1.4}$$

In OP-amps, closed loop gain A is frequency dependent, as shown in the equation below, where ω_{d1} and ω_{d2} are called the dominant poles of the OP-amp. This transfer function is typical OP-Amp that has *internal frequency compensation*. Please view the recorded lecture **[17]** to get to know more about frequency compensation.

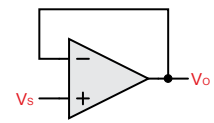


Figure 1.2: A Unity Gain System

$$A = \frac{A_0}{(1 + s/\omega_{d1})(1 + s/\omega_{d2})} \tag{1.5}$$

We can now write the transfer function T for a unity-gain amplifier as,

$$T = \frac{1}{1 + 1/A} \tag{1.6}$$

$$= \frac{1}{(1 + 1/A_0 + s/A_0\omega_{d1} + s/A_0\omega_{d2} + s^2/A_0\omega_{d1}\omega_{d2})}$$

$$= \frac{1}{(1 + (s/GB + s/A_0\omega_{d2} + s^2/GB \cdot \omega_{d2}))} \tag{1.7}$$

The term $GB = A_0\omega_{d1}$, also known as the gain bandwidth product of the operational amplifier, is one of the most important parameters in OP-Amp negative feedback circuit. The above transfer function can be rewritten as

$$T = \frac{1}{1 + s/\omega_0 Q + s^2/\omega_0^2}$$

where

$$Q = \frac{1}{\sqrt{\frac{\omega_{d2}}{GB}} + \frac{1}{A_0}\sqrt{\frac{GB}{\omega_{d2}}}}$$

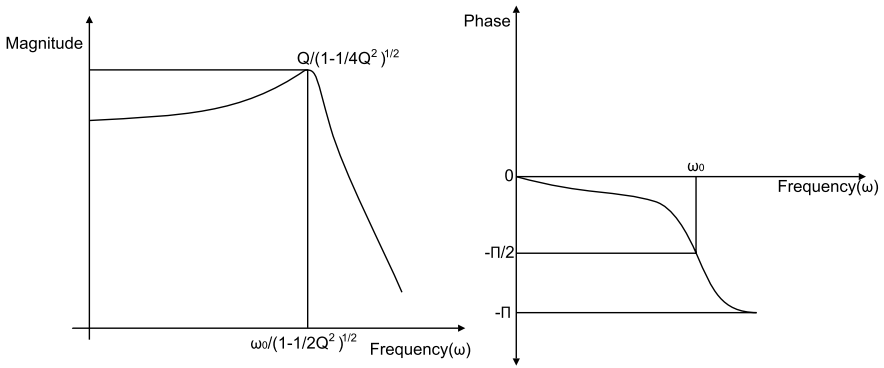


Figure 1.3: Magnitude and Phase response of a Unity Gain System

and

$$\omega_0 = \sqrt{GB \cdot \omega_{d2}}$$

Q is the quality factor and $\xi = \frac{1}{2Q}$ is the damping factor, and ω_0 is the natural frequency of the system. When the frequency response is plotted with magnitude vs ω/ω_0 and phase vs ω/ω_0, it appears as shown in Figure 1.3.

If one applies a step of peak voltage V_p to the unity gain amplifier, and if $V_p \cdot GB <$ slew rate, then the output appears as shown in Figure 2.4 if $Q > \frac{1}{2}$ or $\xi < 1$.

Q is approximately equal to the total number of visible peaks in the step response and the frequency of ringing is $\frac{\omega_0}{(1-1/4Q^2)}$.

Slew-rate is known as the maximum rate at which the output of the OP-Amps is capable of rising; in other words, slew rate is the maximum value that dVo/dt can attain. In this experiment, as we go on increasing the amplitude of the step input, at some amplitude the rate at which the output starts rising remains constant and no longer increases with the peak voltage of input; this rate is called slew rate. It can therefore be determined by applying a square wave of Vp at certain high frequency and increasing the magnitude of the input.

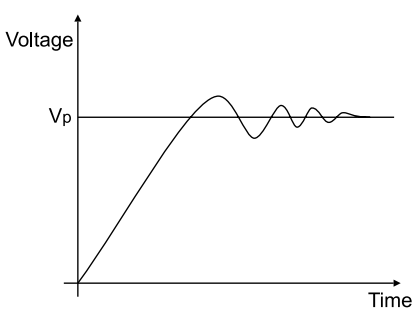


Figure 1.4: Time Response of an Amplifier for a step input of size Vp

Figure 1.5: (a) Non-inverting amplifier of gain 2, (b) Inverting amplifier of gain 2

1.1.2 Non-inverting Amplifier

A non-inverting amplifier with a gain of 2 is shown in Figure 1.5 (a).

1.1.3 Inverting Amplifier

An inverting amplifier with a gain of 2 is shown in Figure 1.5 (b).

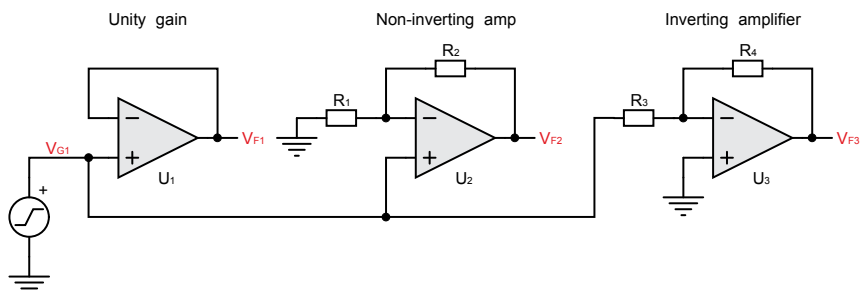


Figure 1.6: Negative Feedback Amplifiers

Figure 1.6 shows all the three negative feedback amplifier configurations. Figure 1.7 illustrates the frequency response (magnitude and phase) of the three different negative feedback amplifier topologies. Figure 1.8 shows the output of the three types of amplifiers for a square-wave input, illustrating the limitations due to slew-rate.

1.2 Exercise Set 1

1. Design the following amplifiers - (a) a unity gain amplifier, (b) a non-inverting amplifier with a gain of 2 (Figure 1.5(a)) and an inverting amplifier with the gain of 2.2 (Figure 1.5(b)).

2. Design an instrumentation amplifier using three OP-Amps with a controllable differential-mode gain of 3. Refer to Figure 1.9(a) for the circuit diagram. Assume that the resistors have 1% tolerance and determine the Common Mode Rejection Ratio (CMRR) of the setup and estimate its bandwidth. We invite the reader to view the recorded lecture **[18]**.

3. Design an instrumentation amplifier using two OP-Amps with a controllable differential-mode gain of 5. Refer to Figure 1.9 for the circuit diagrams of the instrumentation amplifiers and determine the values of the resistors. Assume that the resistors have 1% tolerance and determine the CMRR of the setup and estimate its bandwidth.

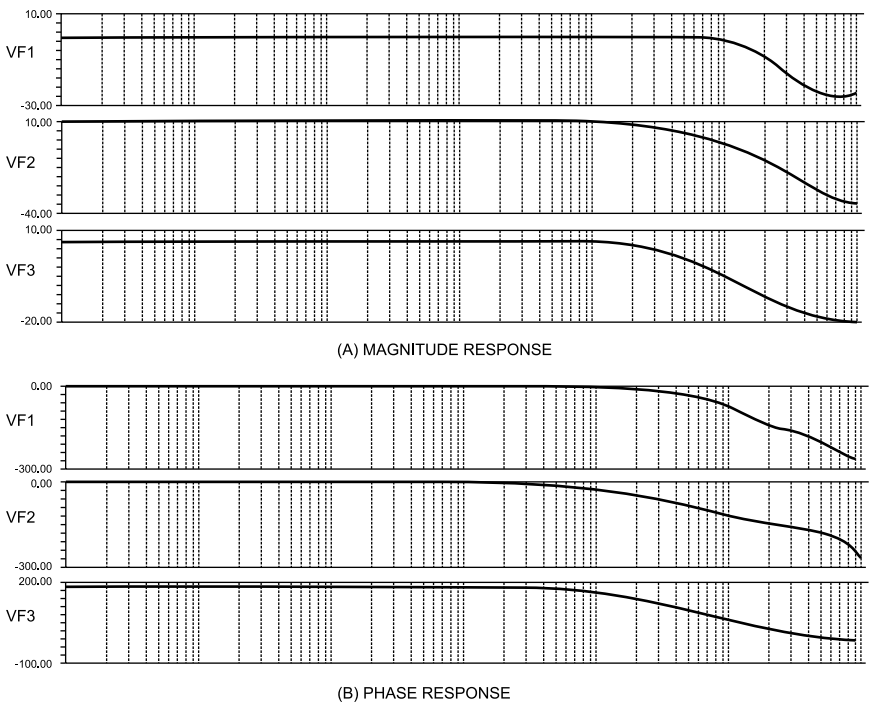


Figure 1.7: Frequency Response of Negative Feedback Amplifiers

1.3 Measurements to be taken

1. Transient response - Apply a square wave of fixed magnitude and study the effect of slew rate on unity gain, inverting and non-inverting amplifiers.

2. Frequency Response - Obtain the gain bandwidth product of the unity gain amplifier, the inverting amplifier and the non-inverting amplifier from the frequency response.

3. DC Transfer Characteristics - Study the saturation limits for an OP-Amp.

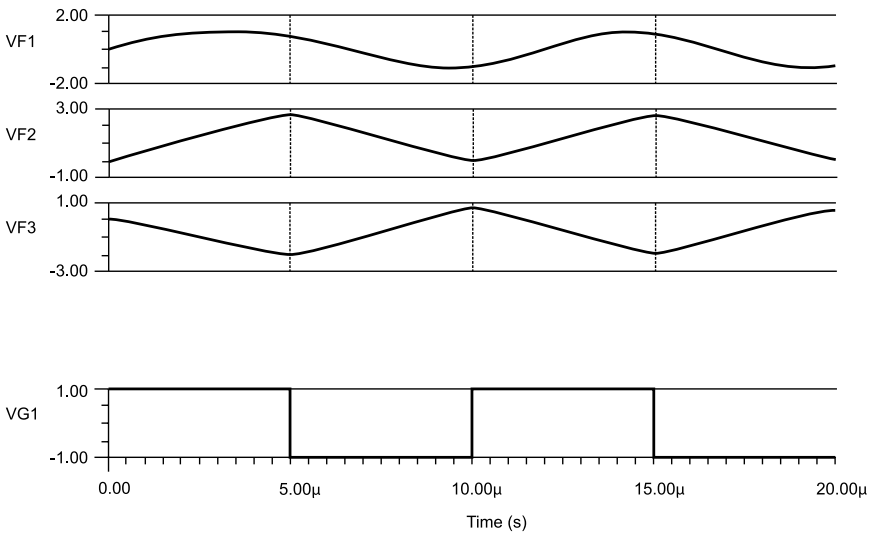


Figure 1.8: Outputs VF1, VF2 and VF3 of Negative Feedback Amplifiers of Figure 1.6 for Square-wave Input VG1

4. Determine the second pole of an OP-Amp and develop the macromodel for the given OP-Amp IC TL082. See Appendix B for an introduction to the topic of analog macromodels.

1.4 What should you submit

1. Submit the simulation results for Transient response, Frequency response and DC transfer characteristics.

2. Take the plots of Transient response, Frequency response and DC transfer characteristics from the oscilloscope and compare it with your simulation results.

3. Apply square wave of amplitude 1V at the input. Change the input frequency and study the peak to peak amplitude of the output. Take the readings in Table 1.1 and compute the slew-rate.

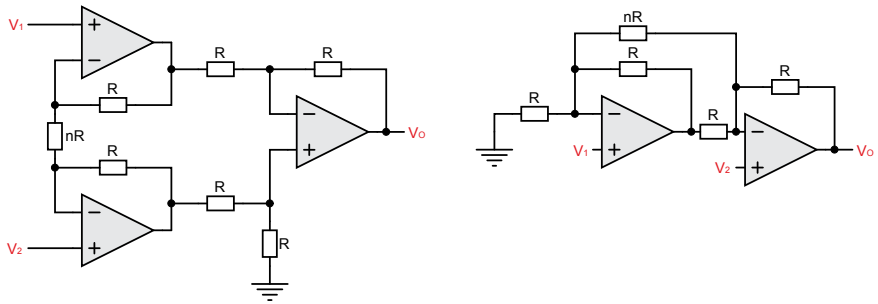


Figure 1.9: Instrumentation Amplifiers with (a) three and (b) two operational amplifiers

S. No.	Input Frequency	Peak to Peak Amplitude of output (Vpp)
1		
2		
3		
4		

Table 1.1: Plot of Peak to Peak amplitude of output Vpp w.r.t. Input frequency

4. Frequency Response - Apply sine wave input to the system and study the magnitude and phase response. Take your readings in Table 1.2.

5. DC transfer Characteristics - Vary the DC input voltage and study its effect on the output voltage. Take your readings in Table 1.3.

1.5 Other related ICs

Specific ICs from Texas Instruments which can be used as instrumentation Amplifiers are INA114, INA118 and INA128. Additional ICs from Texas Instruments which can be used as general purpose OP-Amps are OPA703, OPA357, etc. See CHAPTER 2, EXPERIMENT 1.

S. No.	Input Frequency	Magnitude Variation	Phase Variation
1			
2			
3			
4			

Table 1.2: Plot of Magnitude and Phase variation w.r.t. Input Frequency

S. No.	DC Input Voltage	DC Output Voltage	Phase Variation
1			
2			
3			
4			

Table 1.3: Plot of DC output voltage and phase variation w.r.t. DC input voltage

Further Reading

Datasheets of all these ICs are available at http://www.ti.com.
An excellent reference about operational amplifiers is the "Handbook of Operational Amplifier Applications" by Carter and Brown **[5]**.

Notes on Experiment 1:

Chapter 2

Experiment 2

Study the characteristics of regenerative feedback system with extension to design an astable and monostable multivibrator

Goal of the experiment

The goal of this experiment is to understand the basics of hysteresis and the need of hysteresis in the switching circuits.

2.1 Brief theory and motivation

2.1.1 Inverting Regenerative Comparator

In the earlier experiment we had discussed the use of only negative feedback. Let us now introduce the case of regenerative positive feedback as shown in Figure 2.1. The reader will benefit by listening to the recorded lecture at **[20]**.

$$V_0 = -A_0 \cdot (V_i - \beta V_0) \tag{2.1}$$

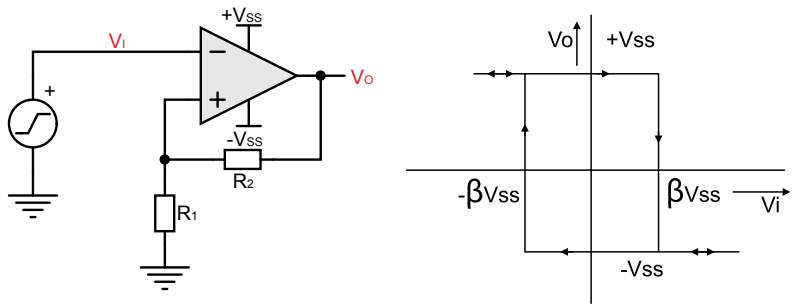


Figure 2.1: Inverting Schmitt-Trigger and its Hysteresis Characteristic

$$\frac{V_0}{V_i} = -A_0 \cdot \frac{1}{1 - A_0 \cdot \beta} \tag{2.2}$$

$$\beta = \frac{R_1}{R_1 + R_2} \tag{2.3}$$

However, when $|A_0 \cdot \beta| = 1$, it becomes unstable as amplifier as output saturates. When $|A_0 \cdot \beta| \gg 1$ the region of operation of this circuit is regenerative comparator. This is the mixed-mode circuit. Output is stable only in two stages $+V_{ss}$ and $-V_{ss}$. When the input is large negative value output saturates at $+V_{ss}$ as input in increased output remain at $+V_{ss}$ until input reaches $\beta \cdot V_{ss}$ at this point it changes to stable state V_{ss}. Now when the input is decreased it can change state only at V_{ss}. Thus hysteresis of $2 \cdot \beta \cdot V_{ss}$ is seen around 0. This kind of comparator is a must while driving a MOSFET as a switch in ON-OFF controllers SMPS (Switched Mode Power Supply), pulse width modulators and class-D audio power amplifiers. The symbol for this inverting type Schmitt trigger is shown in Figure 2.2. The non-inverting Schmitt trigger is as shown in Figure 2.3.

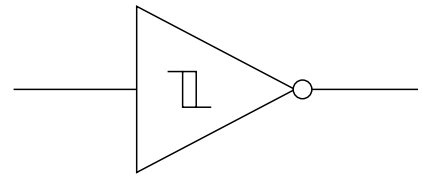


Figure 2.2: Symbol for an Inverting Schmitt Trigger

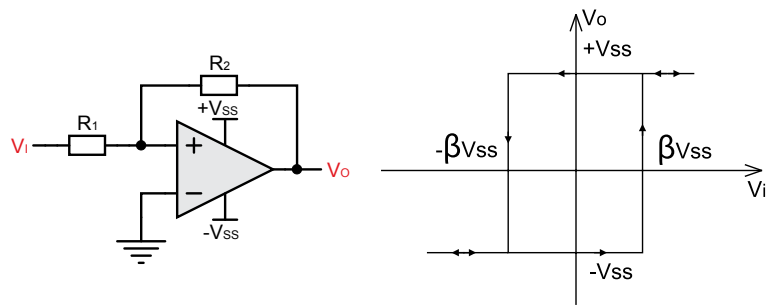


Figure 2.3: Non-inverting Schmitt Trigger and its Hysteresis Curve

2.1.2 Astable Multivibrator

An astable multivibrator is shown in Figure 2.4. The square and the triangular waveforms shown in the figure are both generated using the astable multivibrator. We refer to β as the regenerative feedback. The time period of the multivibrator is given by

$$T = 2 \cdot RC \cdot \ln\left(\frac{1+\beta}{1-\beta}\right) \tag{2.4}$$

2.1.3 Monostable Multivibrator (Timer)

The circuit diagram for a monostable multivibrator is shown in 2.6. The trigger waveform shown in Figure 2.5 is applied to the monostable. The negative edge triggers the monostable, which produces the square waveform shown in Figure 2.6.

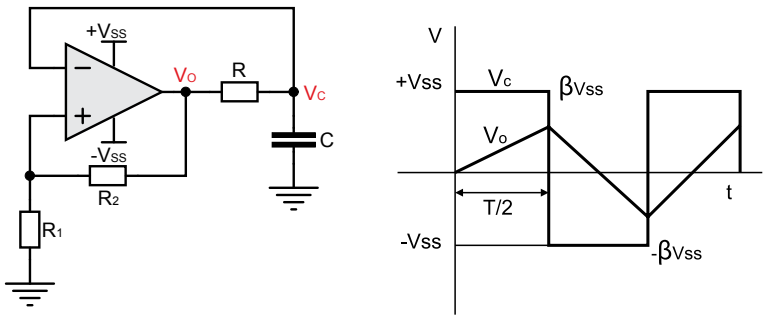


Figure 2.4: Astable Multivibrator and its characteristics

The monostable remains in the "on" state until it is triggered; at this time, the circuit switches to the "off" state for a period equal to τ. The equation for τ is shown below.

$$\tau = RC \cdot \ln\left(\frac{1}{1-\beta}\right) \qquad (2.5)$$

After triggering the monostable at time t, the next trigger pulse must be applied after $t + \tau'$. The formula for τ' is given below.

$$\tau' = RC \cdot \ln\left(\frac{1+\beta}{\beta}\right)$$

S. No.	Regenerative Feedback	Hysteresis
1		
2		
3		
4		

Table 2.1: Plot of Hysteresis w.r.t. Regenerative Feedback

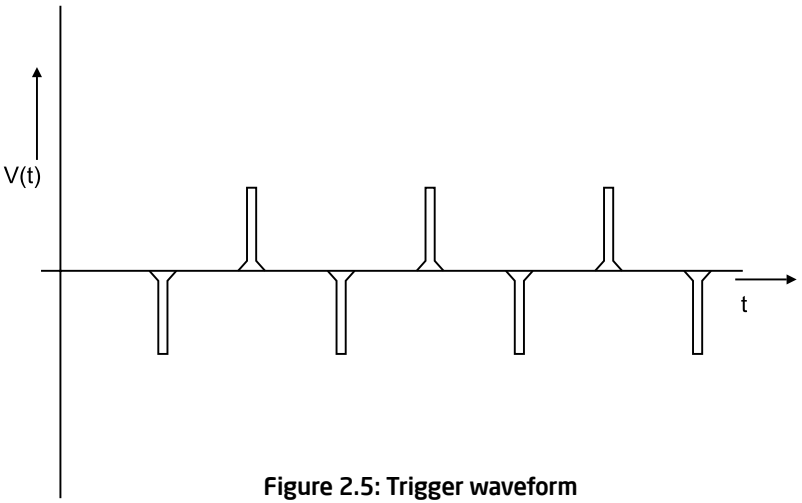
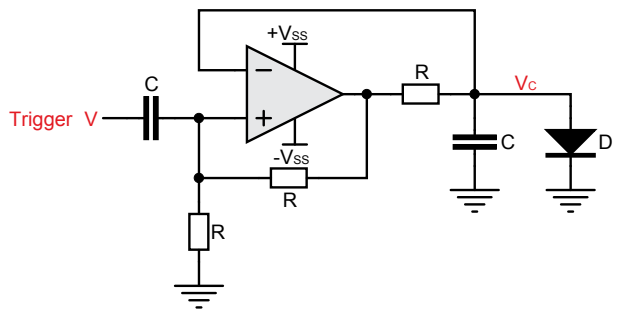


Figure 2.5: Trigger waveform



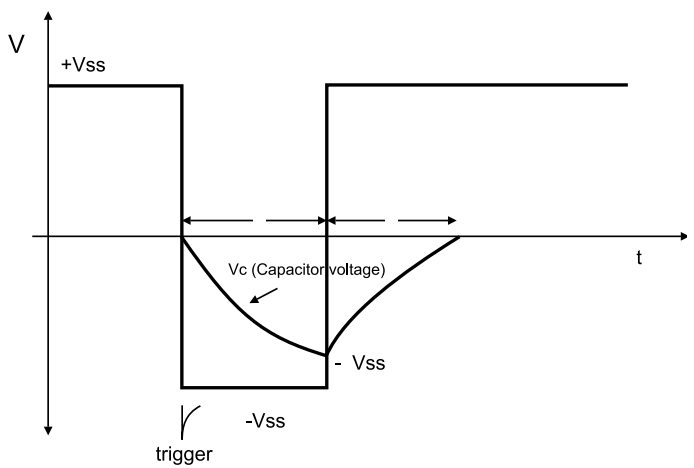


Figure 2.6: Monostable Multivibrator and its outputs

2.2 Exercise Set 2

1. Design a regenerative feedback circuit with the hysteresis of $\pm 1V$. Obtain the DC transfer characteristics of the system. Estimate the hysteresis and see how it can be controlled by varying the regenerative feedback $\beta = \frac{R_1}{R_1 + R_2}$.

2. Vary either R_1 or R_2 in order to vary β. Apply the triangular waveform with the peak voltage of 10V at a given frequency to both circuits and observe the output waveform.

   a) Submit the simulation results for DC transfer characteristics.

   b) Take the plots of DC transfer characteristics from oscilloscope and compare it with simulation results.

   c) Vary the regenerative feedback and see the variation in the hysteresis, hysteresis is directly proportional to regenerative feedback.

3. Design an astable multivibrator using charging and discharging of capacitor C through resistance R between input and output of the Schmitt trigger. See Figure 2.4. Assume that frequency $f = \frac{1}{T} = 1{,}5\,kHz$.

   Design a monostable multivibrator for $\tau = 4\,ms$ and estimate RC using the formula 2.5.

Notes on Experiment 2:

Chapter 3

Experiment 3

Study the characteristics of integrators and differentiator circuits

Goal of the experiment

The goal of the experiment is to understand the advantages and disadvantages of using integrators or differentiators as a building block in solving N^{th} order differential equations or building an N^{th} order filter.

3.1 Brief theory and motivation

Integrators and differentiators can be used as a building block for filters. Filters form the essential block in analog signal processing to improve signal to noise ratio. An OP-Amp can be used to construct an integrator or a differentiator. This experiment is to understand the advantage of integrators as building blocks instead of differentiators. Differentiators are rejected because of their poor high-frequency noise response.

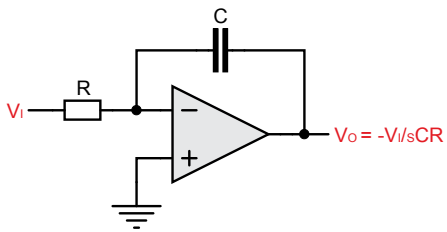


Figure 3.1: Integrator

3.1.1 Integrators

An integrator circuit that uses an OP-Amp is shown in Figure 3.1.
Assuming $A = GB/s$,

$$\frac{V_0}{V_i} = \frac{-\frac{1}{sCR}}{\left(1 + \frac{1}{GB \cdot RC} + \frac{s}{GB}\right)}$$

The output goes to saturation in practice. For making it work a high valued resistance across C must be added in order to bring the OP-Amp to the active region where it can act as an integrator.

3.1.2 Differentiators

A differentiator circuit that uses an OP-Amp is shown in Figure 3.2.

$$\frac{V_0}{V_i} = \frac{-sRC}{\left(1 + \frac{s}{GB} + \frac{s^2 \cdot RC}{GB}\right)} \quad (3.1)$$

$$= \frac{-sRC}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)} \quad (3.2)$$

The output of the differentiator remains at input offset (approximately 0). However, any sudden disturbance at the input causes it to ring at natural frequency ω_0.

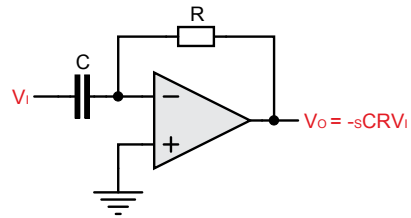


Figure 3.2: Differentiator

3.2 Specifications

Fix the RC time constant of the integrator or differentiator so that the phase shift and magnitude variation of the ideal block remains unaffected by the active device parameters.

3.3 Measurements to be taken

1. Transient Response - Apply the step input and square wave input to the integrator and study the output response. Apply the triangular and square input to the differentiator and study the output response.

2. Frequency Response - Apply the sine wave input and study the phase error and magnitude error for integrator and differentiator.

3.4 What should you submit

1. Simulate the integrator and differentiator and obtain the transient response and phase response.

2. Take the plots of transient response and phase response on an oscilloscope and compare it with simulation results.

S. No.	Input Frequency	Magnitude	Phase
1			
2			
3			
4			
5			

Table 3.1: Plot of Magnitude and Phase w.r.t. Input Frequency

S. No.	Input Frequency	Magnitude	Phase
1			
2			
3			
4			
5			

Table 3.2: Plot of Magnitude and Phase w.r.t. Input Frequency

3. Frequency Response - Apply a sine wave to the integrator (similarly to the differentiator) and vary the input frequency to obtain phase and magnitude error. Prepare a Table of the form 3.1. Figure 3.3 shows the typical frequency response for integrators and differentiators. For an integrator, the plot shows a phase lag which is proportional to ω/GB. The magnitude decreases with increasing frequency. For the differentiator, the phase will change rapidly at natural frequency in direct proportion to quality factor. The magnitude peaks at natural frequency and is directly proportional to the quality factor.

4. Transient response - Apply the square wave as an input to integrator, vary the peak amplitude of the square wave and obtain the peak to peak value of output wave. V_{pp} is directly proportional to peak voltage of input V_p and is given by $V_{pp} = \frac{V_p \cdot T}{2 \cdot RC}$, where $T = 1/f$, f being the input frequency.

Figure 3.4 shows sample output waveforms obtained through simulation.

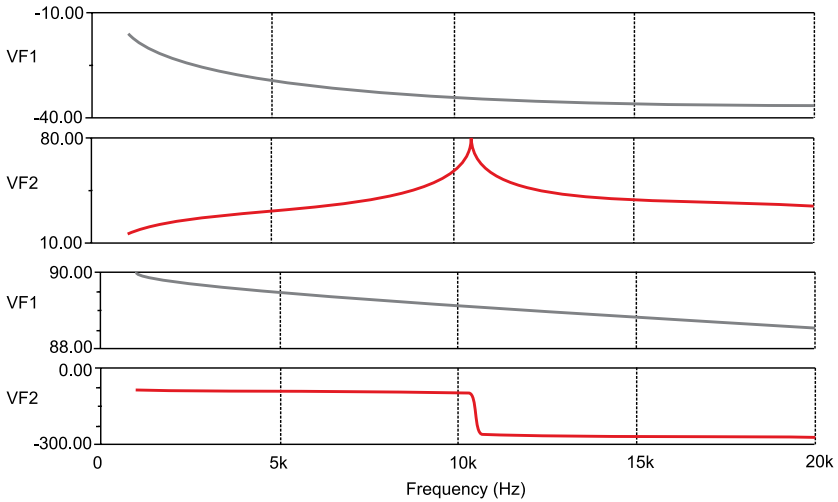
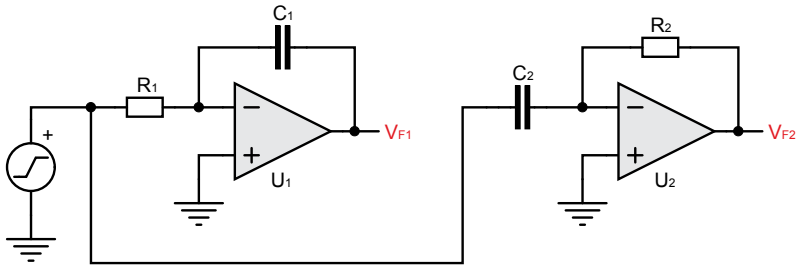
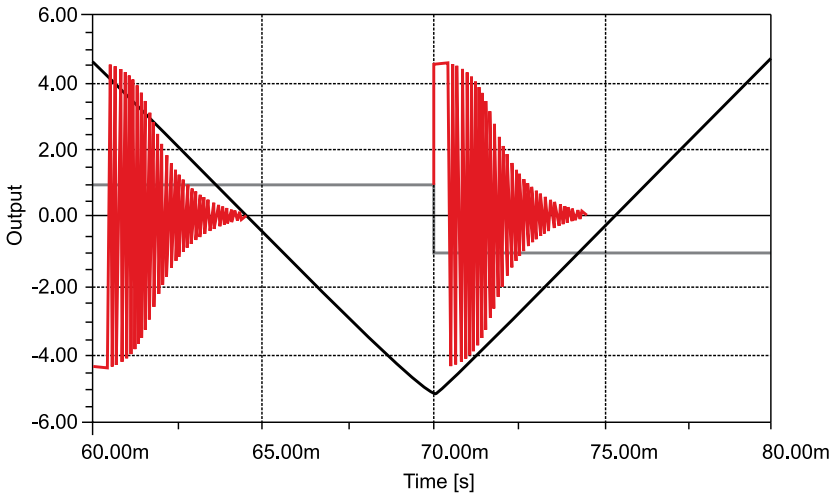


Figure 3.3: Frequency Response of integrator and differentiator

S. No.	Peak Value of input Vp	Peak to Peak value of output
1		
2		
3		
4		

Table 3.3: Variation of Peak to Peak value of output w.r.t. Peak value of Input





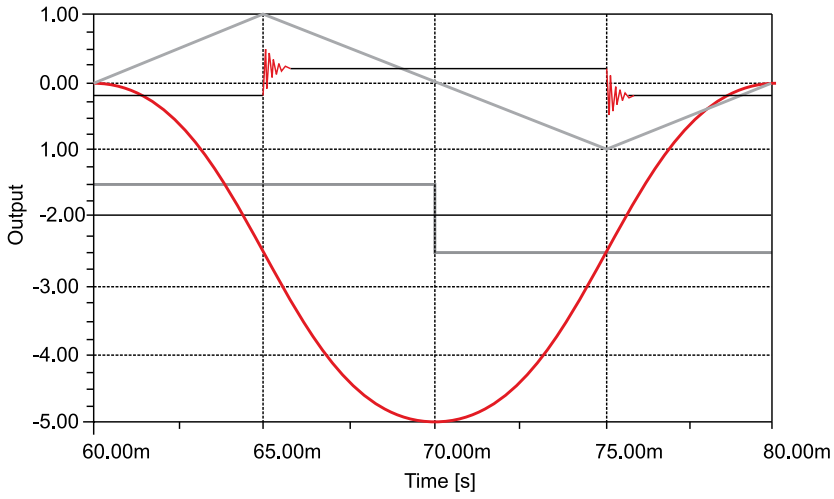


Figure 3.4: Outputs of integrator and differentiator for square-wave and triangular-wave inputs

3.5 Exercise Set 3 - Grounded Capacitor Topologies of Integrator and Differentiator

Determine the function of the circuits shown in Figure 3.5. What are the advantages and disadvantages of these circuits when compared to their conventional counterparts?

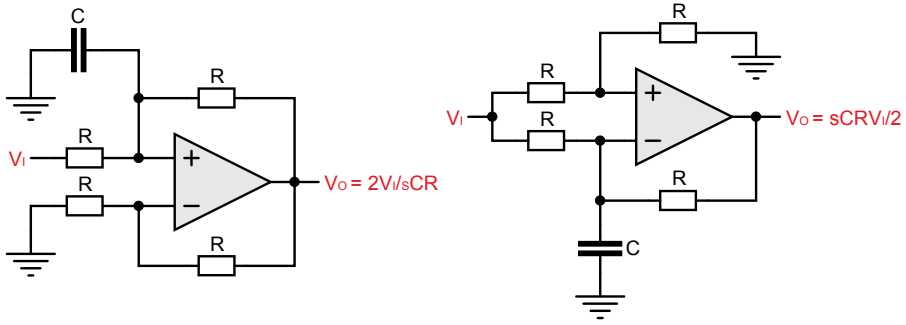


Figure 3.5: Circuit for Exercise 3

Notes on Experiment 3:

Chapter 4

Experiment 4

Design of Analog Filters

Goal of the experiment

To understand the working of four types of second order filters, namely, Low Pass, High Pass, Band Pass, and Band Stop filters, and study their frequency characteristics (phase and magnitude).

4.1 Brief theory and motivation

Second order filters (or biquard filters) are important since they are the building blocks in the construction of N^{th} order filters, for $N > 2$. When N is odd, the N^{th} order filter can be realized using $\frac{N-1}{2}$ second order filters and one first order filter. When N is even, we need $N-1$ second order filters. Please listen to the recorded lecture at **[19]** for a detailed explanation of active filters.

Second order filter can be used to construct four different types of filters. The transfer functions for the different filter types are shown in Table 4.1, where $\omega_0 = 1/RC$ and H_0 is the low frequency gain of the transfer function. The filter names are often abbreviated as LPF (Low-pass Filter), HPF (High-pass Filter), BPF (Band Pass Filter), and BSF (Band Stop Filter). In this experiment, we will describe a universal active filter, which provides all the four filter functionalities. Figure 4.1 shows a second order universal filter realized using two integrators. Note that there are different outputs of the circuit that realize LPF, HPF, BPF and BSF functions.

Low Pass Filter	$\frac{V_{03}}{V_i} = \frac{+H_0}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)}$
High Pass Filter	$\frac{V_{01}}{V_i} = \frac{\left(H_0 \cdot \frac{s^2}{\omega_0^2}\right)}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)}$
Band Pass Filter	$\frac{V_{02}}{V_i} = \frac{\left(-H_0 \cdot \frac{s}{\omega_0}\right)}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)}$
Band Stop Filter	$\frac{V_{04}}{V_i} = \frac{\left(1 + \frac{s^2}{\omega_0^2}\right) \cdot H_0}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)}$

Table 4.1: Transfer functions of Active Filters

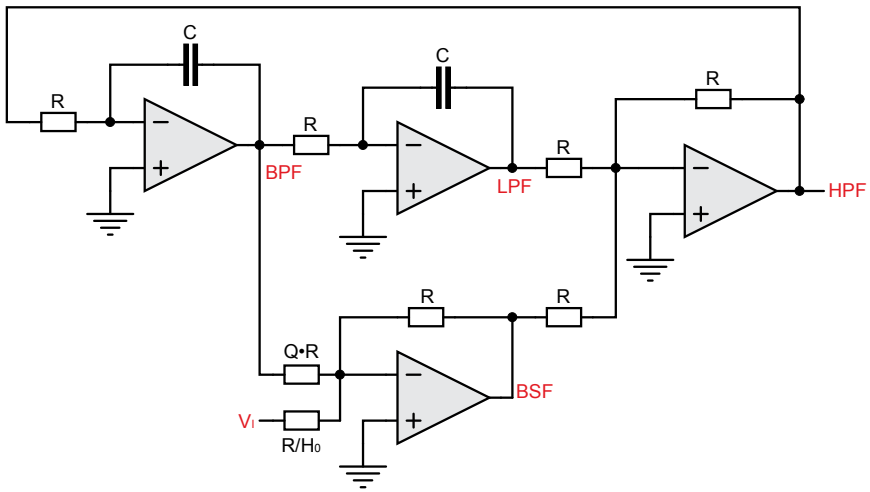


Figure 4.1: A Second-order Universal Active Filter

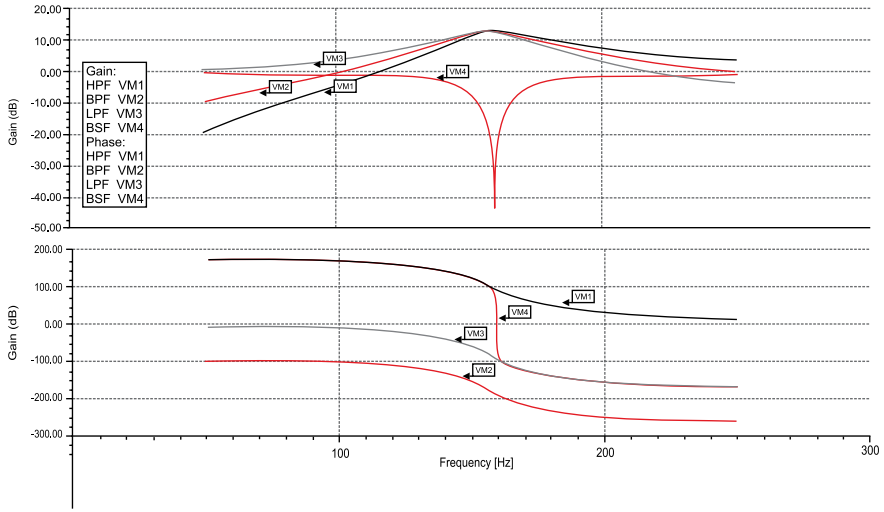


Figure 4.2: Magnitude and Phase response of LPF, BPF, BSF, and HPF filters

Frequency Response of Filters

The magnitude and phase response of LPF, BPF, BSF, and HPF filters are shown in Figure 4.2. Note that the low-pass filter frequency response peaks at $\omega = \omega_0\sqrt{1-\frac{1}{2Q^2}}$ and has a value equal to $\frac{H_0 Q}{\sqrt{1-\frac{1}{4Q^2}}}$. The phase sensitivity $\frac{\delta\phi}{\delta\omega}$ is maximum at $\omega = \omega_0$ and is given by $\frac{-2Q}{\omega_0}$. This information about phase variation can be used to tune the filter to a desired frequency ω_0. This is demonstrated in the next experiment.

For the bandpass filter, the magnitude response peaks at $\omega = \omega_0$ and is given by $H_0 Q$. The bandstop filter shows a null magnitude response at $\omega = \omega_0$.

4.2 Specification

Design a Band Pass and a Band Stop filter. For the BPF, assume $\omega_0 = 1\,kHz$ and $Q = 1$. For the BSF, assume $\omega_0 = 10\,kHz$ and $Q = 10$.

4.3 Measurements to be taken

1. Steady State Response - Apply a square wave input (Try $f = 1\,kHz$ and $f = 10\,kHz$ to both BPF and BSF circuits and observe the outputs.
   - Band Pass output will output the fundamental frequency of the square wave multiplied by the gain at the centre frequency. The amplitude at this frequency is given by $\frac{4 \cdot V_p}{\pi \cdot H_0 \cdot Q}$, where V_p is the peak amplitude of the input square wave.
   - The Band Stop filter's output will carry all the harmonics of the square wave, other than fundamental. This illustrates the application of BSF as a distortion analyzer.
2. Frequency Response - Apply the sine wave input and obtain the magnitude and the phase response.

4.4 What you should submit

1. Simulate the circuits and obtain the Steady-State response and Frequency response.
2. Take the plots of the Steady-State response and Frequency response from the oscilloscope and compare it with simulation results.
3. Frequency Response - Apply a sine wave input and vary its input frequency to obtain the phase and magnitude error. Use Table 4.2 and 4.3 to note your readings. The nature of graphs should be as shown above.

		Band Pass		Band Stop	
S.No.	**Input Frequency**	**Phase**	**Magnitude**	**Phase**	**Magnitude**
1					
2					
3					
4					

Table 4-2: Frequency Response of a BPF with $\omega_0 = 1\,kHz$, $Q = 1$

		Band Pass		Band Stop	
S.No.	**Input Frequency**	**Phase**	**Magnitude**	**Phase**	**Magnitude**
1					
2					
3					
4					

Table 4-3: Frequency Response of a BSF with $\omega_0 = 10\,kHz$, $Q = 10$

4.5 Exercise Set 4

1. Higher order filters are normally designed by cascading second order filters and, if needed, one first- order filter. Design a third order Butterworth Lowpass Filter using FilterPro and obtain the frequency response as well as the transient response of the filter. The specifications are bandwidth of the filter $\omega_0 = 2 \cdot \pi \cdot 10^4\, rad/s$ and $H_0 = 10$.

2. Design a notch filter (band-stop filter) to eliminate the $50Hz$ power life frequency. In order to test this circuit, synthesize a waveform $v(t) = \sin(100\pi t) + 0.1\sin(200\pi t)$ Volts and use it as the input to the filter. What output did you obtain?

Related Circuits

The circuit described in Figure 4.1 is a universal active filter circuit. While this circuit can be built with OP-Amps, a specialized IC called UAF42 from Texas Instruments provides the functionality of the Universal Active Filter. We encourage you to use this circuit and understand its function.

Datasheet of UAF42 is available from http://www.ti.com.
Also refer to the application notes **[7]**, **[11]**, *and* **[12]**.

Notes on Experiment 4:

Chapter 5

Experiment 5

Design of a self-tuned filter

Goal of the experiment

The goal of this experiment is to learn the concept of tuning a filter. The idea is to adjust the RC time constants of the filter so that in phase response of a lowpass filter, the output phase w.r.t. input is exactly 90º at the incoming frequency. This principle is utilized in distortion analyzers and spectrum analyzers, such self tuned filters are used to lock on to the fundamental frequency and harmonics of the input.

5.1 Brief theory and motivation

In order to design self-tuned filters and other analog systems in subsequent experiments, we need to introduce one more building block, the Analog multiplier. The reader will benefit from viewing the recorded lecture at **[21]**. In ASLK PRO, we have used to MPY634 analog multiplier from Texas Instruments. Refer to Figure 5.1, which shows the symbol of an analog multiplier.

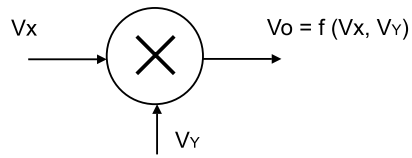


Figure 5.1: Analog Multiplier

$$V_0 = V_{offset} + K_x \times V_x + K_y \times V_y + K_0 \times V_x \times V_y + \xi \quad (5.1)$$

where ξ is a non-linear term in V_x and V_y. For a precision multiplier, $V_r \leq V_x$ and $V_y \leq V_r$, where V_r is the reference voltage of the multiplier. Hence, for precision amplifiers, $V_0 = V_x \times V_y / V_r$.

In Experiment 4, if we replace the integrator with a multiplier followed by integrator, then the circuit becomes a Voltage Controlled Filter (or a Voltage Controlled Phase Generator). This forms the basic circuit for self-tuned filter. See Figure 5.2. The output of the self-tuned filter for a square-wave input, including the control voltage waveform, is shown in Figure 5.3. The figure brings out the aspect of automatic control and self-tuning.

5.1.1 Multiplier as a Phase Detector

In the circuit of Figure 5.1, the output of the multiplier is

$$V_0 = \frac{V_p V_p'}{2V_r} \cdot \left[\cos\phi - \cos(\omega t + \phi)\right] \quad (5.2)$$

After passing through the low-pass filter, the high frequency component gets filtered out and only the average value of output V_{av} remains.

$$V_0 = \frac{V_p V_p'}{2V_r} \cos\phi \quad (5.3)$$

$$K_{pd} = \frac{dV_{av}}{d\phi} \quad (5.4)$$

K_{pd} is called the sensitivity of the phase detector and is measured in Volts/radians.

For $\phi = 90^\circ$, V_{av} becomes 0. This information is used to tune the voltage controlled filter (VCF) automatically. The voltage-controlled filter, along with phase detector, is called a self-tuned filter. See Figure 5.2. ω_0 of the VCF is given by

$$\omega_0 = \frac{V_c}{V_r \cdot RC}$$

Therefore,

$$\frac{d\omega_0}{dV_c} = \frac{1}{V_r RC} = \frac{\omega_0}{V_c}$$

The sensitivity of VCF is $\frac{d\phi}{dV_c}$ radians/sec/Volts. Now

$$\frac{d\phi}{dV_c} = \frac{d\phi}{d\omega_0} \cdot \frac{d\omega_0}{dV_c}$$

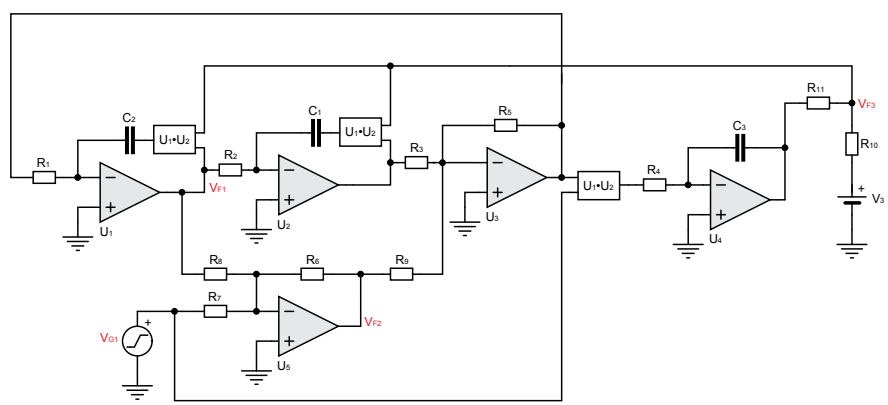


Figure 5.2: A Self-Tuned Filter based on a Voltage Controlled Filter or Voltage Controlled Phase Generator

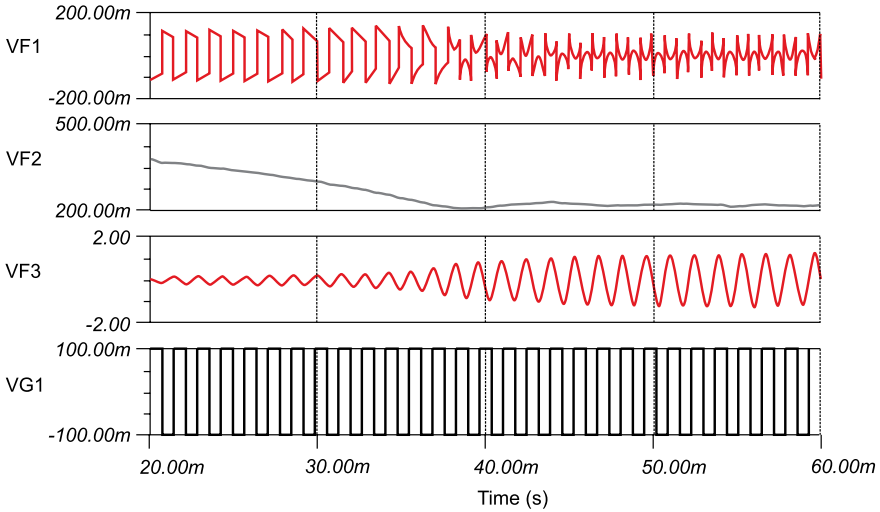


Figure 5.3: Output of the Self-Tuned Filter based on simulation

If we consider the low-pass output, then

$$\frac{V_0}{V_i} = \frac{+H_0}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)}$$

$$\phi = \tan^{-1} \frac{\left(\frac{\omega_r}{\omega_0 Q}\right)}{\left(1 - \left(\frac{\omega_r^2}{\omega_0}\right)\right)}$$

then

$$\frac{d\phi}{d\omega_0} = -2Q/\omega_0$$

Hence, sensitivity of VCF(KVCF) is equal to $\frac{d\phi}{dV_c} = -2Q/V_c$.

For varying input frequency the output phase will always lock to the input phase with 90˚ phase difference between the two if $V_{av} = 0$.

Input voltage =		
S.No.	**Input Frequency**	**Output Amplitude**
1		
2		
3		
4		

Table 5.1: Variation of output amplitude with input frequency

5.2 Specification

Assume that the input frequency is $1\,kHz$ and design a high-Q Band pass filter whose centre frequency gets tuned to $1\,kHz$.

5.3 Measurements to be taken

5.3.1 Transient response

Apply a square wave input and observe the amplitude of the Band Pass output for fundamental and its harmonics.

5.4 What should you submit

1. Simulate the circuits and obtain the transient response of the system.
2. Take the plots of transient response from oscilloscope and compare it with simulation results.
3. Measure the output amplitude of the fundamental (Band Pass output) at varying input frequency at fixed input amplitude.

   Output amplitude should remain constant for varying input frequency within the lock range of the system.

5.4.1 Exercise Set 5

1. Determine the lock range of the self-tuned filter you designed. The lock range is defined as the range of input frequencies where the amplitude of the output voltage remains constant at $H_0 \cdot Q \cdot V_i$

Related Circuits

Texas Instruments also manufactures the following related ICs - Voltage-controlled amplifiers (e.g. VCA820) and multiplying DAC (e.g. DAC7821).

Refer to http://www.ti.com for application notes.

Notes on Experiment 5:

Chapter 6

Experiment 6

Design a function generator and convert it to Voltage-Controlled Oscillator/FM Generator

Goal of the experiment

To understand a classic mixed mode circuit that uses two-bit A to D Converter along with an analog integrator block. The architecture of the circuit is similar to that of a sigma delta converter.

6.1 Brief theory and motivation

The feedback loop is made up of a two-bit A/D converter (at $\pm V_{ss}$ levels), also called Schmitt trigger, and an integrator. The circuit is also known as a function generator and is shown in Figure 6.1. The output of the function generator is shown in Figure 6.2.

The function generator produces a square wave at the Schmitt Trigger output and a triangular wave at the integrator output with the frequency of oscillation equal to $f = (1/4RC)\cdot(R_2/R_1)$. The function generator circuit can be converted as a linear VCO by using the multiplier integrator combination as shown in Figure 6.3.

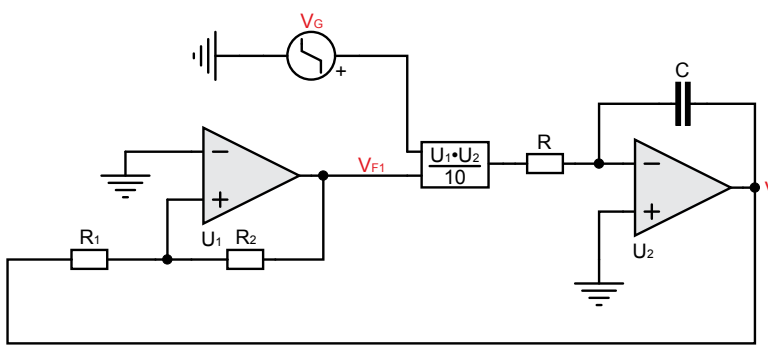


Figure 6.1: Function Generator

The frequency of oscillation of the VCO becomes

$$f' = \frac{V_c \cdot R_2}{4 \cdot RC \cdot V_r \cdot R_1}$$

Sensitivity of the VCO is the important parameter and is given as K_{VCO}, where it is given as

$$K_{VCO} = \frac{df'}{dV_c} = \frac{R_2}{4RC \cdot V_r V_1} = \frac{f}{Vc} Hz/Volts \qquad (6.1)$$

where $f = (1/4RC)\cdot(R_2/R_1)$

VCO is an important analog circuit as it is used in FSK/FM generation and constitutes the modulator part of the MODEM. As a VCO, it can be used in Phase Locked Loop (PLL). It is a basic building block forming sigma delta converter. It can also be used as reference oscillator for a Class D amplifier.

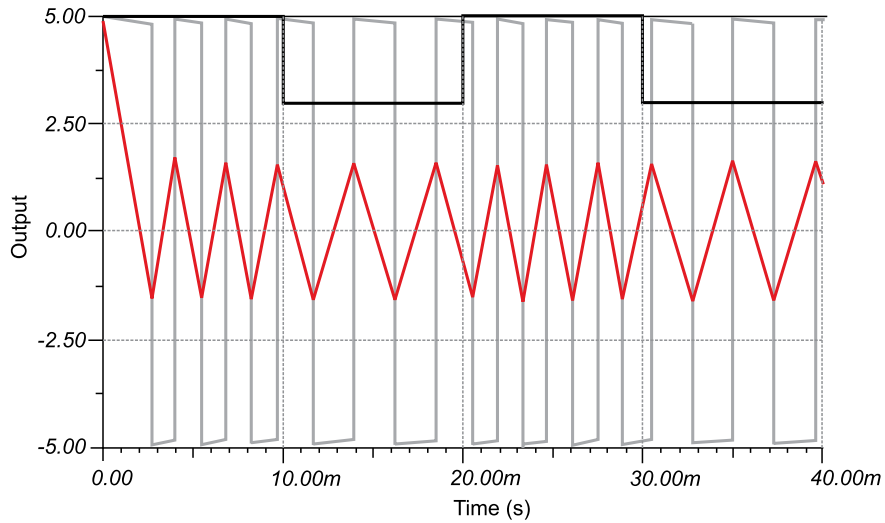


Figure 6.2: Function Generator Output

6.2 Specifications

Design of a function generator which can generate square and triangular wave for a frequency of 1 kHz.

6.3 Measurements to be taken

Determine the frequency of oscillations of square and triangular wave. Frequency of oscillation should be equal to $(1/4RC)\cdot(R_2/R_1)$. Convert the function generator into a Voltage Controlled Oscillator (VCO) or FM/FSK generator also called "mod of modem."

6.4 What should you submit

1. Simulate the circuits and obtain the Transient response of the system.

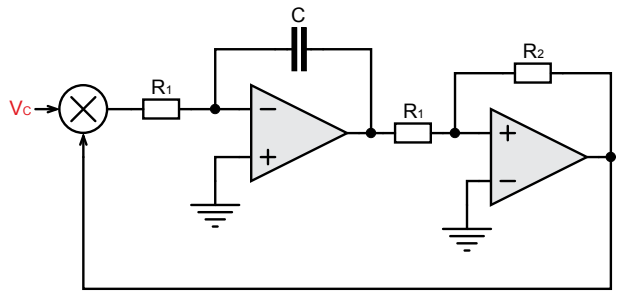


Figure 6.3: Voltage-Controlled Oscillator (VCO)

2. Take the plots of time response from oscilloscope and compare it with simulation results.

3. Vary the control voltage of the VCO and see the effect on the frequency of the output waveform also measure the sensitivity (KVCO) of the VCO which is nothing but $\frac{df}{dV_c}$. Use Table 6.1 to note your readings.

S.No.	Control Voltage (Vc)	Change in Frequency
1		
2		
3		
4		

Table 6.1: Change in frequency as a function of Control Voltage

6.5 Exercise Set 6

Apply 1V, 1kHz square wave over 2V DC and observe the FSK for a VCO which is designed for 10kHz frequency.

Notes on Experiment 6:

Notes on Experiment 6:

Chapter 7

Experiment 7

Design of a Phase Lock Loop (PLL)

Goal of the experiment

The goal of this experiment is to make you aware of the functionality of the Phase Lock Loop commonly referred to as PLL which is primarily used for a frequency synthesizer in high frequency stable clock generators. From a crystal of some kHz range, it is possible to generate waveform of GHz frequency range using a PLL.

7.1 Brief theory and motivation

In the loop of self-tuned filter studied in experiment number 5 if we replace the Voltage Control Filter (VCF) with Voltage Control Oscillator (VCO) (discussed in experiment 6) then it becomes PLL as shown in Figure 7.1. The reader will benefit from viewing the recorded lecture at **[22]**.

The sensitivity of the PLL is given by K_{VCO} and is equal to $\frac{d\omega}{dV_c}$, where $\omega = \frac{V_c}{4V_r \cdot RC}$, frequency of oscillation of VCO. Hence $\frac{d\omega}{dV_c} = \frac{V_c}{V_r \cdot RC}$, which is nothing but ω/V_c

$$K_{VCO} = \omega/V_c \tag{7.1}$$

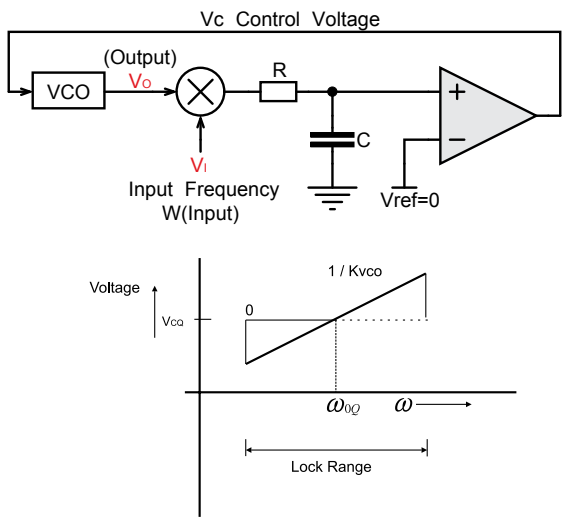


Figure 7.1: Phase Locked Loop (PLL) and its characteristics

When no input voltage is applied to the system, the system oscillates at the free running frequency of the VCO, given by ω_{0Q} with corresponding control voltage of V_{CQ}. If the input is applied to the system with the same frequency as ω_{0Q}, the PLL will continue to run at the free running frequency and the phase difference between the two signals V_0 and V_i as 90˚ since V_{ref} is 0 (already explained in *Experiment 5 of Chapter 6*). As the frequency of input signal is changed, the control voltage will change correspondingly, so as to lock the output frequency to the input frequency. As a result, there is a change of phase difference between the two signals away from 90˚. The range of input frequencies for which output frequencies gets locked to the input is called the lock range of the system. The lock range is defined as $K_{pd} \times \frac{\pi}{2} \times A_0 \times K_{VCO}$ on either side of ω_{0Q}.

7.2 Specifications

Design a PLL to get locked to frequency of 1 kHz.

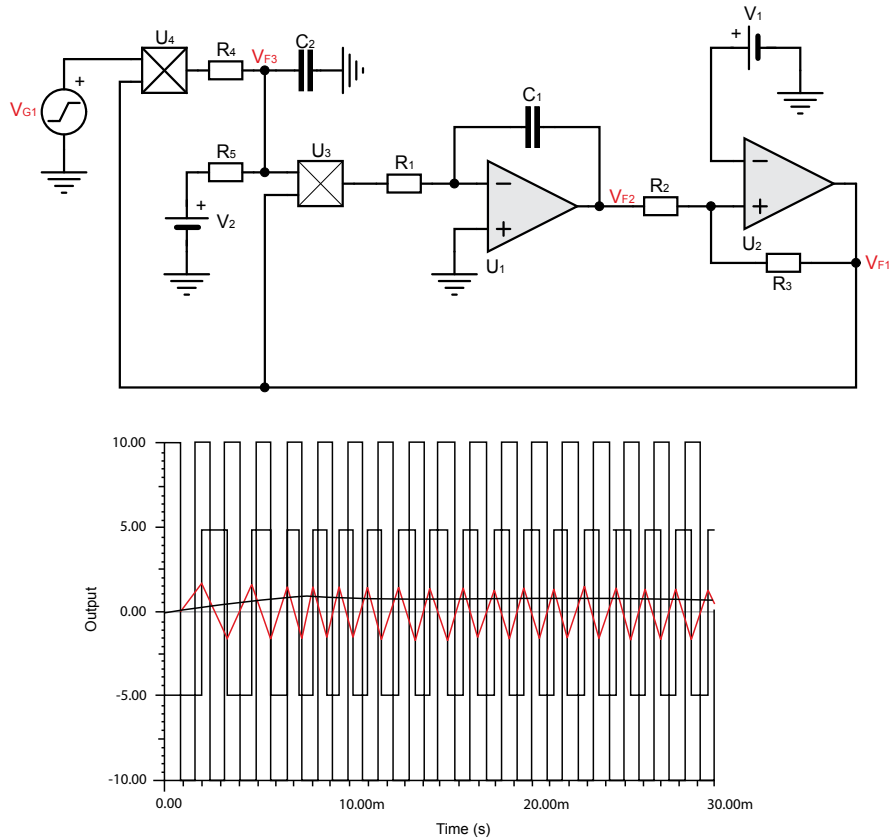


Figure 7.2: Sample output waveform for the Phase Locked Loop (PLL) Experiment

7.3 Measurements to be taken

1. Measure the lock range of the system and measure the change in the phase of the output signal as input frequency is varied within the lock range.
2. Vary the input frequency and obtain the change in the control voltage and plot the output. A sample output characteristic of the PLL is shown in Figure 7.2.

7.4 What you should submit

1. Simulate the circuits and obtain the characteristics of the system.
2. Take the plots of characteristics from oscilloscope and compare it with simulation results.
3. Measure the change in the phase of the output signal as input frequency is varied within the lock range.
4. Vary the input frequency and obtain the change in the control voltage. Use Table 7.2 to record your readings.

S.No.	Input Frequency	Output Phase
1		
2		
3		
4		

Table 7.2: Control Voltage as a function of Input Frequency

S.No.	Input Frequency	Control Voltage
1		
2		
3		
4		

Table 7.1: Output Phase as a function of Input Frequency

7.5 Exercise Set 7

Design a Frequency Synthesizer to generate a waveform of 1MHz frequency from a 100kHz crystal as shown in Figure 7.3.

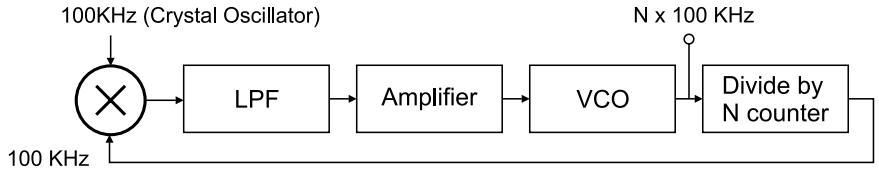


Figure 7.3: Block Diagram of Frequency Optimizer

Notes on Experiment 7:

Notes on Experiment 7:

Chapter 8

Experiment 8

Automatic Gain Control (AGC) Automatic Volume Control (AVC)

Goal of the experiment

In the front-end electronics of a system, we may require that the gain of the amplifier be adjustable, since the amplitude of the input keeps varying. Such a system can be designed using feedback. This experiment demonstrates one such system.

8.1 Brief theory and motivation

The reader will benefit from the recorded lectures at **[25]**. Another useful reference is the application note on Automatic Level Controller for Speech Signals using PID Controllers **[2]**.

In the signal chain of an electronic system, the output of the sensor can vary depending on the strength of the input. To adapt to wide variations in the magnitude of the input, we can design an amplifier whose gain can be adjusted dynamically. This is possible when the input signal has a narrow bandwidth and the control system is called Automatic Gain Control or AGC. Since we may wish to maintain the output voltage of the amplifier at a constant level, we also use the term Automatic Volume Control (AVC). Figure 8.1 shows an AGC circuit. The typical I/O characteristics of AGC/AVC circuit is shown in Figure 8.2. As shown in Figure 8.2, the output value of the system remains constant at $\sqrt{2V_r V_{ref}}$ beyond input voltage $V_{pi} = \sqrt{2V_r V_{ref}}$.

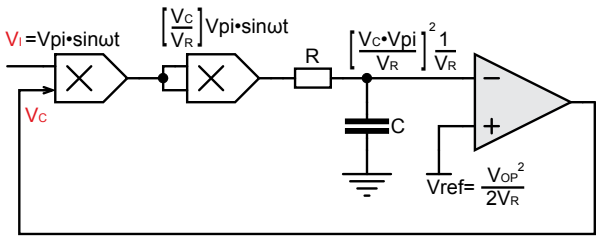


Figure 8.1: Automatic Gain Control (AGC)/Automatic Volume Control (AVC)

8.2 Specification

Design AGC/AVC system to maintain the peak amplitude of the sine wave at 2V.

8.3 Measurements to be taken

Transfer Characteristics - Plot the input versus output characteristics for the AGC/AVC.

8.4 What you should submit

1. Simulate the circuit of Figure 8.1 and obtain the Transfer Characteristic of the system. Assume that the input comes from a function generator; use a sine wave input of a single frequency.

2. Build the circuit shown on Figure 8.1. Plot/print the transfer characteristic using the oscilloscope and compare it with simulation results.

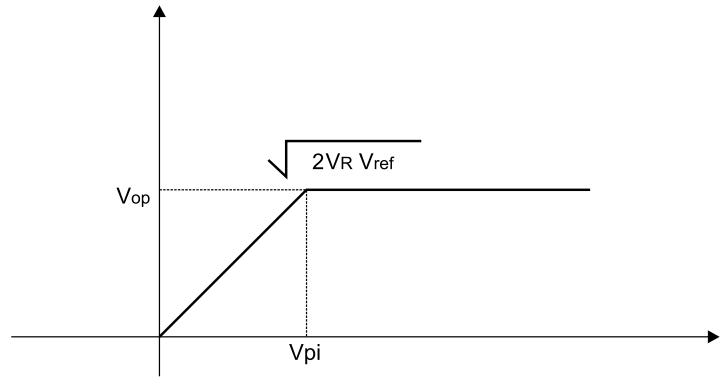
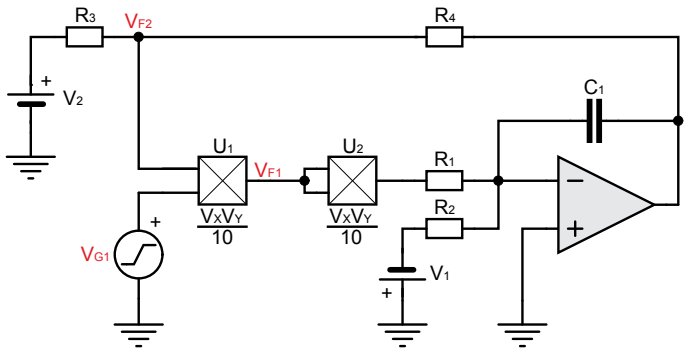


Figure 8.2: Input-Output Characteristics of AGC/AVC

S.No.	Input Voltage	Output Voltage
1		
2		
3		
4		

Table 8.1: Transfer characteristic of the AGC circuit

3. Plot the output as a function of input voltage. Enter sufficient number of readings in Table 8.2. Does the output remain constant as the magnitude of the input is increased? Beyond what value of the input voltage does the gain begin to stabilize? We have included sample output waveform for the AGC circuit in Figure 8.3.



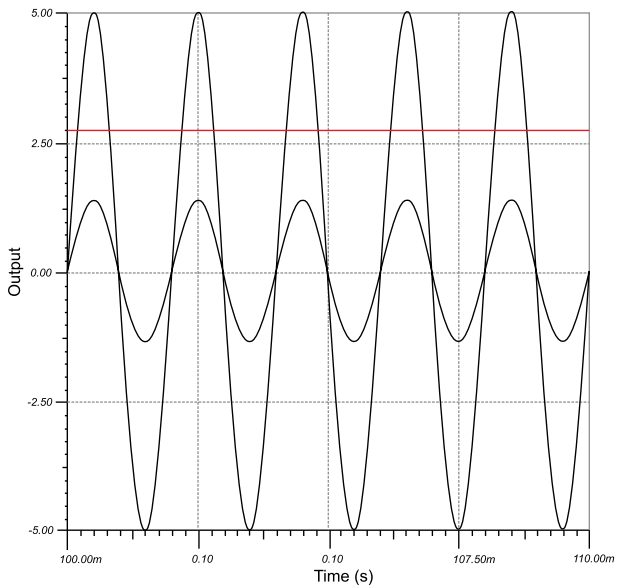


Figure 8.3: AGC circuit and its output

8.5 Exercise Set 8

Determine the lock range for the AGC, which is defined as the range of input values for which output voltage remains constant.

Notes on Experiment 8:

Notes on Experiment 8:

Chapter 9

Experiment 9

DC-DC Converter

Goal of the experiment

The goal of the experiment is to design a high-efficient DC-DC converter using a general purpose OP-Amp and a comparator and study its characteristics. We also aim to study the characteristics of a DC-DC converter IC, and for this purpose we selected the wide-input non synchronous buck DC/DC controller TPS40200 from Texas Instruments. This IC is included in ASLK PRO as evaluation module.

9.1 Brief theory and motivation

The reader will benefit from viewing the recorded lecture at **[24]**. Also refer to the application note, Design Considerations for Class-D Audio Power Amplifiers **[15]**.

Function generator is the basic block for DC-DC converter. The triangular output of the function generator with peak amplitude V_p and frequency f is fed to the comparator whose other input is connected to the reference voltage Vref. The output of this comparator is the PWM (Pulse width modulation) waveform whose duty cycle is given by $\frac{\tau}{T} = \frac{1}{2}(1 - V_{ref}/V_p)$, where T is time period of triangular wave and is equal to $T = 1/f$. This duty cycle is directly proportional to reference voltage Vref. If we connect the lossless low-pass filter (LC filter) at the output of the comparator as shown in Figure 9.1, it is possible to get stable DC voltage V_{av} with high efficiency between $\pm V_{ss}$ depending upon the value of V_{ref}. Hence circuit becomes SMPS system where $V_{av} = -V_{ref} \cdot V_{ss}/V_p$.

If we replace LC filter with MOSFET, and apply audio input as V_{ref} to the comparator then at output of the MOSFET amplified audio output is obtained, this is Class D Power Amplifier operation.

9.2 Specifications

Design a DC-DC converter which has 10 kHz oscillator whose triangular wave output with peak amplitude Vp is fed to a comparator whose other input is connected to Vref (reference voltage).

9.3 Measurements to be taken

9.3.1 Time response

Obtain the time response of the system and plot V_{ref} versus $\frac{\tau}{T}V_{ref}$.

9.3.2 Transfer function

Obtain the V_{ref} versus V_{av} characteristics.

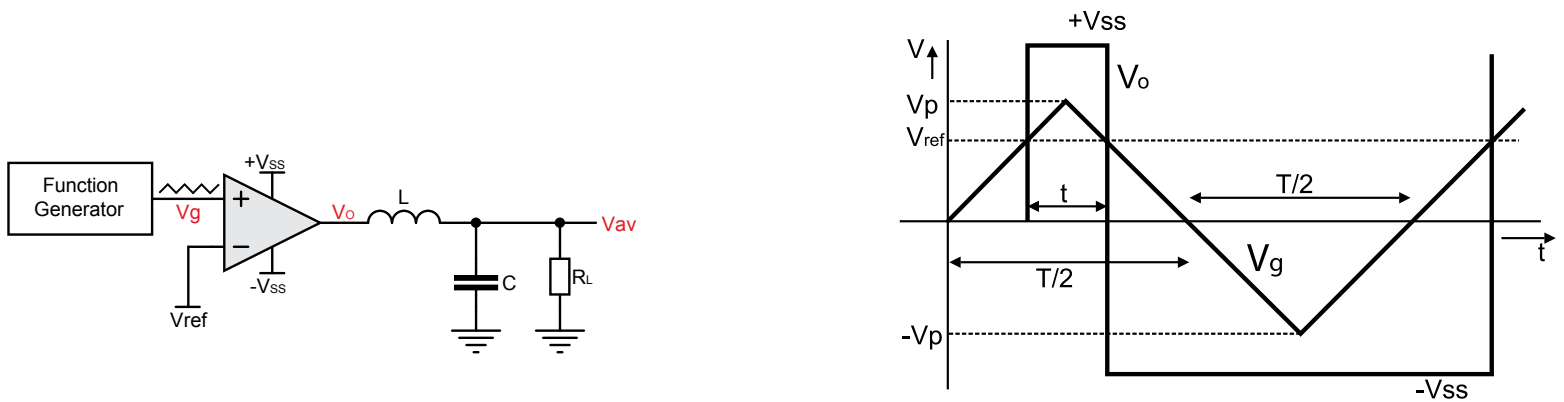


Figure 9.1: DC-DC Converter and PWM waveform

9.4 What should you submit

1. Simulate the circuits and obtain the time response and transfer characteristics of the system.
2. Take the plots of transfer characteristics and time response from oscilloscope and compare it with simulation results.
3. Plot the average output voltage V_{av} as a function of reference voltage V_{ref} and obtain the plot; the plot will be linear.
4. Plot the duty cycle V_{ref} as a function of reference voltage V_{ref} and obtain the plot, the plot will be linear. We have included the typical output waveform of the SMPS circuit in Figure 9.2

S.No.	Reference Voltage	Output Voltage
1		
2		
3		
4		

Table 9.1: Variation of output voltage with reference voltage in a DC-DC converter

S.No.	Reference Voltage	Duty Cycle τ/T
1		
2		
3		
4		

Table 9.2: Variation of duty cycle with reference voltage in a DC-DC converter

9.5 Exercise Set 9

Perform the same experiment with the specialized IC for DC-DC converter from Texas Instrument TPS40200 and compare the characteristics of both systems.

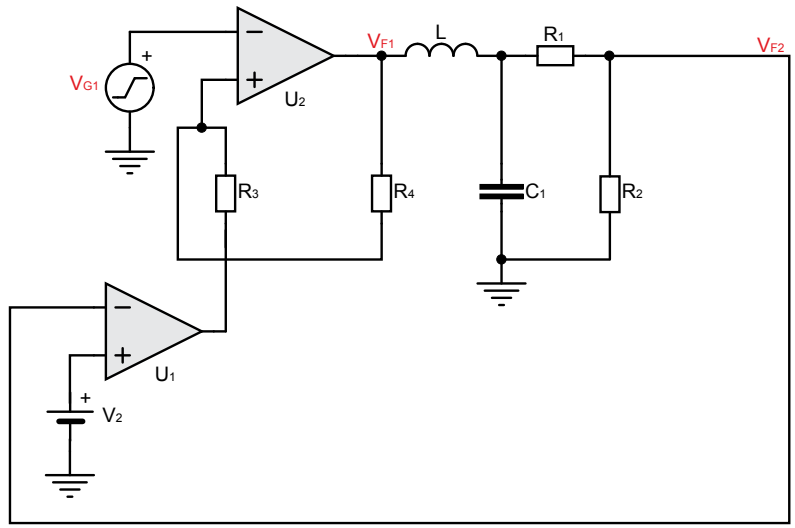
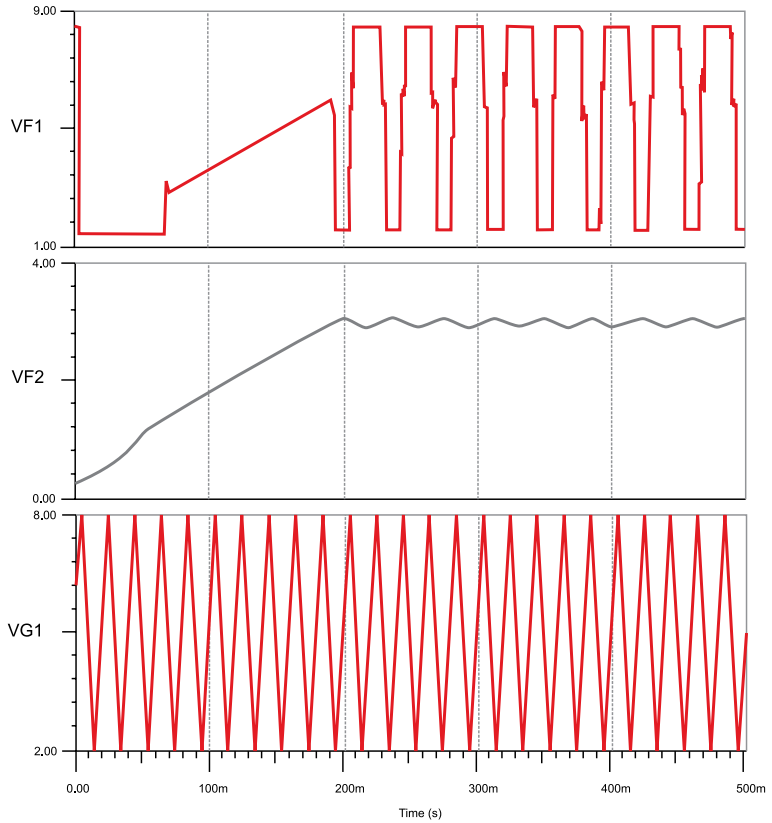


Figure 9.2: (a) SMPS Circuit (b) Output Waveforms



Notes on Experiment 9:

Chapter 10

Experiment 10

Design a Low Dropout (LDO) regulator

Goal of the experiment

The goal of this experiment is to design a Low Dropout regulator using general purpose OP-Amp and PMOS and study its characteristics with extension to study characteristics of TPS7250 IC. We aim to design a linear voltage regulator with high efficiency which is used in low noise high efficiency applications.

10.1 Brief theory and motivation

LDO is used to produce regulated voltage for high efficiency low noise applications. Please view the recorded lectures at **[23]** for a detailed description of voltage regulators. In case of DC-DC converter switching takes place (as shown by PWM waveform) and switching is a source of noise but in LDO no switching takes place hence it is used as voltage regulator in low noise high efficient systems. As shown in the circuit below LDO uses PMOS along with OP-Amp so that power dissipation in OP-Amp is minimal and efficiency is high. The regulated output voltage is given by $V_0 = V_{ref}\left(1 + R_2/R_1\right)$.

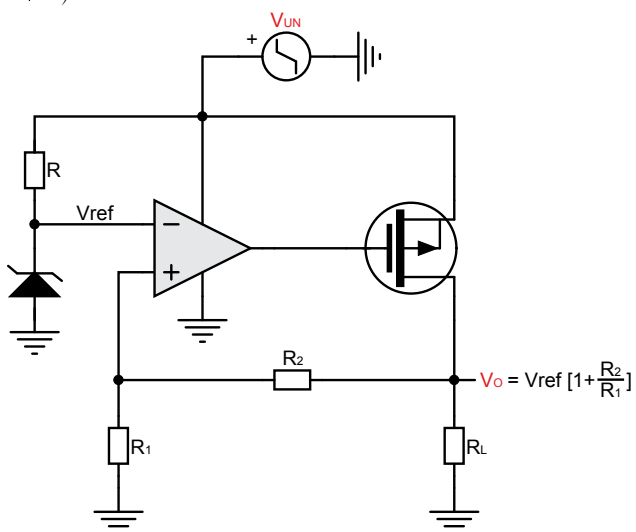


Figure 10.1: Low Dropout Regulator (LDO)

10.2 Specifications

Generate 3V output when input voltage is varying from 4V to 5V.

10.3 Measurements to be taken

1. Output Characteristics - Measure the load regulation of the system. Load regulation is given by dV_0/V_0 when Io is varying from minimum to maximum value.
2. Transfer Characteristics - Measure the line regulation of the system. Line regulation is given by dV_0/V_0 when V_0 is varying from minimum to maximum value.
3. Measure the ripple rejection by applying the ripple input voltage and measuring the output ripple voltage.
4. Measure the output impedance of the LDO, which is given by $\frac{dV_0}{dI_0}$. We have shown the sample output of load regulation and line regulation in Figure 10.2.

S.No.	Reference Voltage	Output Voltage
1		
2		
3		
4		

Table 10.1: Variation of Load Regulation with Load Current in an LDO

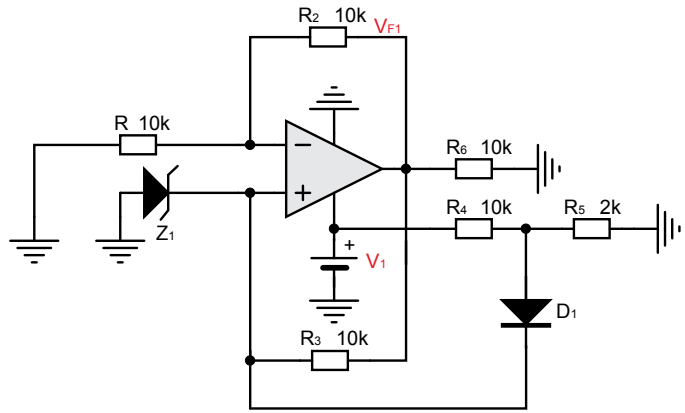
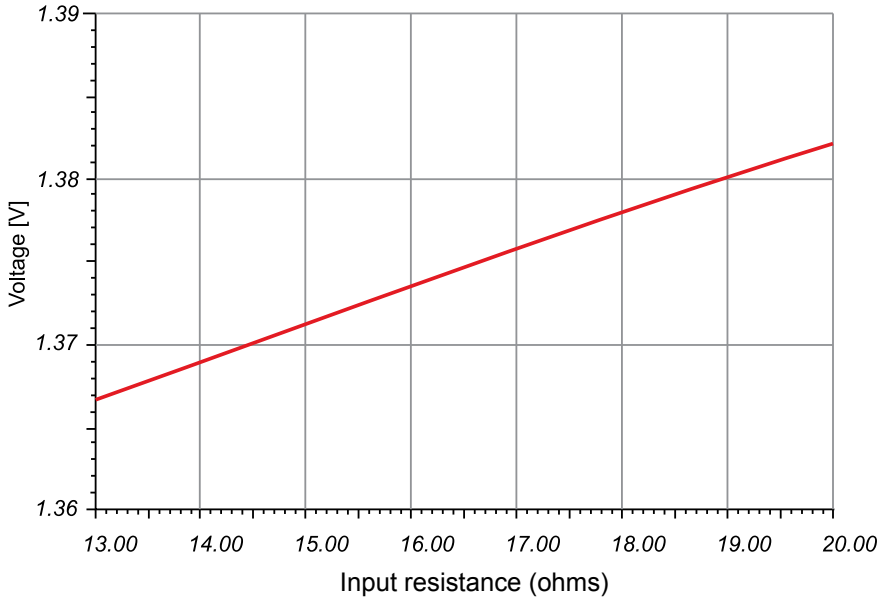
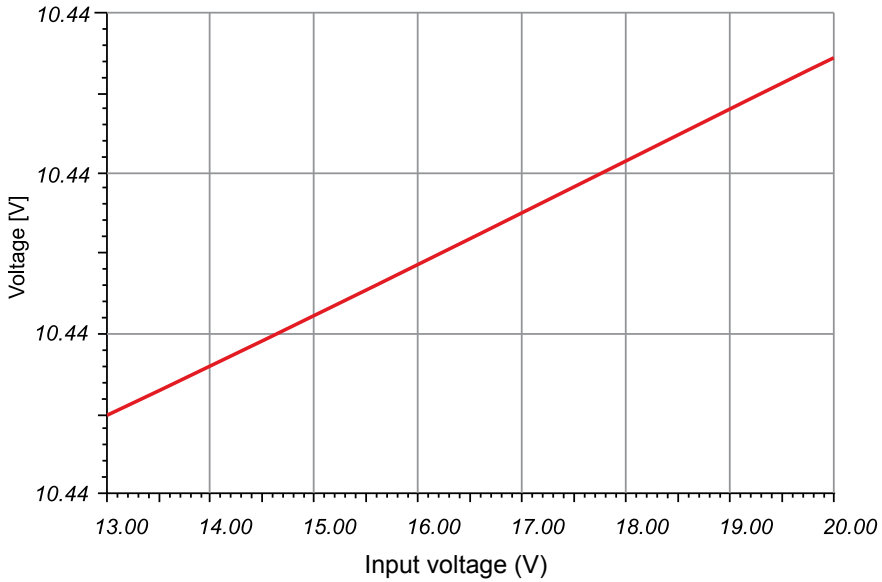


Figure 10.2: A regulator circuit and its simulated outputs - line regulation and load regulation





2. Take the plots of output characteristics, transfer characteristics and ripple rejection from the Oscilloscope and compare it with simulation results.

3. Obtain the Load Regulation - Vary the load such that load current varies and obtain the output voltage, see the point till where output voltage remains constant. After that output will fall as the load current increases.

4. Obtain the Ripple Rejection - Apply the input ripple voltage and see the output ripple voltage, with the input ripple voltage output ripple voltage will rise.

5. Obtain the Line Regulation - Vary the input voltage and plot the output voltage as a function of the input voltage. Until the input reaches a certain value, the output voltage remains constant; after this point, the output voltage will rise as the input voltage is increased.

6. Calculate the output impedance.

S.No.	Input Voltage	Line Regulation
1		
2		
3		
4		

S.No.	Ripple Input Voltage	Ripple Output Voltage
1		
2		
3		
4		

Figure 10.3: Variation of Line Regulation with Input Voltage in an LDO

10.4 What should you submit

1. Simulate the circuits and compute the output characteristics, transfer characteristics, and ripple rejection.

10.5 Exercise Set 10

Perform the same experiment with the specialized IC for LDO from Texas Instrument TPS7250 and compare the characteristics of both systems.

Notes on Experiment 10:

Chapter 11

Experiment 11

To study the parameters of an LDO integrated circuit

Goal of the experiment

The ASLK Pro kit includes an on-board voltage regulator evaluation module TPS7250. The goal of this experiment is to study the parameters of the Low Dropout Regulator (LDO) IC TPS7250 from Texas Instruments using the on-board evaluation module.

11.1 Brief theory and motivation

TPS7250 evaluation module helps us evaluate the operation and performance of the TPS7250 family of linear regulators. The linear regulator TPS7250 from Texas Instruments is capable of 200mA output current at 5V fixed output voltage level. It is a low quiescent current, low noise, high PSRR, fast start-up LDO with excellent line and transient response. See Figure 11.1 for the schematic diagram of the evaluation module.

The input supply voltage VIN is fed at screw terminal CN3 and falls in the range 5.5V to 11V. The leads to the input supply must be as short as possible and must be twisted to reduce EMI transmission. The capacitor C102 improves the transient response of the regulator. The capacitor C101 helps to reduce the ringing on input when supply wires are too long.

The regulator can be enabled/disabled using the **ON/OFF** jumper **JP7**. The "Enable" pin (EN) must never be left floating. Connecting a shorting jumper wire between pins 1 (GND) and pin 2 (EN) of JP7 enables the regulator. Connecting a jumper wire between pins 2 (EN) and pin 3 (VIN) disables the regulator. Output voltage is available on screw terminal **CN4**, or **Vout** pin header, and the typical load current is 200mA.

11.2 Specifications

To study the parameters (Line regulation, Load regulation) of LDO TPS7250 using the on-board evaluation module.

11.3 Measurements to be taken

1. Obtain the Line Regulation: Vary the input voltage (from 5.5V to 11V in steps of 0.5V) and plot the output voltage as the function of the input voltage for a fixed output load.

2. Obtain the Load Regulation: Vary the load (within the permissible limits) such that load current varies and obtain the output voltage for a fixed input voltage. Plot the output voltage as function of the load current.

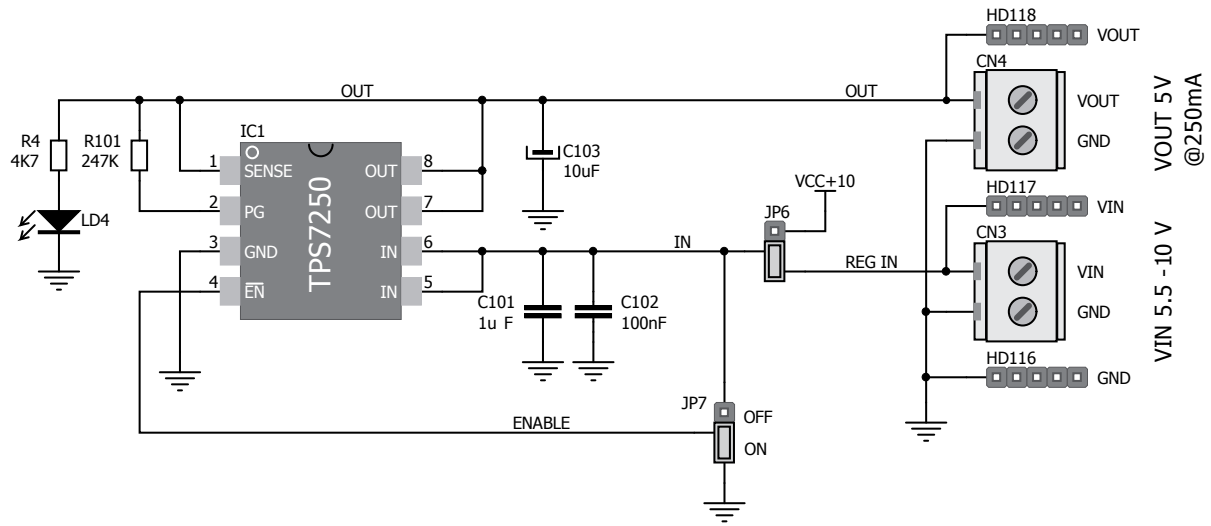


Figure 11.1: Schematic diagram of on-board evaluation module

11.4 What should you submit?

1. Simulate the circuit using a simulator such as **PSPICE Capture** (version 15.7 or higher) or **Cadence** 16.0. The typical characteristics will be of the form as shown in Figure 11-2(a) and Figure 11-2(b).

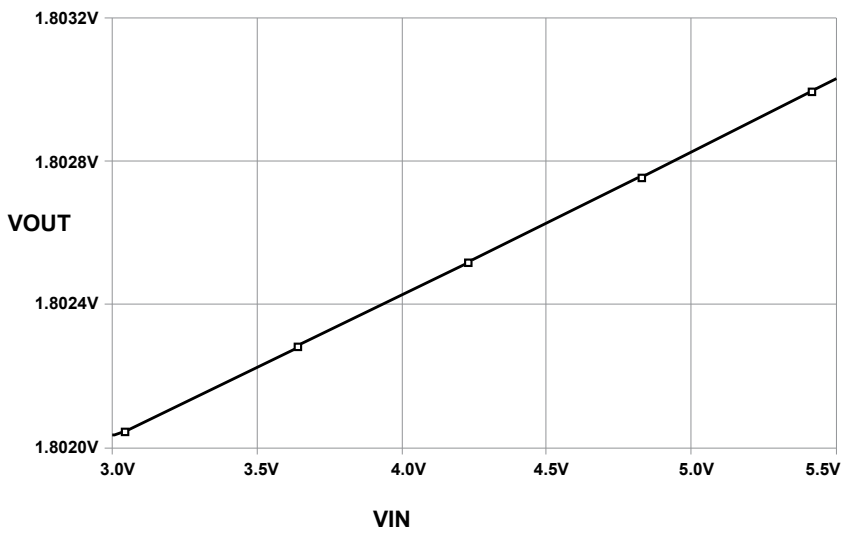


Figure 11.2(a): Line regulation

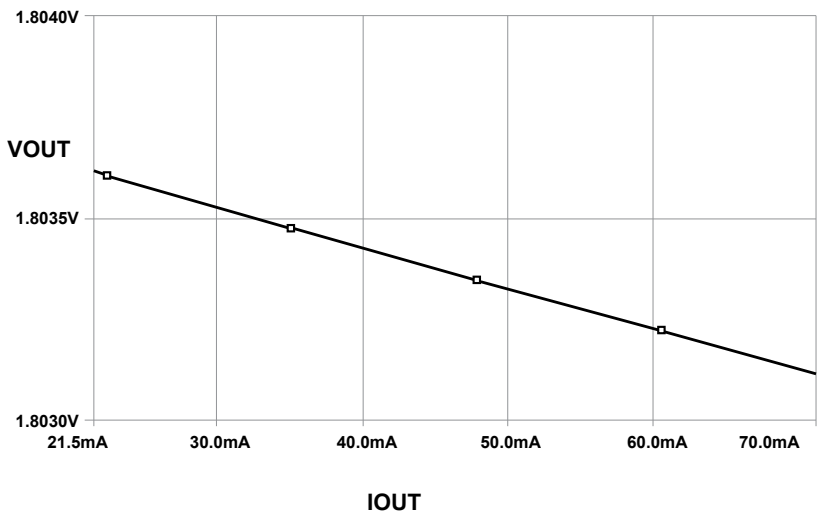


Figure 11.2(b): Load regulation

2. Vary the input voltage for constant load and observe the output voltage. Use Table 11-1 for taking the readings for line regulation.

S.No.	Input voltage (VIN)	Output voltage (VOUT)
1		
2		
3		
4		

Table 11.1: Line regulation

3. Vary the load so that load current varies; observe the output voltage for constant input voltage. Use Table 11-2 for taking the readings for load regulation.

S.No.	Load current (IOUT)	Output voltage(VOUT)
1		
2		
3		
4		

Table 11-.2: Load regulation

Notes on Experiment 11:

Chapter 12

Experiment 12

To study the parameters of a DC-DC Converter using on-board Evaluation module

Goal of the experiment

The goal of the experiment is to configure the on-board evaluation module TPS40200 on the ASLK PRO Kit as a switched mode power supply that can provide a regulated output voltage of 5V or 3.3V for an input whose range is 6V-15V.

12.1 Brief theory and motivation

The TPS40200 evaluation module included on ASLK PRO. Kit uses the TPS40200 non synchronous buck converter to provide a resistor-selected, 3.3V or 5V output that delivers up to 2.5A from up to 16V input bus. See Figure 12-1 for a schematic diagram of the EVM. The evaluation module operates from a single supply and uses the single P-channel Power FET and Schottky diode to produce a low cost buck converter. The regulated output of the EVM is resistance-selected and can be adjusted within the limited range by making the changes in the feedback loop, as shown below.

$$V_{out} = \frac{V_{ref}}{\beta}$$

$$V_{ref} = 0.7V$$

$$\beta = \frac{R_{209}}{R_{209} + R_{207}}$$

The feedback factor β can be changed by changing feedback resistance R209 to adjust the output. But in ASLK PRO, we do not have the provision of changing R209. We can therefore achieve this task by connecting an external resistance of suitable value between the terminals TP8 and the ground.

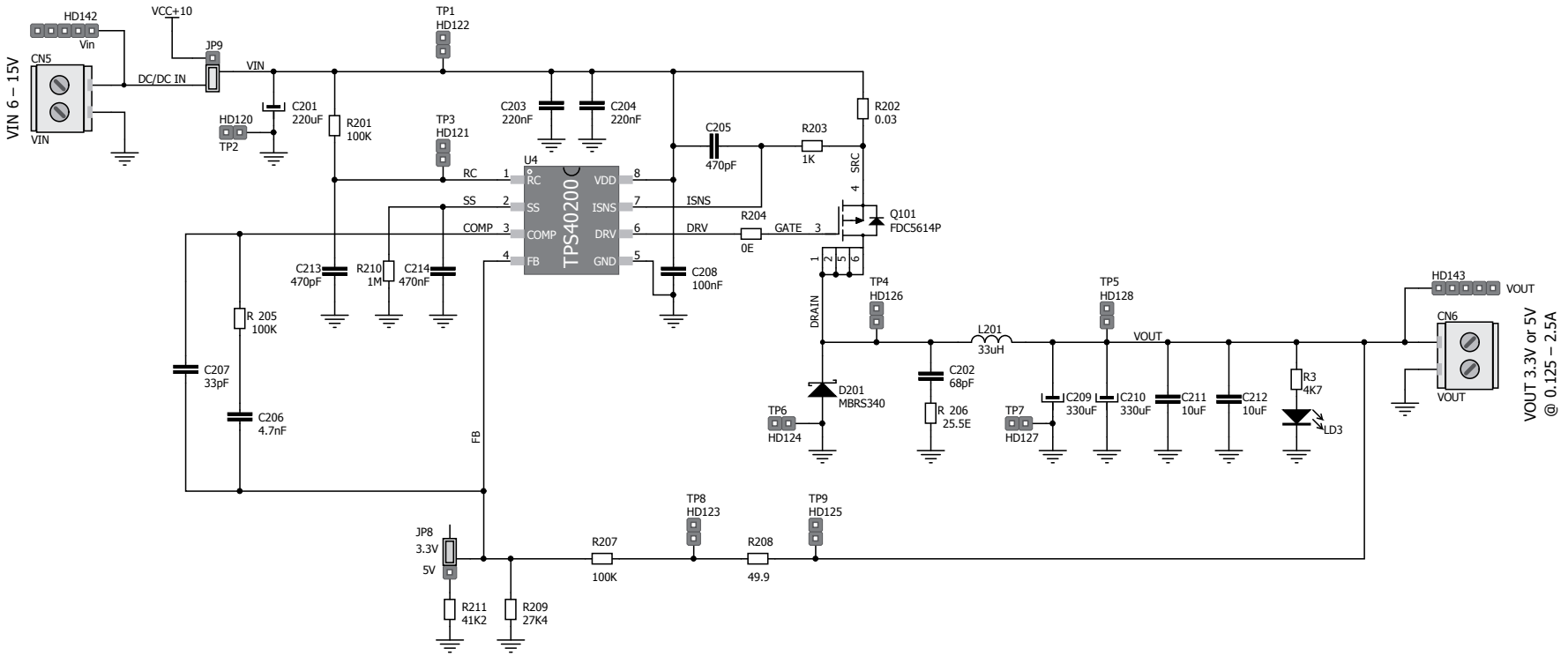


Figure 12.1: Schematic of the on-board EVM

What should be the value of the external resistance for the regulated output of 5V?

The unregulated input is connected at screw terminal CN5. Output load is connected to screw terminal at CN6.The switching waveform can be observed at the terminal TP4.The evaluation module has a switching frequency of 200 kHz. This frequency is decided by the combination of R201 and C213. The duty cycle of this waveform varies linearly with the input voltage for a constant output voltage, as shown below.

$$V_{out} = V_{in} \cdot duty\ cycle$$

The output ripple voltage can be measured across terminals TP5 and TP7 by simply placing the oscilloscope probes. The oscilloscope must be set for $1M\Omega$ impedance, AC coupling. The same terminals can be used for the measurement of the regulated output DC voltage using a voltmeter.

12.2 Specifications

In this experiment, we wish to study the line and load regulation for the TPS40200 integrated circuit when it is configured to generate a 5V DC output.

12.3 Measurements to be taken

Configure the on board evaluation module to generate constant 5V DC output by making the changes in the feedback path using the available terminals.

1. Obtain the Line Regulation: Vary the input voltage from 10V to 15V in steps of 0.5V and plot the output voltage as the function of the input voltage for a constant output load.

2. Obtain the Load Regulation: Vary the load (within the permissible limits) such that load current varies and obtain the output voltage for constant input voltage. Plot the output voltage as a function of the load current.

12.4 What should you submit?

1. What should be the value of the external resistance to be connected between TP8 and Ground to configure the evaluation module to generate regulated output voltage of 5V?

2. Simulate the configured circuit using a simulator. The typical waveforms will be of the form shown in Figure 12.2.

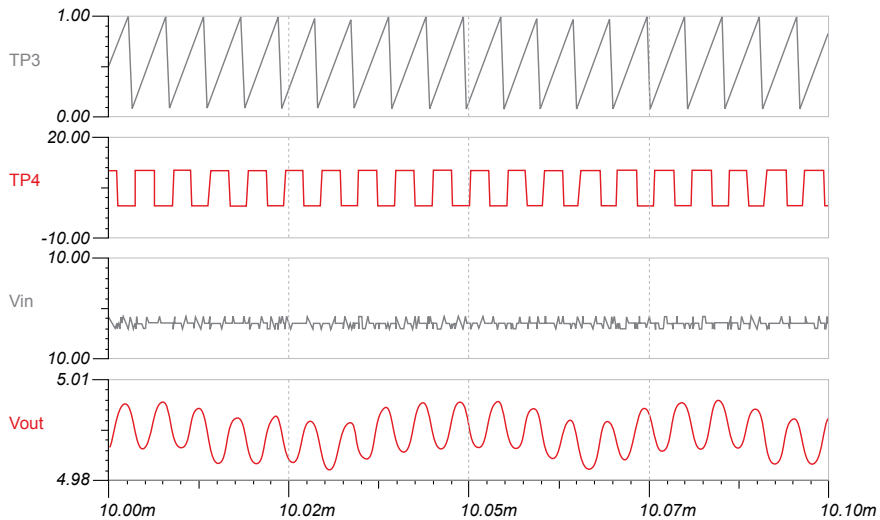


Figure 12.2: Simulation waveforms - TP3 is the PWM waveform and TP4 is the switching waveform

3. Configure the on board evaluation module to generate a regulated output voltage of 5V, and observe the waveforms mentioned in Figure 12.2 and compare with the simulation results.

4. Vary the input voltage for a regulated output voltage of 5V and observe the change in the duty cycle of the PWM waveform. Use Table 12.1 to record the readings. Compare the readings with simulation results and plot the graph between the input voltage and duty cycle. Is the plot linear?

S.No.	Input voltage (Vin)	Duty cycle
1		
2		
3		
4		

Table 12.1: Variation of the duty cycle of PWM waveform with input voltage

5 Vary the input voltage for a fixed load and observe the output voltage. Use Table 12.2 for taking the readings for line regulation

S.No.	Input voltage (Vin)	Output voltage (Vout)
1		
2		
3		
4		

Table 12.2: Line regulation

6 Vary the load so that load current varies; observe the output voltage for a fixed input voltage. Use Table 12.3 for taking the readings.

S.No.	Load current	Output voltage (Vout)
1		
2		
3		
4		

Table 12.3: Load regulation

Notes on Experiment 12:

Chapter 13

Experiment 13

Design of a Digitally Controlled Gain Stage Amplifier

Goal of the experiment

The goal of the experiment is to design a negative feedback amplifier whose gain is digitally controlled using a multiplying DAC.

13.1 Brief theory and motivation

More and more, we see the trend of using Digital Signal Processors and/or Microcontrollers to control the behavior of the front-end signal conditioning circuits in an instrumentation or RF system. Examples of such systems are Automatic Gain Control system and Automatic Voltage Control systems. In this experiment, we will demonstrate the use of a multiplying DAC to control the gain of a programmable gain amplifier; we include an exercise at the end of this chapter to illustrate the use of a microcontroller for controlling the gain of a programmable gain amplifier.

See Figure 13.1 for the circuit of an inverting amplifier; the gain of this amplifier can be digitally controlled by changing the bit pattern presented to the input of the multiplying DAC, **DAC7821**.

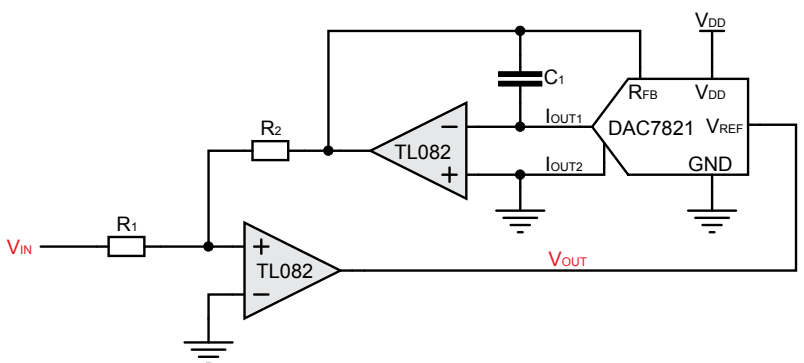


Figure 13.1: Circuit for Digital Controlled Gain Stage Amplifier

Let the 12-bit input pattern to DAC be given by $(A_{11}\,A_{10}\ldots A_0)$. The expression for the output voltage of the negative feedback amplifier is given by

$$V_{out} = V_{in} \cdot \frac{R_2}{R_1} \cdot \frac{4096}{\sum_{0}^{11} A_n 2^n}$$

13.2 Specifications

To study the variation in gain when the bit pattern applied to the input of the DAC is changed.

13.3 Measurements to be taken

Apply a 100 Hz sine wave of 100mV peak amplitude at V_{in} and measure the output voltage amplitude. Select R_2/R_1 to be 2.2. Vary the input bit pattern $(A_{11}\,A_{10}\ldots A_0)$ and measure the amplitude of the output voltage.

13.4 What should you submit?

1. The circuit of Figure 13.1 cannot be directly simulated, since the macro-model for **DAC7821** is not available at the time of writing. For the purpose of simulation, we will use the macro model of a different 12-bit DAC, the **MV95308**. Simulate the circuit schematic shown in Figure 13.2, which is equivalent to the circuit of Figure 13.1. Observe the output waveforms for different bit patterns. The typical simulation waveforms are of the form shown in Figure 13.3.

2. Use the circuit shown in Figure 13.1 for practical implementation of the Digital programmable gain stage amplifier.

3. Apply the sine wave of fixed amplitude and vary the bit pattern, as shown in Table 13.1. Note the Peak to Peak amplitude of the output. Compare the simulation results with the practical results.

S.No.	BIT Pattern	Peak to Peak Amplitude of the output
1	**100000000000**	
2	**010000000000**	
3	**001000000000**	
4	**000100000000**	

Table 13.1: Variation in output amplitude with bit pattern

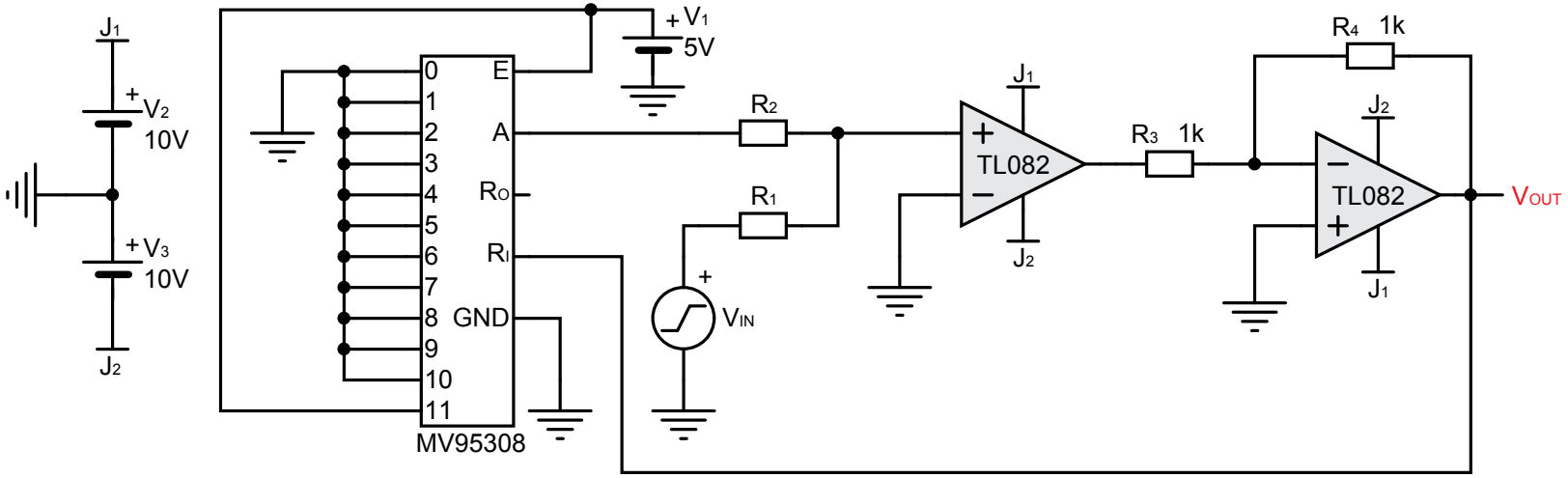


Figure 13.2: Equivalent Circuit for simulation

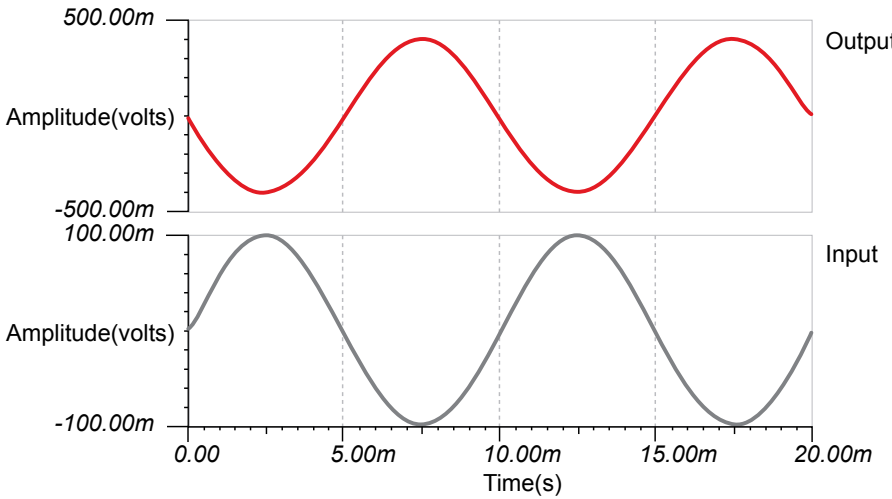


Figure 13.3: Simulation output of digitally controlled gain stage amplifier when the input pattern for the DAC was selected to be 0x800

13.5 Exercise Set 13

Design a digitally programmable non-inverting amplifier whose gain varies from 6.4 and above.

Notes on Experiment 13:

Notes on Experiment 13:

Chapter 14

Experiment 14

Design of a Digitally Programmable Square and Triangular wave generator/oscillator

Goal of the experiment

To design a digitally controlled oscillators where the oscillation frequency of the output square and triangular wave forms is controlled by a binary pattern. Such systems are useful in digital PLL and in FSK generation in a MODEM.

14.1 Brief theory and motivation

In Experiment 6, we used an analog multiplier in conjunction with an integrator to build a VCO. In this experiment, we will use a multiplying **DAC7821** (instead of a multiplier) and an integrator to implement a digitally controlled square and triangular wave generator. See Figure 14.1 for the circuit schematic of a digitally programmable square and triangular wave generator. VOUT is the square wave output and the output of the integrator is the triangular waveform.

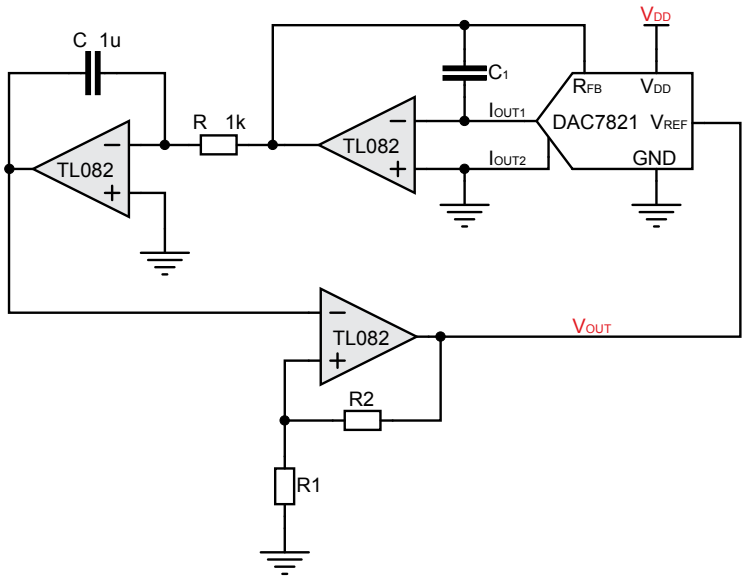


Figure 14.1: Circuit for Digital Controlled Oscillator

Frequency of oscillations of digital programmable oscillator is given by

$$f = \frac{1}{4RC} \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{\sum_{0}^{11} A_n 2^n}{4096}$$

14.2 Specifications

Design a Digitally Programmable Oscillator that can generate square and triangular waveforms with a maximum frequency of 400 Hz.

14.3 Measurements to be taken

Implement the Digitally programmable Square and Triangular wave generator using the circuit as shown in Figure 14.1.Observe the frequency of Oscillations of system and vary it by varying bit pattern input to the DAC.

14.4 What Should you Submit

1. Simulate the circuit using any simulator and observe the frequency of oscillation of the square and triangular waveforms. See Figure 14.2 for the result of simulation. The typical simulation waveforms are of the form shown in Figure 14.3. For this simulation, we used the macro-model of **MV95308** since the macro-model for the DAC is not available at the time of writing.
2. Vary the bit pattern input to the DAC in manner specified in Table 14.1 and note down the change in the frequency of oscillations and compare the practical results with the simulation results.
3. Plot a graph where the x-axis shows the analog equivalent of the bit pattern and the y-axis shows the frequency of oscillations. Note that the 12-bit input to the DAC is interpreted as an unsigned number.

S.No.	BIT Pattern	Peak to Peak Amplitude of the output
1	**100000000000**	
2	**010000000000**	
3	**001000000000**	
4	**000100000000**	

Table 14.1: Varying the bit pattern input to the DAC

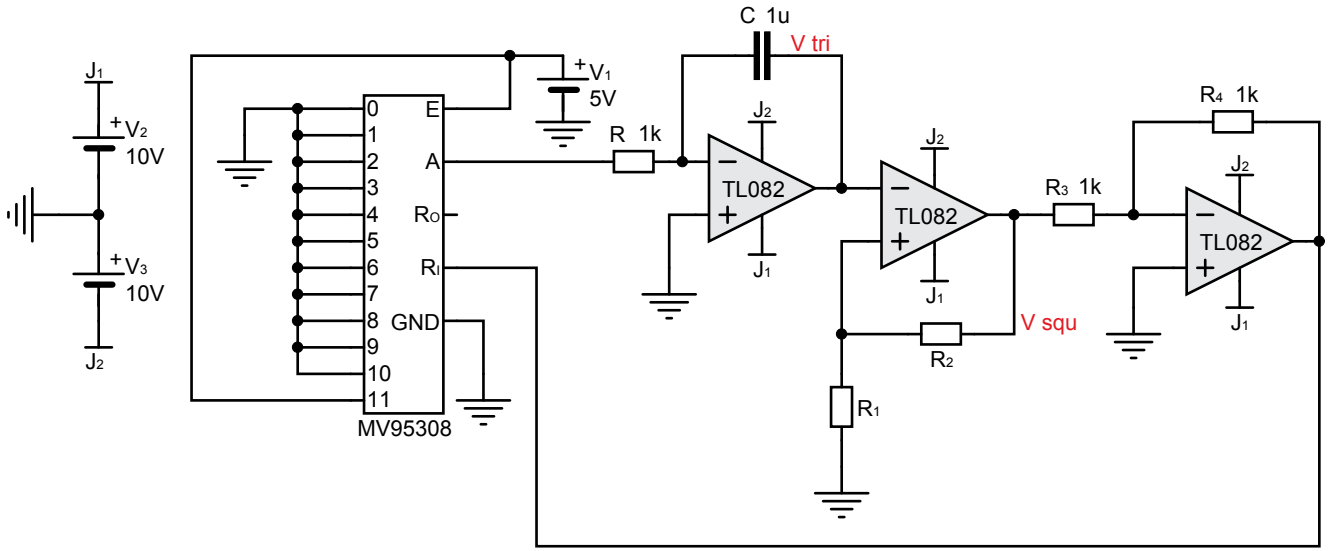


Figure 14.2: Circuit for Simulation

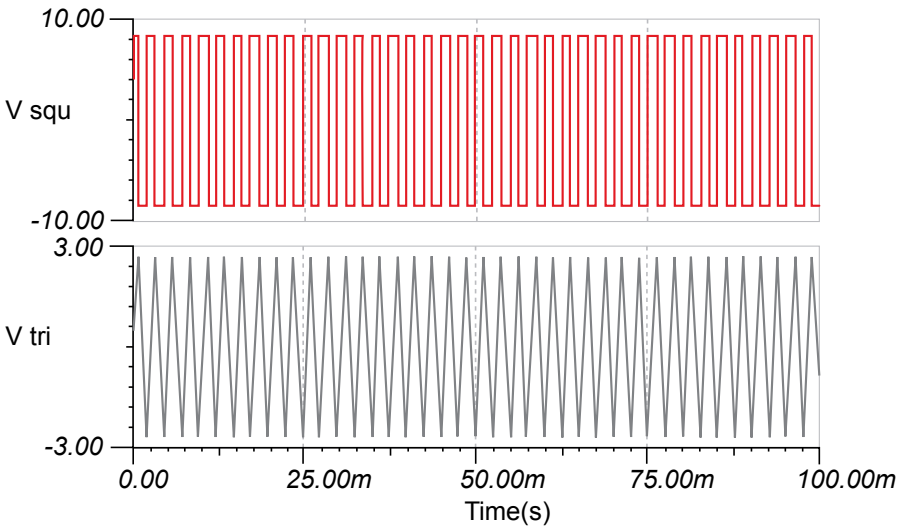


Figure 14.3: Simulation Results

Notes on Experiment 14:

14.5 Exercise Set 14

Design a digitally programmable band-pass filter with $Q = 10$ and gain of 1 at the centre frequency.

Notes on Experiment 14:

Appendix A

ICs used in ASLK PRO

Texas Instruments Analog ICs used in ASLK PRO

JFET-Input Operational Amplifier

TL082

A.1.1 Features

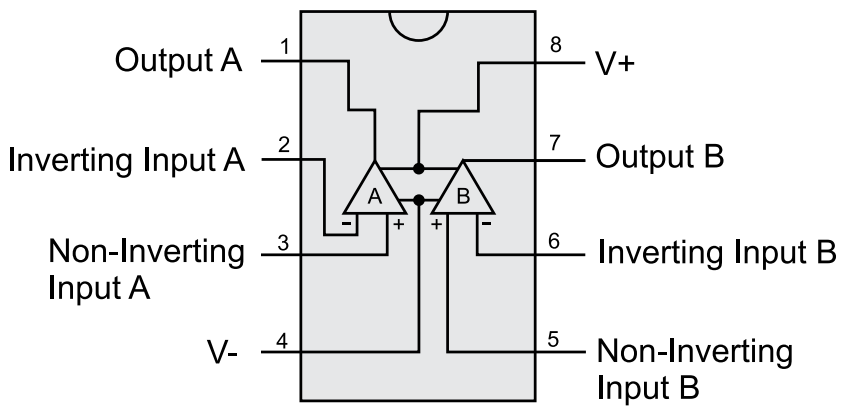
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion...0.003% Typ
- High Input Impedance...JFET-Input Stage
- Latch-Up-Free Operation
- High Slew Rate...13 V/μs Typ
- Common-Mode Input Voltage Range Includes VCC+

A.1.2 Applications

- Input Buffer
- High-Speed Integrators
- D/A Converters
- Sample And Hold Circuits

A.1.4 Download Datasheet

http://www.ti.com/lit/gpn/tl082



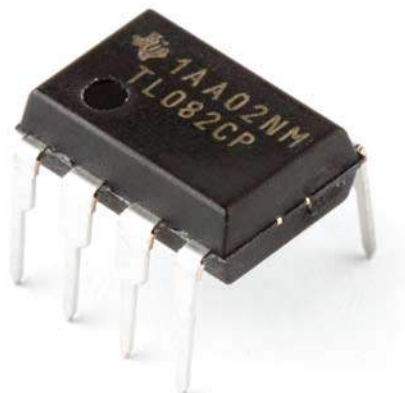


Figure A.1: TL082 - JFET-Input Operational Amplifier

A.1.3 Description

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family. The C-suffix devices are characterized for operation from 0˚C to 70˚C. The I-suffix devices are characterized for operation from -40˚C to 85˚C. The Q-suffix devices are characterized for operation from -40˚C to 125˚C.

MPY634

Wide Bandwidth Analog Precision Multiplier

A.2.1 Features

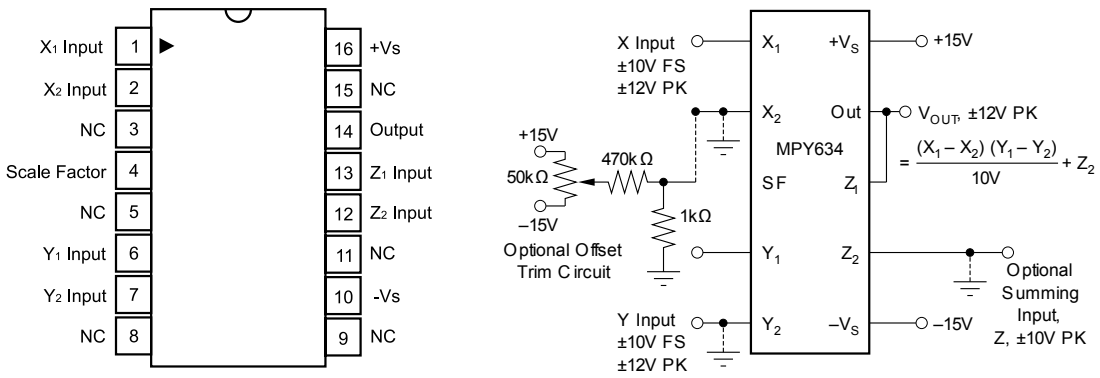
- Wide Bandwidth: 10MHz Typ
- 0.5% Max Four-Quadrant Accuracy
- Internal Wide-Bandwidth Op Amp
- Easy To Use
- Low Cost

A.2.2 Applications

- Precision Analog Signal Processing
- Modulation And Demodulation
- Voltage-Controlled Amplifiers
- Video Signal Processing
- Voltage-Controlled Filters And Oscillators

A.2.4 Download Datasheet

http://www.ti.com/lit/gpn/mpy634



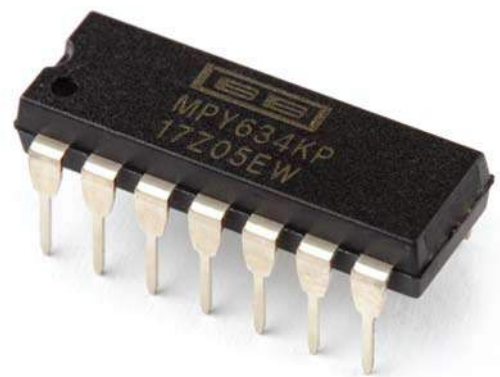


Figure A.2: MPY634 - Analog Multiplier

A.2.3 Description

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy. The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection. An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.

12 Bit, Parallel, Multiplying DAC

DAC 7821

A.3.1 Features

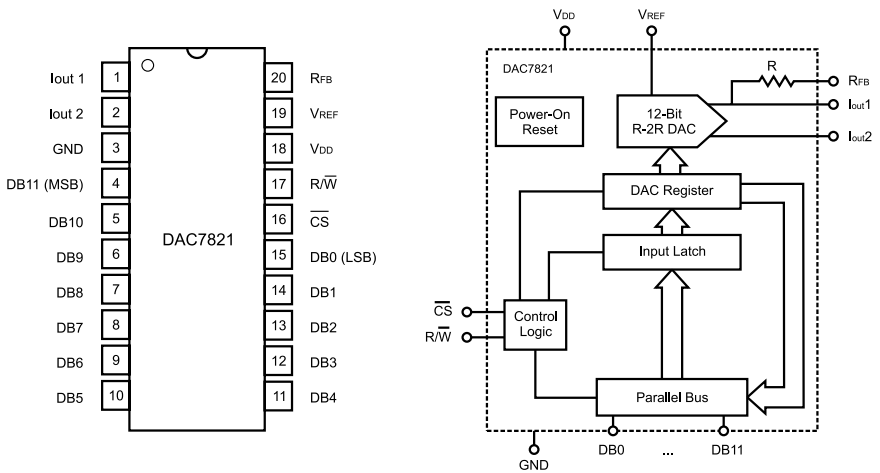
- 2.5V to 5.5V supply operation
- Fast Parallel Interface: 17ns Write Cycle
- Update Rate of 20.4MSPS
- 10MHz Multiplying Bandwidth
- 10V input
- Low Glitch Energy: 5nV-s
- Extended Temperature Range: -40˚C to +125˚C
- 20-Lead TSSOP Packages
- 12-Bit Monotonic
- 1LSB INL
- Read back Function
- Power-On Reset with Brownout Detection
- Industry-Standard Pin Configuration
- 4-Quadrant Multiplication

A.3.2 Applications

- Portable Battery-Powered Instruments
- Analog Processing
- Waveform Generators
- Programmable Amplifiers and Attenuators
- Digitally Controlled Calibration
- Programmable Filters and Oscillators
- Composite Video
- Ultrasound

A.3.4 Download Datasheet

http://www.ti.com/lit/gpn/dac7821



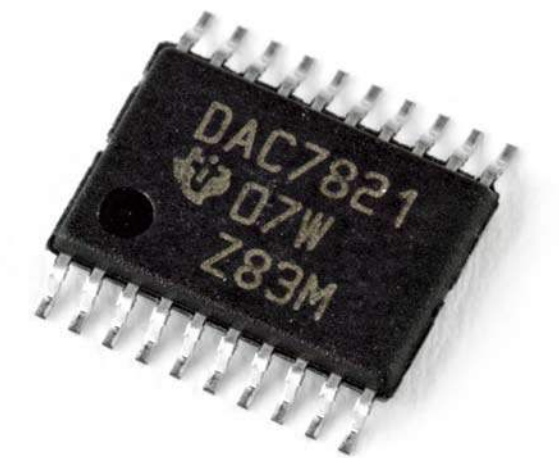


Figure A.3: DAC 7821 - Digital to Analog Converter

A.3.3 Description

The DAC7821 is a CMOS 12-bit current output digital-to-analog converter (DAC). This device operates from a single 2.5V to 5.5V power supply, making it suitable for battery-powered and many other applications. This DAC operates with a fast parallel interface. Data read back allows the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeroes and the DAC outputs are at zero scale. The DAC7821 offers excellent 4-quadrant multiplication characteristics, with a large signal multiplying and width of 10MHz. The applied external reference input voltage (VREF) determines the full-scale output current. An integrated feedback resistor (RFB) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier. The DAC7821 is available in a 20-lead TSSOP package.

TPS40200

Wide-Input, Non-Synchronous Buck DC/DC Controller

A.4.1 Features

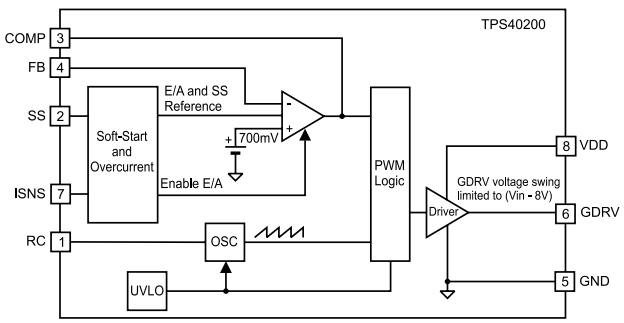
- Input Voltage Range 4.5 to 52 V
- Output Voltage (700 mV to 90% VIN)
- 200 mA Internal P-Channel FET Driver
- Voltage Feed-Forward Compensation
- Undervoltage Lockout
- Programmable Fixed Frequency (35-500 kHz) Operation
- Programmable Short Circuit Protection
- Hiccup Overcurrent Fault Recovery
- Programmable Closed Loop Soft Start
- 700 mV 1% Reference Voltage
- External Synchronization
- Small 8-Pin SOIC (D) and QFN (DRB) Packages

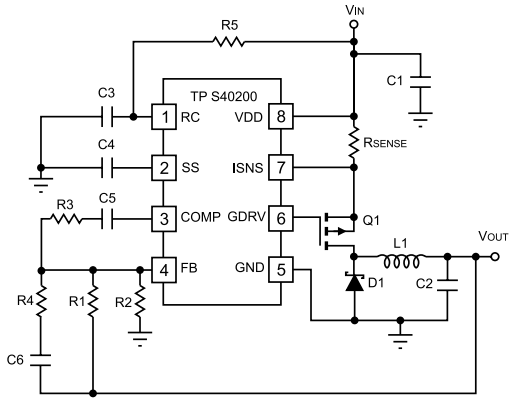
A.4.2 Applications

- Industrial Control
- DSL/Cable Modems
- Distributed Power Systems
- Scanners
- Telecom

A.4.4 Download Datasheet

http://www.ti.com/lit/gpn/tps40200





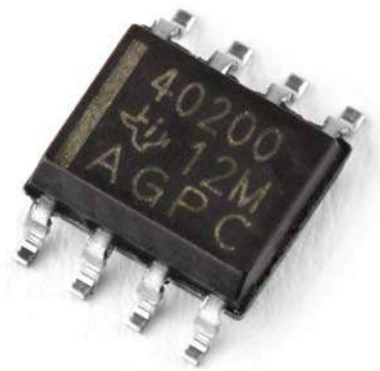


Figure A.4: TPS40200 - DC/DC Controller

A.4.3 Description

The TPS40200 is a flexible non-synchronous controller with a built in 200-mA driver for P-channel FETs. The circuit operates with inputs up to 52V with a power-saving feature that turns off driver current once the external FET has been fully turned on. This feature extends the flexibility of the device, allowing it to operate with an input voltage up to 52V without dissipating excessive power. The circuit operates with voltage-mode feedback and has feed-forward input-voltage compensation that responds instantly to input voltage change. The internal 700mV reference is trimmed to 1%, providing the means to accurately control low voltages. The TPS40200 is available in an 8-pin SOIC, and supports many of the features of more complex controllers.

Micropower Low-Dropout (LDO) Voltage Regulator

TPS7250

A.5.1 Features

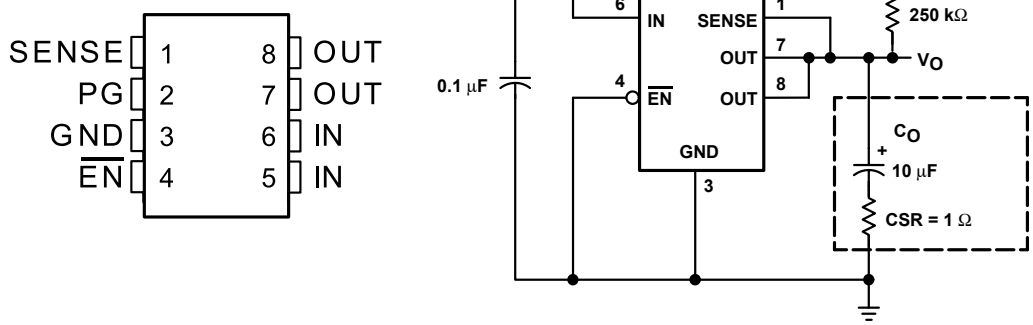
- Available in 5-V, 4.85-V, 3.3-V, 3.0-V, and 2.5-V Fixed-Output and Adjustable Versions
- Dropout Voltage <85 mV Max at IO = 100 mA (TPS7250)
- Low Quiescent Current, Independent of Load, 180 mA Typ
- 8-Pin SOIC and 8-Pin TSSOP Package
- Output Regulated to ±2% Over Full Operating Range for Fixed-Output Versions
- Extremely Low Sleep-State Current, 0.5 mA Max
- Power-Good (PG) Status Output

A.5.2 Applications

- Wireless Handsets
- Smart Phones, PDAs
- MP3 Players
- ZigBeeTM Networks
- BluetoothTM Devices
- Li-Ion Operated Handheld Products
- WLAN and Other PC Add-on Cards

A.5.4 Download Datasheet

http://www.ti.com/lit/gpn/tps7250



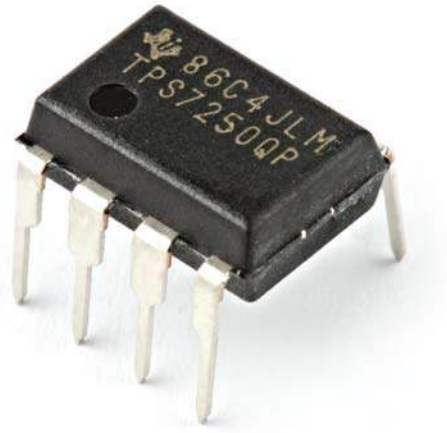


Figure A.5: TPS7250 -Micropower Low-Dropout (LDO) Voltage Regulator

A.5.3 Description

The TPS72xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, micropower operation, and miniaturized packaging. These regulators feature extremely low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in small-outline integrated-circuit (SOIC) packages and 8-terminal thin shrink small-outline (TSSOP), the TPS72xx series devices are ideal for cost-sensitive designs and for designs where board space is at a premium. A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS device. Because the PMOS pass element behaves as a ue resistor, the dropout voltage is very low - maximum of 85 mV at 100 mA of load current (TPS7250) - and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (300 mA maximum) and is stable over the entire range of output load current (0 mA to 250 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage and micropower operation result in a significant increase in system battery operating life.

A.6.1 2N3906 Features

- PNP General Purpose Transistor
- Collector-Emiter Breakdown Voltage: $V_{(BR)CEO}$ = 40V
- Collector-Base Breakdown Voltage: $V_{(BR)CBO}$ = 40V
- h_{FE}: 100 @ I_C = 10mA DC, V_{CE} = 1V DC
- Transition Frequency: f = 100MHz @ V_{CE} = 20V DC, I_C = 10mA DC

Figure A.6: 2N3906
PNP General Purpose Amplifier

A.6.2 Download Datasheet

http://61.222.192.61/mccsemi/up_pdf/2N3906(TO-92).pdf

A.6.3 2N3904 Features

- NPN General Purpose Transistor
- Collector-Emiter Breakdown Voltage: $V_{(BR)CEO}$ = 40V
- Collector-Base Breakdown Voltage: $V_{(BR)CBO}$ = 60V
- h_{FE}: 100 @ I_C = 10mA DC, V_{CE} = 1V DC
- Transition Frequency: f = 100MHz @ V_{CE} = 20V DC, I_C = 10mA DC

Figure A.7: 2N3906
NPN General Purpose Amplifier

A.6.4 Download Datasheet

http://61.222.192.61/mccsemi/up_pdf/2N3904(TO-92).pdf

A.6.5 BS250 Features

- P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET
- Drain-Source Voltage: V_{DS} = -45V
- Continuous Drain Current I_D = -230 mA @ T_{AMB} = 25°C
- Gate-Source Voltage: V_{GS} = ±20 V
- Static Drain-Source on-State Resistance: $R_{DS(ON)}$ = 14Ω @ V_{GS} = -10V, I_D = -200mA
- Gate-Source Threshold Voltage: $V_{GS(TH)}$ Min -1V; Max: -3.5V @ I_D=-1mA, V_{DS}=V_{GS}

Figure A.8: BS250
P-Channel Enhancement
Mode Vertical DMOS FET

A.6.6 Download Datasheet

http://www.diodes.com/datasheets/BS250P.pdf

1N4448 Small Signal Diode

Figure A.9:
1N4448 Small Signal Diode

A.7.1 Features

- Breakdown Voltage: V_R = 100V @ I_R = 100µA
- Forward Voltage: V_F = 620-720mV @ I_F = 5mA
- Reverse Leakage: I_R = 25uA @ V_R = 20V
- Total Capacitance: C_T = 4pF, V_R = 0, f = 1MHz
- Reverse Recovery Time: t_{RR} = 4nS @ I_F = 10mA, V_R = 6.0V, R_L = 100Ω

A.7.2 Download Datasheet

http://www.fairchildsemi.com/ds/1N/1N914.pdf

Appendix B

Introduction to Macromodels

Simulation models are very useful in the design phase of an electronic system. Before a system is actually built using real components, it is necessary to perform a 'software breadboarding' exercise through simulation to verify the functionality of the system and to measure its performance. If the system consists of several building blocks B1, B2, ..., Bn, the simulator requires a mathematical representation of each of these building blocks in order to predict the system performance. Let us consider a very simple example of a passive component such as a resistor. Ohm's law can be used to model the resistor if we intend to use the resistor in a DC circuit. But if the resistor is used in a high frequency application, we may have to think about the parasitic inductances and capacitances associated with the resistor. Similarly, the voltage and current may not have a strict linear relation due to the dependence of the resistivity on temperature of operation, skin effect, and so on. This example illustrates that there is no single model for an electronic component. Depending on the application and the accuracy desired, we may have to use simpler or more complex mathematical models.

We will use another example to illustrate the above point. The MOS transistor, which is the building block of most integrated circuits today, is introduced at the beginning of the course on VLSI design. In a digital circuit, the transistor may be simply modeled as an ideal switch that can be turned on or off by controlling the gate voltage. This model is sufficient if we are only interested in understanding the functionality of the circuit. If we wish to analyze the speed of operation of the circuit or the power dissipation in the circuit, we will need to model the parasitics associated with the transistors. If the same transistor is used in an analog circuit, the model that we use in the analysis would depend on the accuracy which we want in the analysis. We may perform different kinds of analysis for an analog circuit - DC analysis, transient analysis, and steady-state analysis. Simulators such as SPICE require the user to specify the model for the transistor. There are many different models available today for the MOS transistor, depending on the desired accuracy. The level-1 model captures the dependence of the drain-to-source current on the gate-to-source and drain-to-source voltages, the mobility of the majority carrier, the width and length of the channel, and the gate oxide thickness. It also considers non-idealities such as channel length modulation in the saturation region, and the dependence of the threshold voltage on the source-to-bulk voltage. More complex models for the transistor are available, which have more than 50 parameters.

B.1 Micromodels

If you have built an operational amplifier using transistors, a straight-forward way to analyze the performance of the OP-Amp is to come up with the micromodel of the OPAMAP, where each transistor is simply replaced with its corresponding simulation model. Micromodels will lead to accurate simulation, but will prove computationally intensive. As the number of nodes in the circuit increases, the memory requirement will be higher and the convergence of the simulation can take longer.

A macromodel is a way to address the problem of space-time complexity mentioned above. In today's electronic systems we make use of analog circuits such as operational amplifiers, data converters, PLL, VCO, voltage regulators, and so on. The goal of the system designer is not only to get a functionally correct design, but also to optimize the cost and performance of the system. The system-level cost and performance depend on the way the building blocks B1, B2,..., Bn have been implemented. For example, if B1 is an OP-Amp, we may have several choices of operational amplifiers. Texas Instruments offers a large number of operational amplifiers that a system designer can choose from. Refer to Table B.1. As you will see, there are close to 2000 types of operational amplifiers available! These are categorized into 17 different bins to make the selection simpler. However, you will notice that 240 varieties are available in the category of Standard Linear amplifers! How does a system designer select from this large collection? To understand this, you must look at the characteristics of a standard linear amplifier - these include the number of operational amplifiers in a single package, the Gain Bandwidth Product of the amplifier, the CMRR, Vs (min), Vs (max), and so on. See *http://tinyurl.com/ti-std-linear*. The website allows you to specify these parameters and narrow your choices.

But how does one specify the parameters for the components? The overall system performance will depend on the way the parameters for the individual components have been selected. For example, the gain-bandwidth product of an operational amplifier B1 will influence a system-level parameter such as the noise immunity or stability. If one has **n** components in the system, and there are **m** choices for each component, there are **m·n** possible system configurations. Even if we are able to narrow the choices through some other considerations, we may still have to evaluate several system configurations. Performing simulations using micromodels will be a painstaking and non-productive way of selecting system configurations.

B.2 Macromodels

A macromodel is a mathematical convenience that helps to reduce simulation complexity. The idea is to replace the actual circuit by something that is simpler, but is nearly equivalent in terms of input characteristics, output characteristics, and feedforward characteristics. Simulation of a complete system becomes much more simple when we use macromodels for the blocks. Manufacturers of semiconductors provide macromodels for their products to help system designers in the process of system configuration selection. The macromodels can be loaded into a simulator.

	Characteristic	Number of Varieties
1	Standard Linear Amplifier	240
2	Fully Differential Amplifier	28
3	Voltage Feedback	68
4	Current Feedback	47
5	Rail to Rail	14
6	JFET/CMOS	23
7	DSL/Power Line	19
8	Precision Amplifier	641
9	Low Power	144
10	High Speed Amplifier (≥50MHz)	182
11	Low Input Bias Current/FET Input	38
12	Low Noise	69
13	Wide Bandwidth	175
14	Low Offset Voltage	121
15	High Voltage	4
16	High Output Current	54
17	LCD Gamma Buffer	22

Table B.1: Operational Amplifiers available from Texas Instruments

As you can guess, there is no single macromodel for an IC. A number of macromodels can be derived, based on the level of accuracy desired and the computational complexity that one can afford. A recommended design methodology is to start with a simple macromodel for the system components and simulate the system. A stepwise refinement procedure may be adopted and more accurate models can be used for selected components when the results are not satisfactory.

Notes on Appendix B:

Notes on Appendix B:

Appendix C
Activity

Convert your PC/laptop into an Oscilloscope

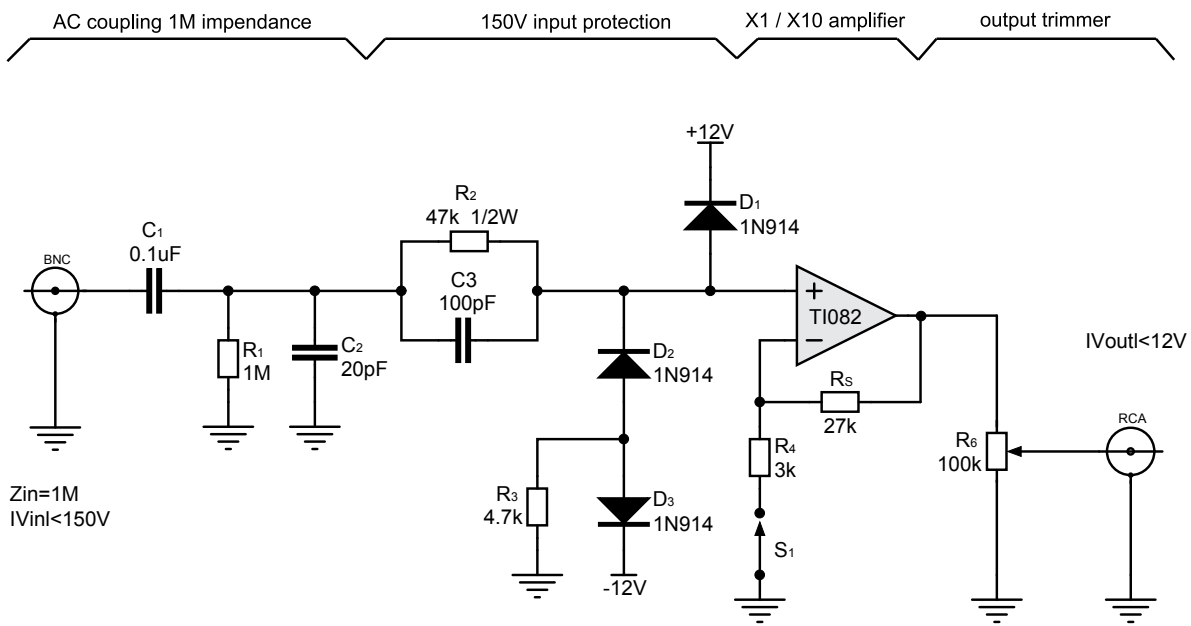
C.1 Introduction

In any analog lab, an oscilloscope is required to display waveforms at different points in the circuit under construction in order to verify circuit operation and, if necessary, redesign the circuit. High-end oscilloscopes are needed for measurements and characterization in labs. Today, solutions are available to students for converting a PC into an oscilloscope. These solutions require some additional hardware to route the analog signals to the PC for observation; they also require software that provides the graphical user interface to convert a PC display into an oscilloscope. Since most students have access to a PC or laptop today, we have designed the Analog System Lab such that a PC-based oscilloscope solution can be used along with ASLK PRO. We believe this will reduce the dependence of the student on a full-edged lab. In this chapter, we will review a solution for a PC-based oscilloscope. The components on the ASLK PRO can be used to build the interface circuit needed to convert the PC into an oscilloscope.

One of the solutions for a "PC oscilloscope" is Zelscope **[33]** which works on personal computers running Microsoft Windows XP. The hardware requirements for the PC are modest (300+ MHz clock, 64+ MB memory). It uses the sound card in the PC for converting the analog signals into digital form. The Zelscope software, which requires about 1 MB space, is capable of using the digitized signal to display waveforms as well as the frequency spectrum of the analog signal. At the 'line in' jack of the sound card, the typical voltage should be about 1 volt AC; hence it is essential to protect the sound card from over voltages. A buffer amplifier circuit is required to protect the sound card from overvoltages. Two copies of such a circuit are needed to implement a dual-channel oscilloscope. The buffer amplifier circuit is shown in Figure C.1 and has been borrowed from **[32]**.

Limitations

- Not possible to display DC voltages (due to input capacitor of sound card blocks DC)
- Low frequency range (10 Hz-20 kHz)
- Measurement is not very accurate



Two identical circuits required for two channels
All resistors are 1/4W, 5% unless noted otherwise
All capacitors are ceramic discs

Adapted from a circuit in:
Horowitz,P and Hill, W, 2nd ed, 1989 *The Art of Electronics*

Oscilloscope probe to sound card line in buffer
by Tim Witham
July 20, 1996

Figure C.1: Buffer circuit needed to interface an Analog Signal to Oscilloscope

Appendix D

Connection diagrams

OP AMP TYPE I - A - INVERTING

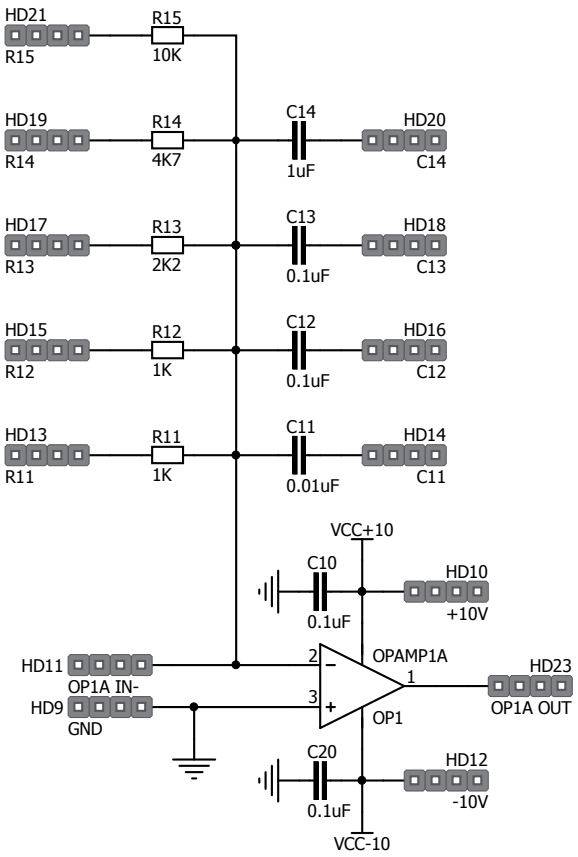


Figure D.1: OP-Amp 1A connected in Inverting Configuration

OP AMP TYPE I - B - INVERTING

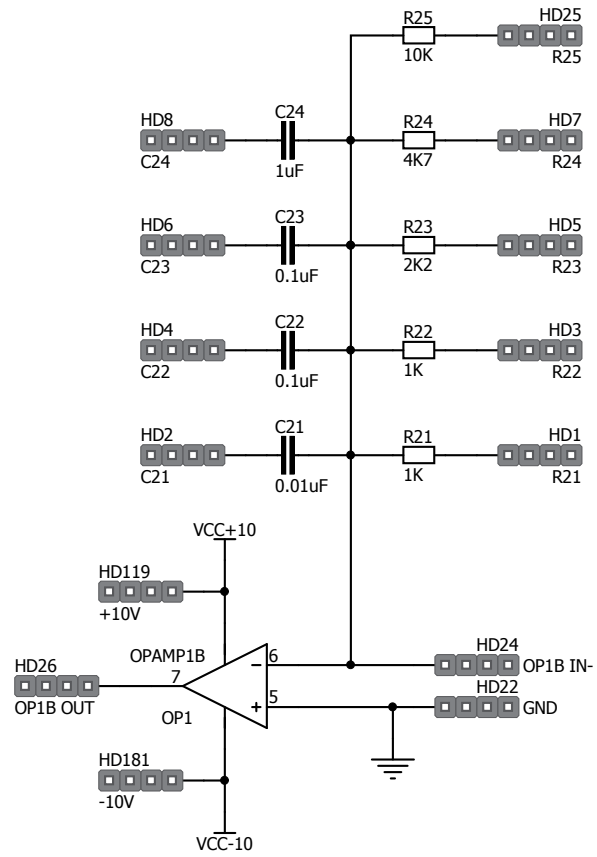


Figure D.2: OP-Amp 1B connected in inverting configuration

OP AMP TYPE II - A - FULL

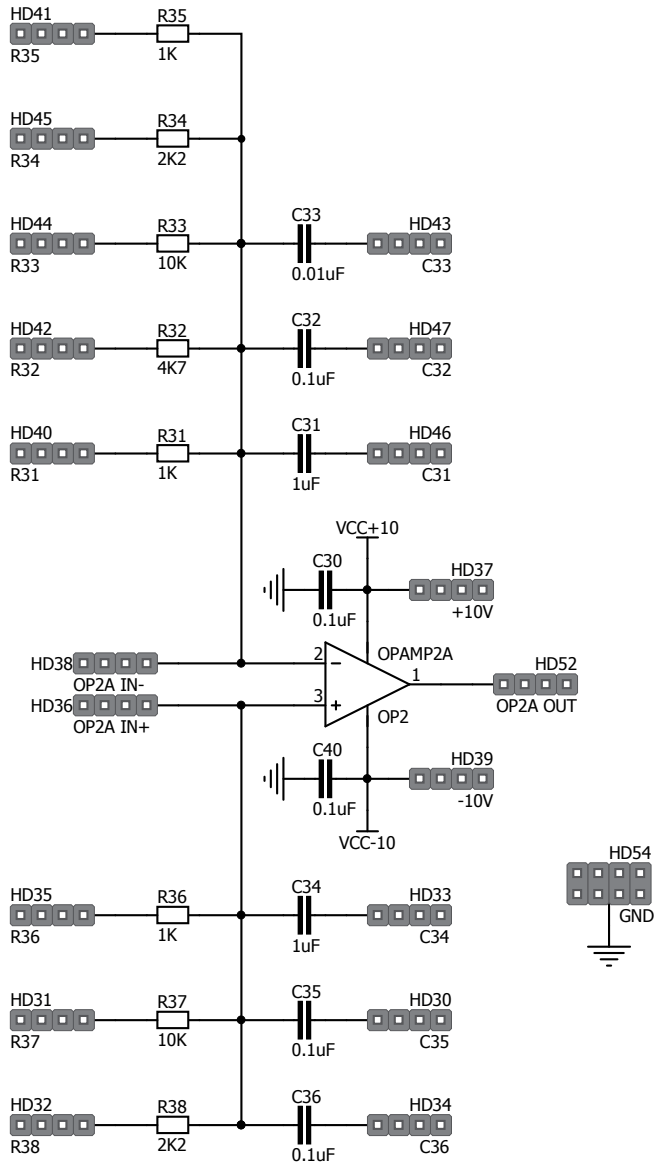


Figure D.3: OP-Amp 2A can be used in both inverting and non-inverting configuration

OP AMP TYPE II - B - FULL

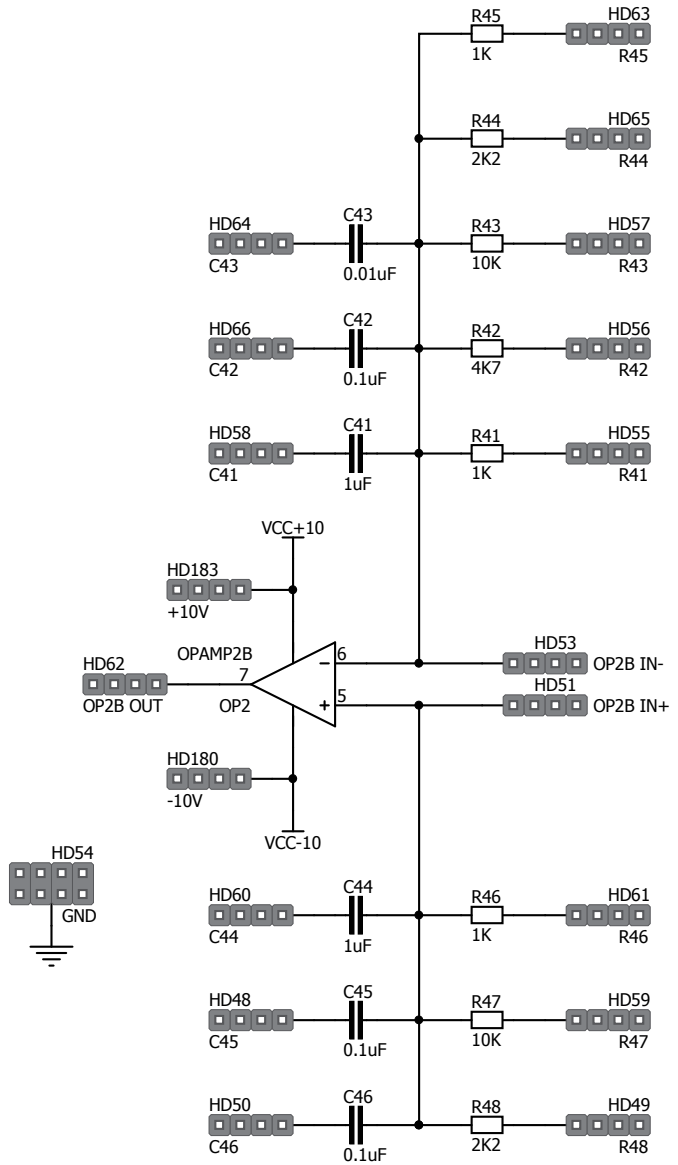


Figure D.4: OP-Amp 2B can be used in both inverting and non-inverting configuration

OP AMP TYPE III - A - BASIC

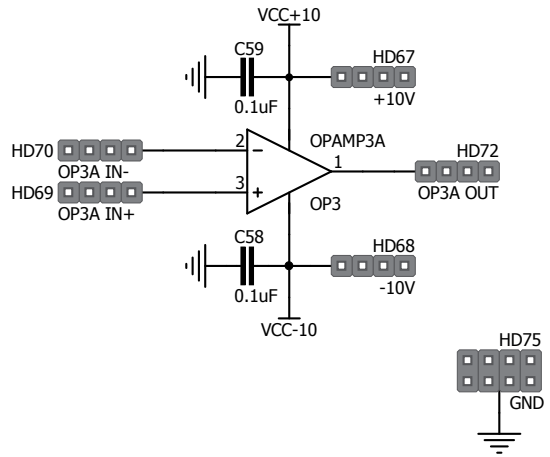


Figure D.5: OP-Amp 3A can be used in unity gain configuration or any other custom configuration

OP AMP TYPE III - B - BASIC

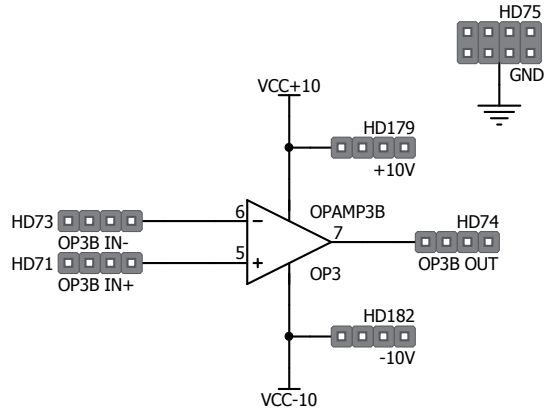


Figure D.6: OP-Amp 3B can be used in unity gain configuration or any other custom configuration

ANALOG MULTIPLIER - SET I

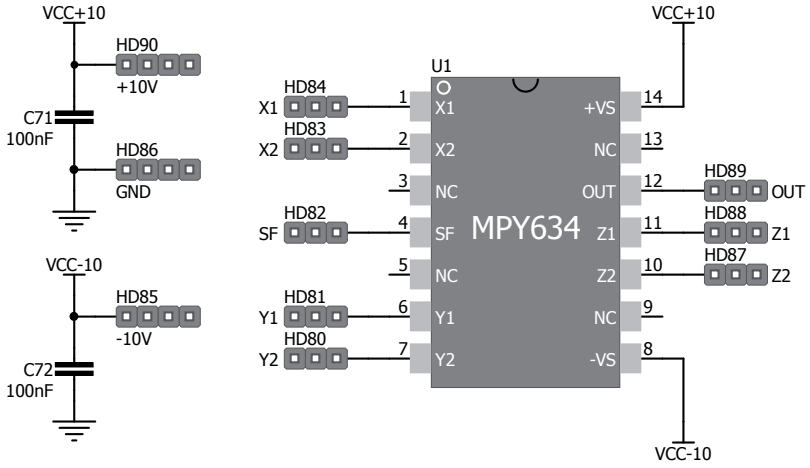


Figure D.7: Connections for analog multiplier MPY634 - SET I

ANALOG MULTIPLIER - SET II

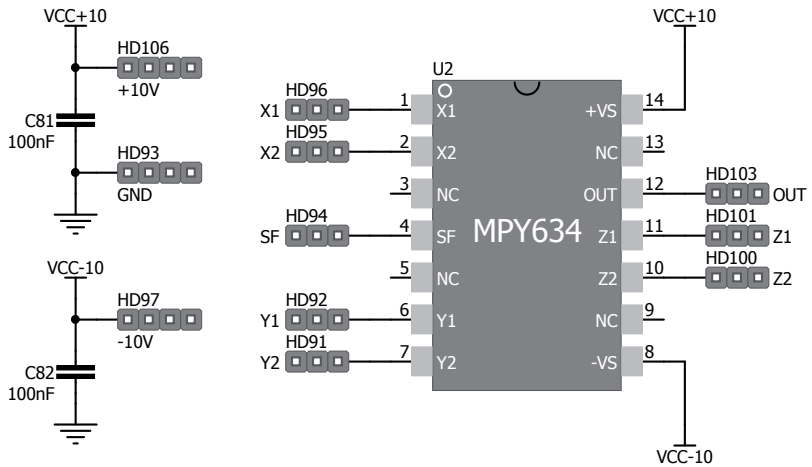


Figure D.8: Connections for analog multiplier MPY634 - SET II

ANALOG MULTIPLIER - SET III

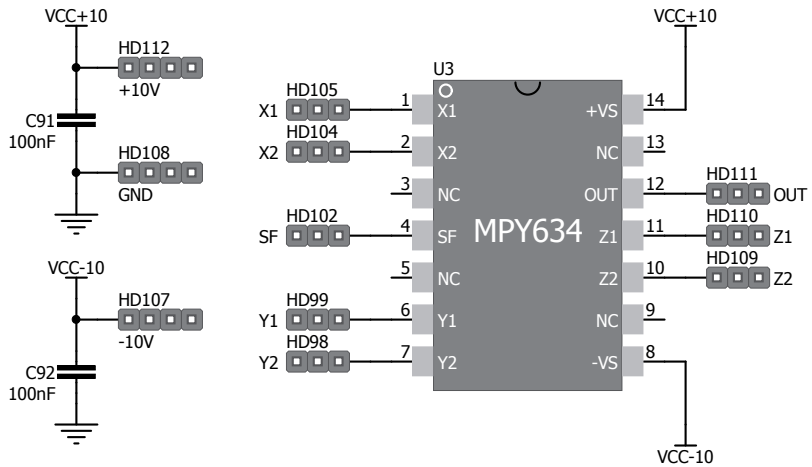


Figure D.9: Connections for analog multiplier MPY634 - SET III

DAC I

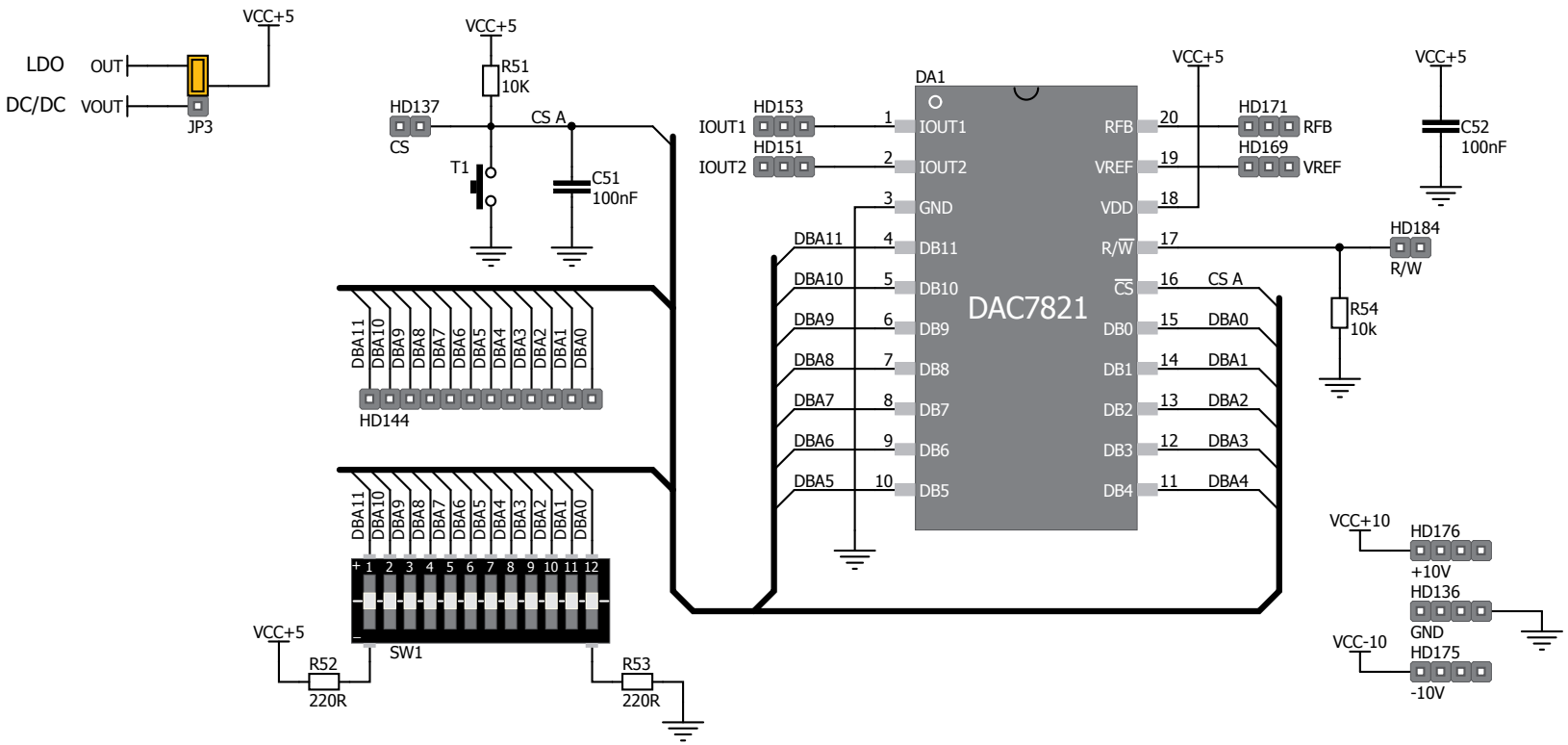


Figure D.10: connections for analog-to-digital converter DAC7821 - DAC I

DAC II

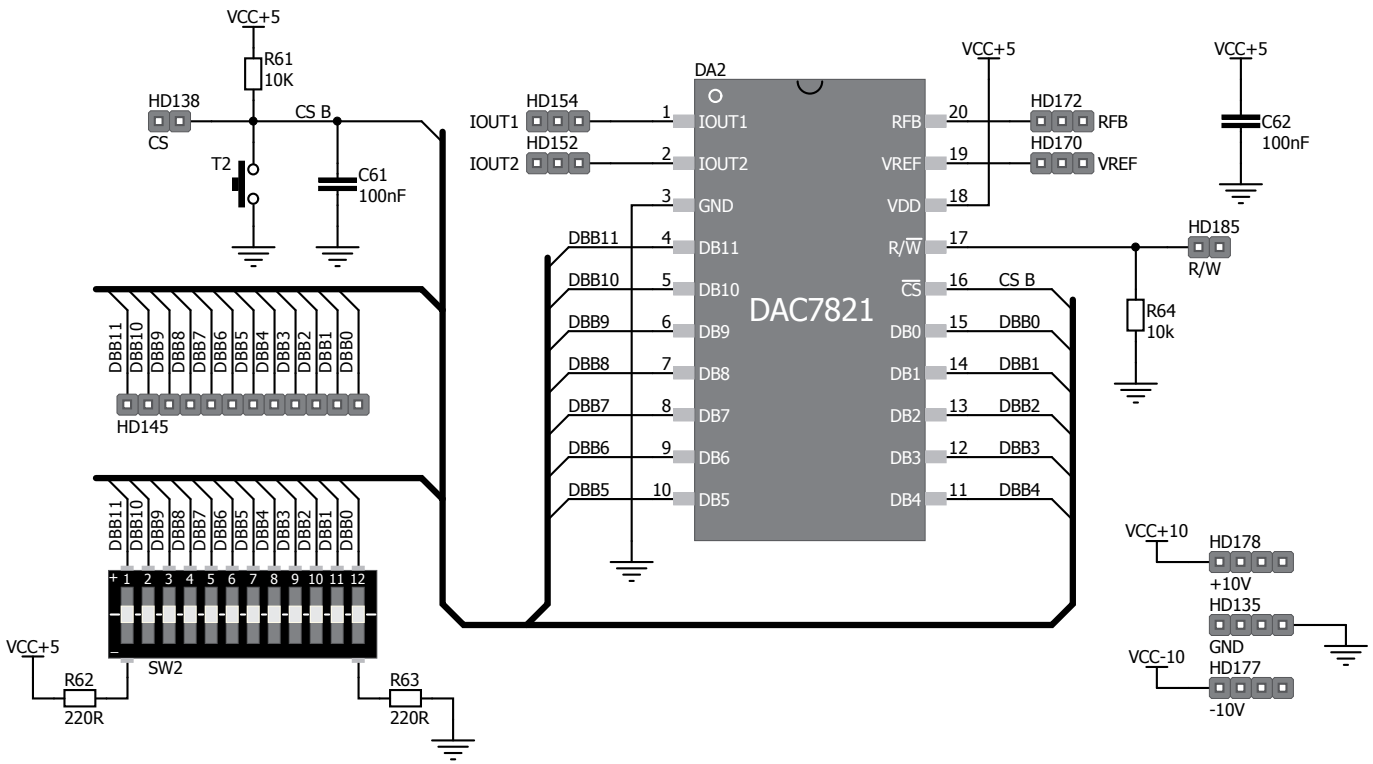


Figure D.11: connections for analog-to-digital converter DAC7821 - DAC II

DC/DC CONVERTER

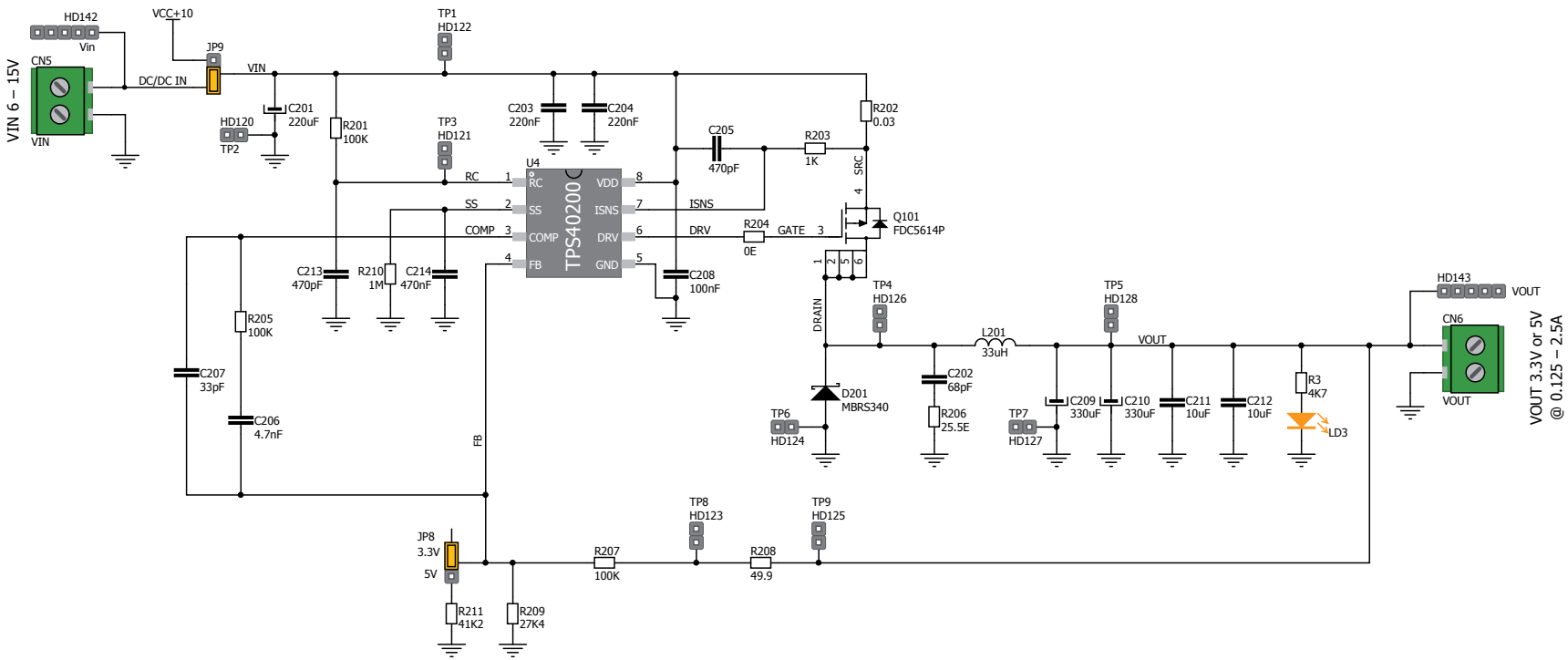


Figure D.12: Connections for TPS40200 Evaluation step-down DC/DC converter

LDO REGULATOR

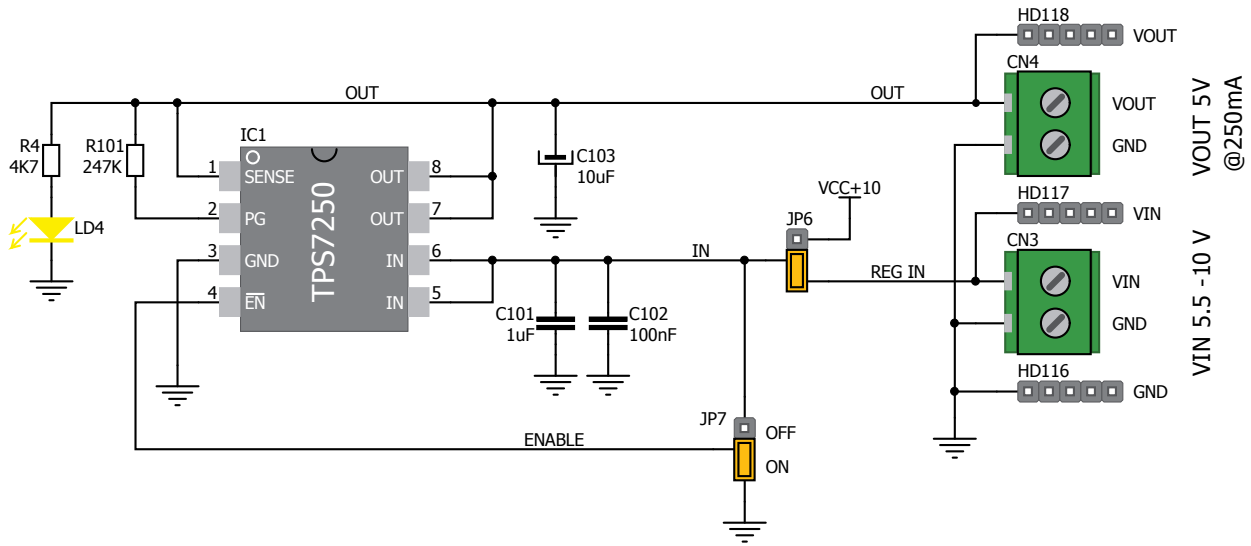


Figure D.13: Connections for TP7250 low-dropout linear voltage regulator

TRANSISTOR SOCKET (MOSFET)

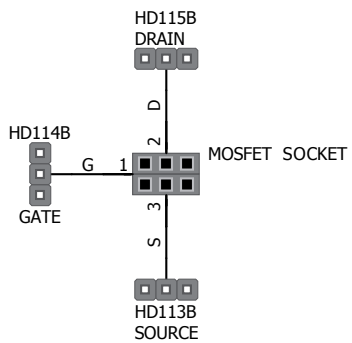


Figure D.14: MOSFET socket

TRANSISTOR SOCKET (BJT)

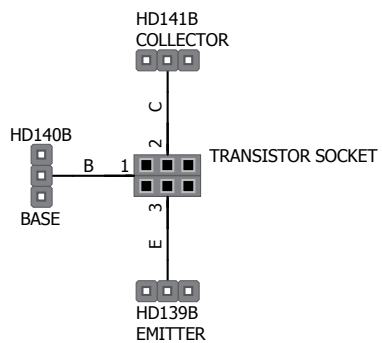


Figure D.15: Bipolar Junction Transistor socket

DIODES

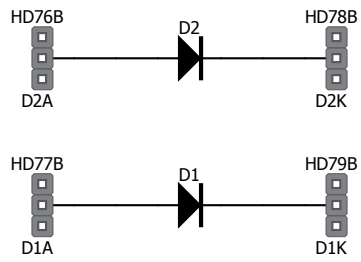


Figure D.16: Diode sockets

TRIMMERS

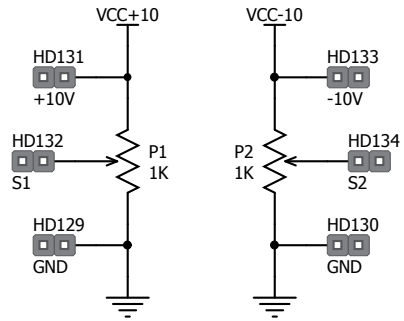


Figure D.17: Trimmer-potentiometers

POWER SUPPLY

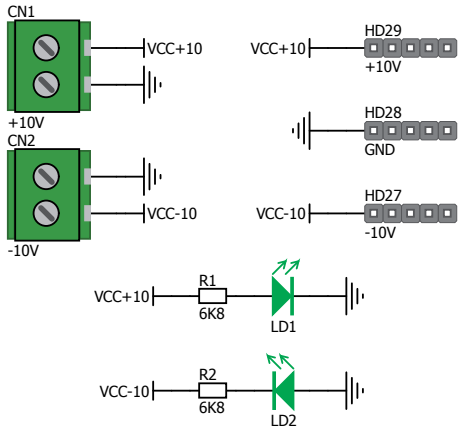


Figure D.18: Main power supply

GENERAL PURPOSE AREA

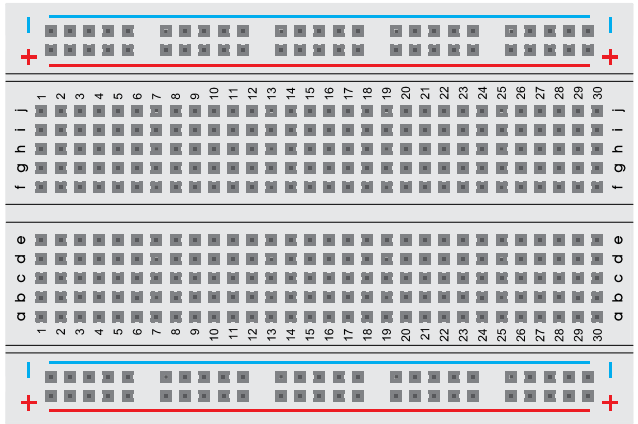


Figure D.19: General purpose area (2.54mm / 100mills pad spacing)

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Texas Instruments

Analog System Lab Kit PRO MANUAL

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Special Thanks to
Harmanpreet Singh
for his help in performing the additional experiments
(Experiments 11-14) included in the new release of ASLK Pro.

Publisher
MikroElektronika Ltd.
www.mikroe.com

June 2012.

Analog System Lab Kit PRO Manual
ver. 1.03b