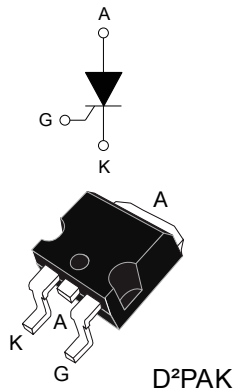



40 A 1200 V automotive grade thyristor (SCR) in D²PAK



Features

- AEC-Q101 qualified 
- High junction temperature: 150 °C
- AC off state voltage: +/- 1200 V
- Nominal on-state RMS current: 40 A_{RMS}
- High EFT noise immunity: 1000 V/μs
- Max. gate triggering current: 50 mA
- ECOPACK2 compliant component

Application

- On board charger
- Capacitor discharge
- Overvoltage crowbar protection
- Power supplies
- AC switches
- Solid state relays

Description

The **TN4050HP-12GY-TR** is an automotive grade SCR thyristor designed for applications such as automotive on board and stationary battery chargers.

This SCR thyristor, rated for a 40 A RMS power switching, offers superior performances in peak voltage robustness up to 400 V sine wave pulse. Its key features allow the design of functions such as a 56 A RMS AC switch and a 50 A AC-DC controlled rectifier-bridge.

The **TN4050HP-12GY-TR** is available in D²PAK surface mount package, ideal for automatic assembly lines.

Product status

TN4050HP-12GY-TR

Product summary

I_{T(RMS)}	40 A
V_{DRM}/V_{RRM}	1200 V
V_{DSM}/V_{RSM}	1400 V
I_{GT}	50 mA
T_j	-40 to 150 °C

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter		Value	Unit
$I_{T(RMS)}$	RMS on-state current (180 ° conduction angle)		40	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)			
I_{TSM}	Non repetitive surge peak on-state current, $V_R = 0$ V	$t_p = 8.3$ ms	440	A
		$t_p = 10$ ms		
I^2t	I^2t value for fusing	$t_p = 10$ ms	800	A^2s
di/dt	$I_G = 2 \times I_{GT}$, $tr \leq 100$ ns Critical rate of rise of on-state current	$f = 50$ Hz	200	$A/\mu s$
V_{DRM} / V_{RRM}	Repetitive off-state voltage		1200	V
V_{DSM} / V_{RSM}	Non repetitive surge peak off-state voltage	$t_p = 10$ ms	1400	V
V_{GM}	Peak forward gate voltage	$t_p = 20$ μs	10	V
I_{GM}	Peak forward gate current	$t_p = 20$ μs	8	A
V_{RGM}	Maximum peak reverse gate voltage		5	V
$P_{G(AV)}$	Average gate power dissipation		1	W
T_{stg}	Storage junction temperature range			-40 to +150 °C
T_j	Operating junction temperature			-40 to +150 °C

Table 2. Electrical characteristics ($T_j = 25$ °C unless otherwise specified)

Symbol	Test Conditions		Value	Unit
I_{GT}	$V_D = 12$ V, $R_L = 33$ Ω	Min.	10	mA
		Max.	50	
V_{GT}		Max.	1.3	V
I_{GD}	$V_D = 800$ V, $R_L = 3.3$ Ω	$T_j = 150$ °C	Min. 3	mA
V_{GD}	$V_D = 800$ V, $R_L = 3.3$ Ω	$T_j = 150$ °C	Min. 0.2	V
I_H	$I_T = 500$ mA, gate open		Max. 100	mA
I_L	$I_G = 1.2 \times I_{GT}$		Max. 125	mA
dV/dt	$V_D = 800$ V, gate open	$T_j = 150$ °C	Min. 1000	$V/\mu s$

Table 3. Timing Parameters

Symbol	Test Conditions		Value	Unit
t_{gt}	$I_T = 80$ A, $V_D = 800$ V, $I_G = 100$ mA, $dI_G/dt = 0.2$ A/ μs		Typ. 1	μs
t_q	$I_{TM} = 25$ A, $V_D = 800$ V, $dI_T/dt = 10$ A/ μs , $V_R = 75$ V, $dV_D/dt = 20$ V/ μs , $t_p = 100$ μs	$T_j = 150$ °C	Typ. 150	μs

Table 4. Static Characteristics

Symbol	Test Conditions		Value	Unit
V_{TM}	$I_{TM} = 80$ A, $t_p = 380$ μs	$T_j = 25$ °C	Max. 1.55	V

Symbol	Test Conditions			Value	Unit
V_{TO}	On-state threshold voltage	$T_j = 150\text{ °C}$	Max.	0.83	V
R_D	On-state dynamic resistance	$T_j = 150\text{ °C}$	Max.	10	mΩ
I_{DRM}/I_{RRM}	$V_D = V_{DRM}, V_R = V_{RRM}$	$T_j = 25\text{ °C}$	Max.	5	μA
		$T_j = 125\text{ °C}$		0.9	mA
		$T_j = 150\text{ °C}$		6	mA
I_{DSM}/I_{RSM}	$V_D = V_{DSM}, V_R = V_{RSM}$	$T_j = 25\text{ °C}$	Max.	10	μA

Table 5. Thermal parameters

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Max.	0.4
$R_{th(j-a)}$	Junction to ambient (DC, $S_{CU} = 2.5\text{ cm}^2$, $e_{CU} = 70\text{ μm}$)	Typ.	45

1.1 Characteristics (curves)

Figure 1. Maximum average power dissipation versus average on-state current

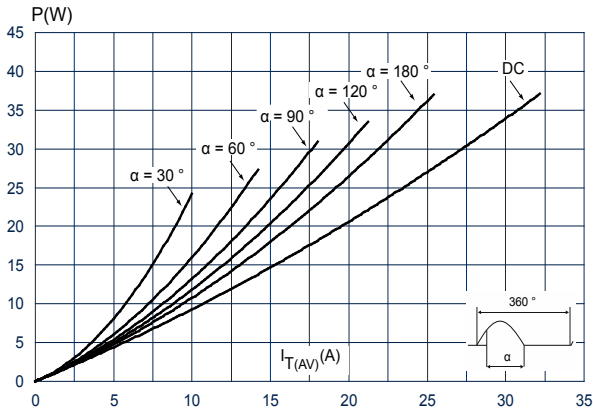


Figure 2. Average and D.C. on-state current versus case temperature

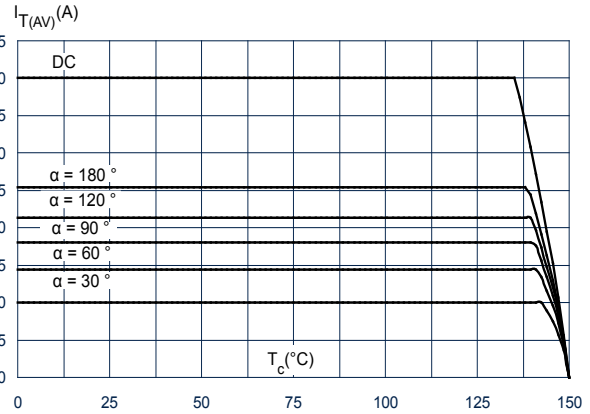


Figure 3. Average and D.C. on-state current versus ambient temperature

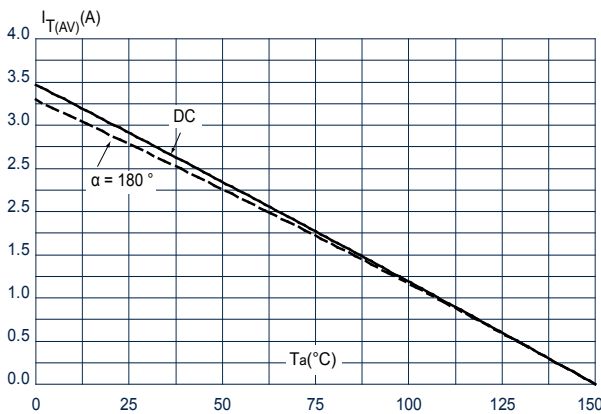


Figure 4. On-state characteristics (maximum values)

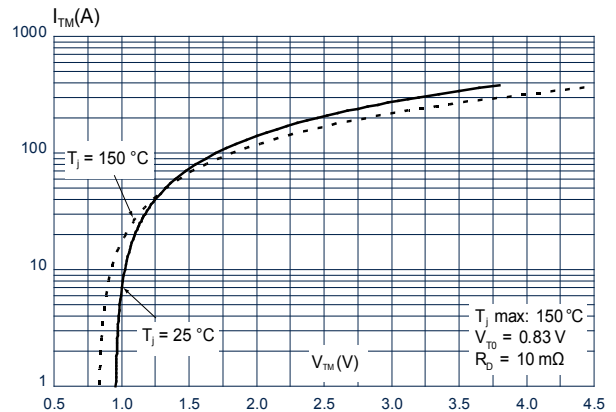


Figure 5. Surge peak on-state current versus number of cycles

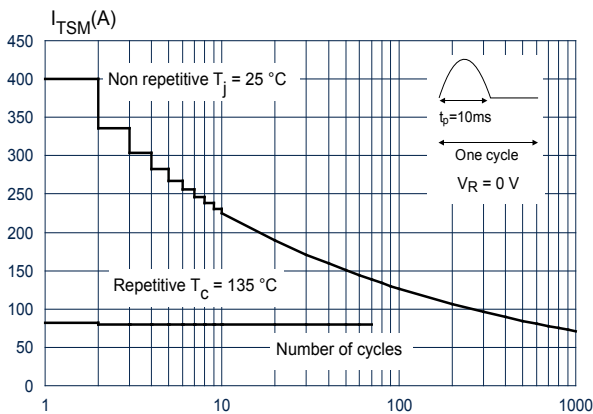


Figure 6. Non repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms

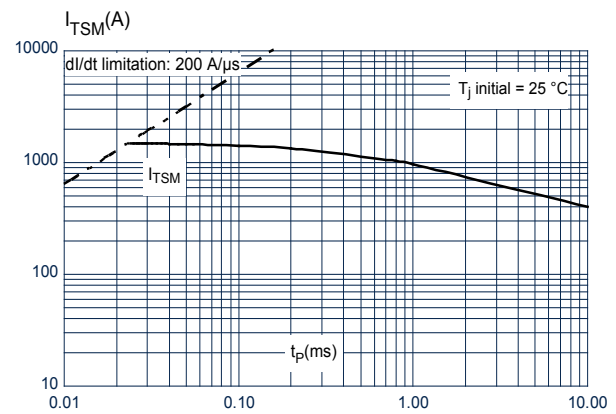
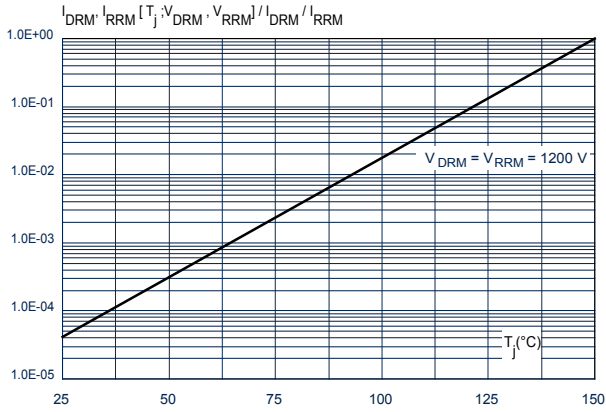
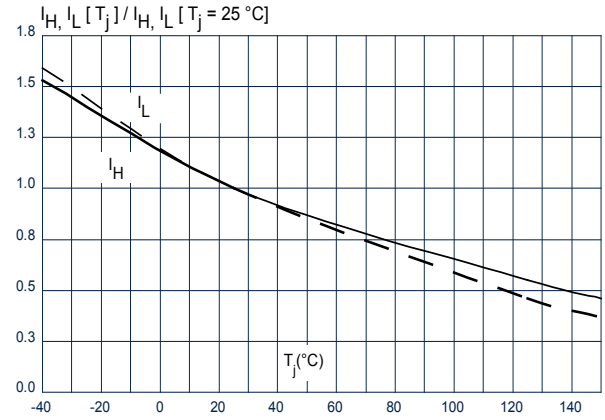
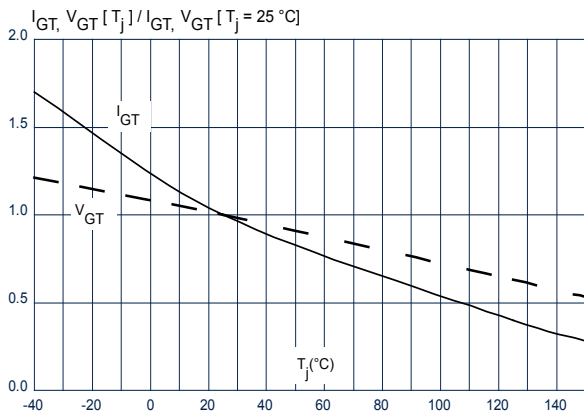
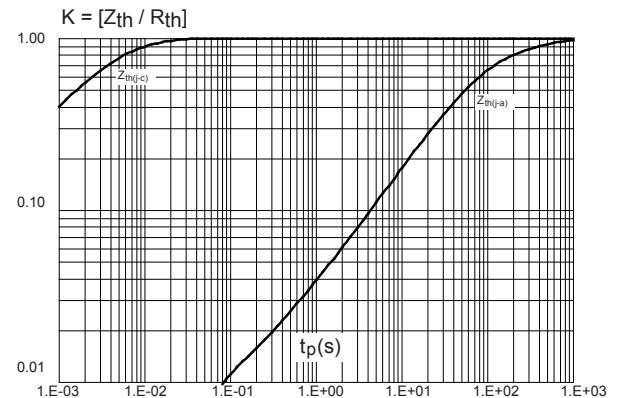
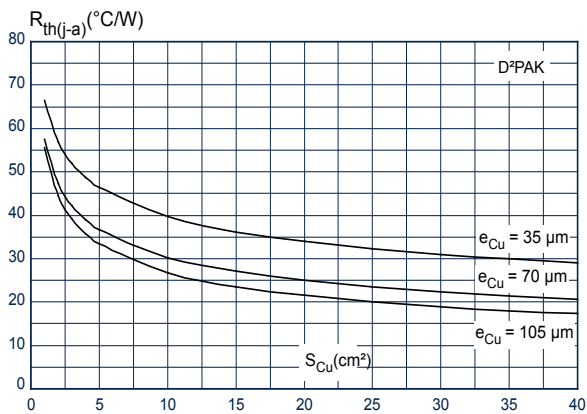
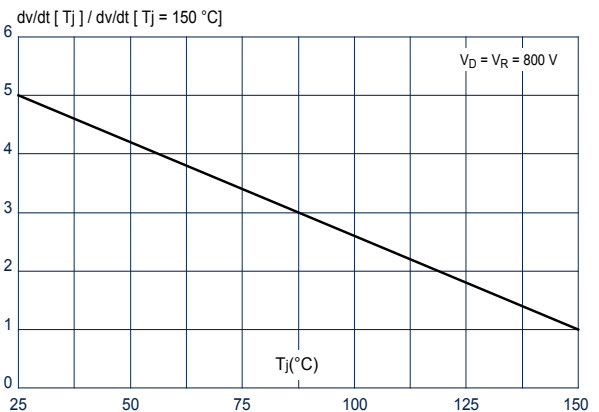


Figure 7. Relative variation of leakage current versus junction temperature for different values of blocking voltage (typical values)

Figure 8. Relative variation of holding and latching current versus junction temperature (typical values)

Figure 9. Relative variation of gate trigger current and gate voltage versus junction temperature (typical values)

Figure 10. Relative variation of thermal impedance junction to case and junction to ambient versus pulse duration

Figure 11. Thermal resistance junction to ambient versus copper surface under tab (typical values, epoxy printed board FR4) (D²PAK)

Figure 12. Relative variation of static dV/dt immunity versus junction temperature


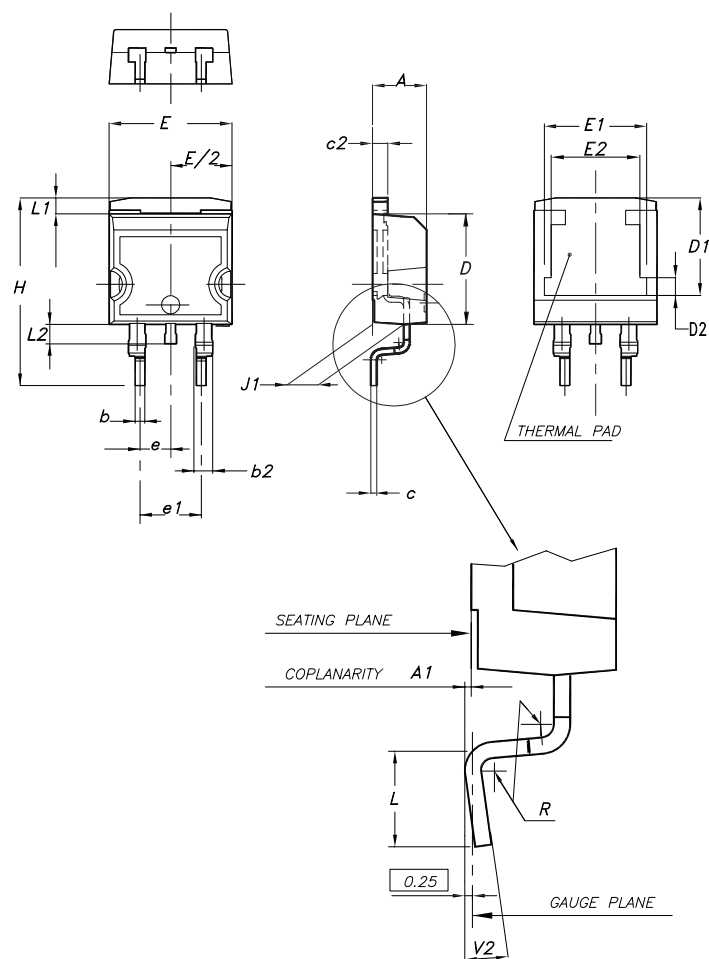
2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 D²PAK package information

- Epoxy meets UL94, V0.
- Cooling method: by conduction (C)

Figure 13. D²PAK package outline

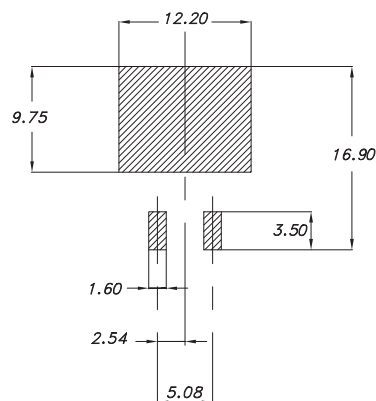


Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

Table 6. D²PAK package mechanical data

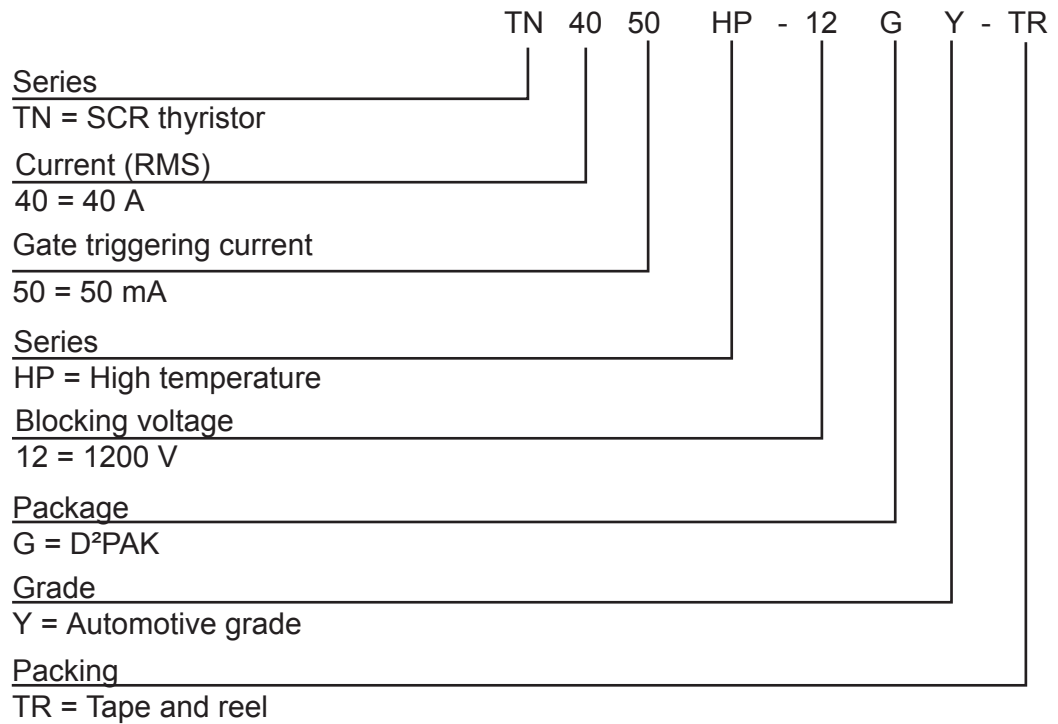
Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.1732		0.1811
A1	0.03		0.23	0.0012		0.0091
b	0.70		0.93	0.0276		0.0366
b2	1.14		1.70	0.0449		0.0669
c	0.45		0.60	0.0177		0.0236
c2	1.23		1.36	0.0484		0.0535
D	8.95		9.35	0.3524		0.3681
D1	7.50	7.75	8.00	0.2953	0.3051	0.3150
D2	1.10	1.30	1.50	0.0433	0.0511	0.0591
E	10		10.40	0.3937		0.4094
E1	8.30	8.50	8.70	0.3267	0.3346	0.3425
E2	6.85	7.05	7.25	0.2697	0.2776	0.2854
e		2.54			0.1000	
e1	4.88		5.28	0.1921		0.2079
H	15		15.85	0.5906		0.6240
J1	2.49		2.69	0.0980		0.1059
L	2.29		2.79	0.0902		0.1098
L1	1.27		1.40	0.0500		0.0551
L2	1.30		1.75	0.0512		0.0689
R		0.4			0.0157	
V2	0°		8°	0°		8°

1. Dimensions in inches are given for reference only

Figure 14. D²PAK recommended footprint (dimensions are in mm)


0079457_Rev28_footprint

3 Ordering information

Figure 15. Ordering information scheme

Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN4050HP-12GY-TR	TN40P12YB	D ² PAK	1.38 g	1000	Tape and reel 13"

Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Dec-2021	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2021 STMicroelectronics – All rights reserved