19-1448; Rev 4; 11/08

MAXIM

Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

General Description

The MAX4473 PA power control IC is intended for closed-loop bias control of GSM power amplifiers. The device facilitates accurate control of the current delivered to the power amplifier (PA) through a control voltage. The error amplifier senses the voltage drop across an external current-sense resistor placed between the supply and the PA. The output of the error amplifier adjusts the PA gain until the current is proportional to the power control voltage applied to the MAX4473. This unique topology is useful in time-division-multiple-access (TDMA) systems, such as GSM, where accurate transmit burst shaping and power control is required. User-selectable current sensing and gain setting resistors maximize flexibility.

The MAX4473 operates from a single 2.7V to 6.5V supply and typically draws 1.2mA of supply current. The error amplifier has a common-mode range that extends from 1V to V_{CC}. The power control input and error amplifier outputs swing rail-to-rail. A low-power shutdown mode reduces supply current to less than 1µA and activates an on-board active pull-down at the error amplifier output. Fast enable/disable times of 0.9µs reduce average power consumption without compromising dynamic performance. The MAX4473 is available in a space-saving 8-pin µMAX® package.

Applications

GSM Cellular Phones

Cordless Phones

Precision Current Control

High-Frequency Servo Loops

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features

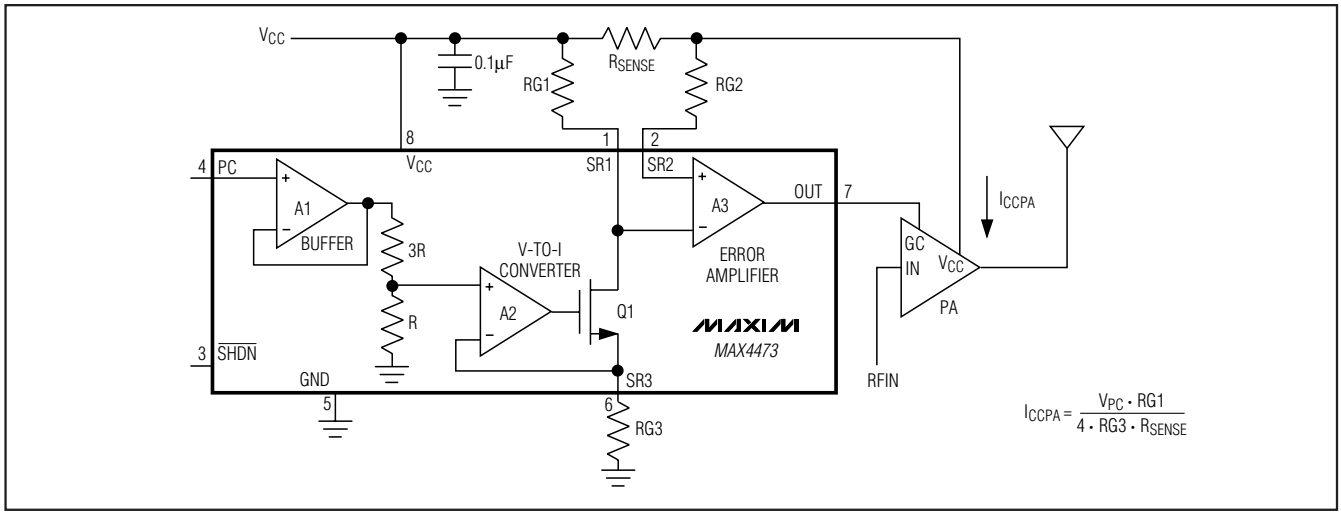
- **Optimized for GSM Timing Requirements**
- **2.7V to 6.5V Single-Supply Operation**
- **1.2mA Supply Current**
- **≤ 1µA Supply Current in Shutdown Mode**
- **Guaranteed 1.5µs Enable/Disable Times**
- **Active Output Pull-Down in Shutdown Mode**
- **Rail-to-Rail Error Amplifier Output**
- **Rail-to-Rail Power Control Input**
- **Output Drive Capability—500Ω and 300pF Loads**
- **1V to V_{CC} Current Sense Input Common-Mode Voltage Range**
- **No Phase-Reversal for Common-Mode Voltage from 0 to V_{CC}**
- **External Current Sensing and Gain Setting Resistors Maximize Flexibility**
- **Available in a Space-Saving 8-Pin µMAX**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4473EUA	-40°C to +85°C	8 µMAX
MAX4473ESA	-40°C to +85°C	8 SO

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND 7V
SR1, SR2, SR3, PC, $\overline{SHDN}$, OUT to GND .....-0.3V to (V_{CC} + 0.3V)
SR1 to SR3 .....0 to V_{CC}
OUT and SR3 Short-Circuit Duration to V_{CC} or GND .....Continuous
Current into Any Pin .....±50mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.10mW/°C above +70°C) 330mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature. .....+150°C
Storage Temperature Range. .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6.5V, $\overline{SHDN}$ > 2.4V, MAX4473 test circuit, RG1 = RG2 = 1kΩ ±1%, RG3 = 2.5kΩ ±1%, R_{SENSE} = 100Ω ±1%, R_L = 10kΩ, C_L = 300pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 6.0V, V_{PC} = 1.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage			2.7		6.5	V
Supply Current	V_{PC} = 0			1.2	2	mA
Shutdown Supply Current	$\overline{SHDN}$ < 0.4V, R_L = 10Ω			0.03	1	µA
$\overline{SHDN}$ Input High Voltage			2.4			V
$\overline{SHDN}$ Input Low Voltage					0.4	V
$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 0 to V_{CC}				±0.5	µA
ERROR AMPLIFIER						
SR1, SR2 Input Offset Voltage	1V < V_{SR1}, V_{SR2} < V_{CC}			±0.5	±2	mV
	1V < V_{SR1}, V_{SR2} < V_{CC} at +25°C			±0.5	±1	
SR1, SR2 Input Offset Voltage Drift	1V < V_{SR1}, V_{SR2} < V_{CC}			10		µV/°C
SR1, SR2 Input Common-Mode Voltage Range	Inferred from CMRR test; V_{SR2} = GND (Note 2)		1		V_{CC}	V
SR1, SR2 Input Bias Current	1V < V_{SR1}, V_{SR2} < V_{CC}, V_{PC} = GND, SR3 = unconnected			±0.04	±1	µA
SR1, SR2 Input Bias Offset Current	1V < V_{SR1}, V_{SR2} < V_{CC}, V_{PC} = GND, SR3 = unconnected			±0.001	±0.2	µA
SR1, SR2 Shutdown Leakage Current	$\overline{SHDN}$ < 0.4V, V_{SR1} = V_{SR2} = V_{CC}			±0.001	±0.5	µA
Common-Mode Rejection Ratio	1V < V_{SR1}, V_{SR2} < V_{CC}, V_{PC} = GND	V_{CC} = 2.7V	65	85		dB
		V_{CC} = 6.5V	75	95		
Power-Supply Rejection Ratio	2.7V < V_{CC} < 6.5V, V_{PC} = GND		80	90		dB
Large-Signal Gain	R_L = 10kΩ to V_{CC} / 2	V_{CC} = 6.5V, 0.3V < V_{OUT} < 6V	80	130		dB
		V_{CC} = 2.7V, 0.3V < V_{OUT} < 2.4V	80	125		
	R_L = 500Ω to V_{CC} / 2	V_{CC} = 6.5V, 0.7V < V_{OUT} < 5.5V	80	130		
		V_{CC} = 2.7V, 0.7V < V_{OUT} < 2.2V	80	120		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 6.5V, $\overline{SHDN}$ > 2.4V, MAX4473 test circuit, RG1 = RG2 = 1kΩ ±1%, RG3 = 2.5kΩ ±1%, R_{SENSE} = 100Ω ±1%, R_L = 10kΩ, C_L = 300pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 6.0V, V_{PC} = 1.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	R_L = 10Ω to V_{CC} / 2	0.15		V_{CC} - 0.15	V
	R_L = 500Ω to V_{CC} / 2	0.5		V_{CC} - 0.5	
Output Current Limit	V_{OUT} = V_{CC} / 2		20		mA
Gain-Bandwidth Product	R_L = 10Ω, C_L = 300pF, f_o = 10kHz		2		MHz
Phase Margin	R_L = 10Ω, C_L = 300pF		60		degrees
Slew Rate	Measured from 30% to 70% of V_{OUT}, R_L = 10Ω, C_L = 300pF		1.8		V/µs
Capacitive-Load Stability	No sustained oscillations (Note 3)	0		300	pF
Enable/Disable Time	From 50% of $\overline{SHDN}$ edge to V_{OUT} = 1V, V_{PC} = 2V		0.9	1.5	µs
GAIN CONTROL BUFFER AND V-TO-I CONVERTER					
PC Input Bias Current	GND < V_{PC} < V_{CC} - 0.15V		±0.04	±1	µA
SR3 Output Current Limit	V_{PC} < 2.55V, SR1 = SR2 = V_{CC}	0.750	4		mA
V_{PC} to VRG1 Ratio	Measure voltage across RG1, 0.3V < V_{PC} < 2.55V (Note 4)	0.095	0.1	0.105	V/V
PC Input Bandwidth	Bandwidth from V_{PC} to V_{RG1}		2		MHz

Note 1: Limits over temperature are guaranteed by design.

Note 2: No output phase-reversal for input common-mode voltage range from GND to V_{CC}. Common-mode range limited by voltage drop across Q1 and RG3.

Note 3: Guaranteed by design.

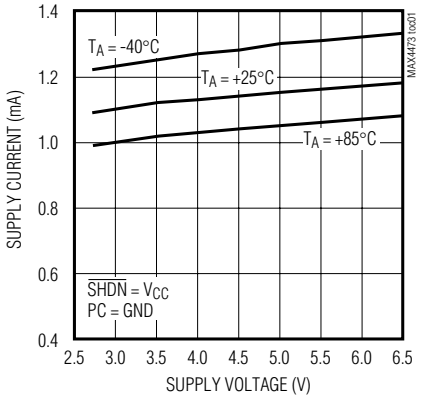
Note 4: Error dependent on tolerance of RG1, RG2, and RG3. Specified with 0.1% tolerance resistors.

Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

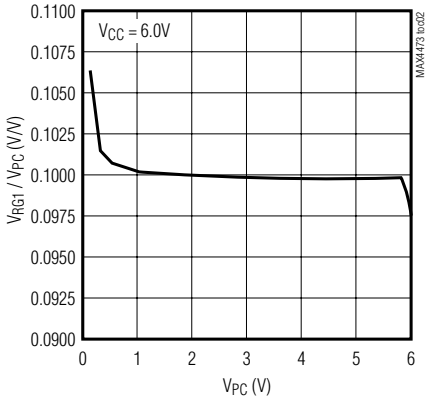
Typical Operating Characteristics

(See *Test Circuit*, T_A = +25°C, unless otherwise noted.)

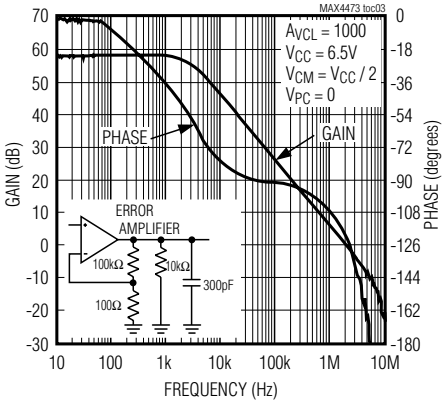
SUPPLY CURRENT vs. SUPPLY VOLTAGE



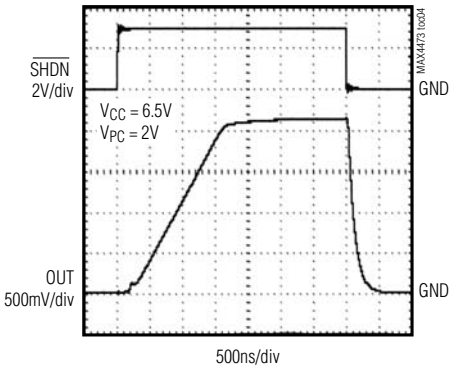
VRG1 / VPC RATIO vs. VPC RESPONSE



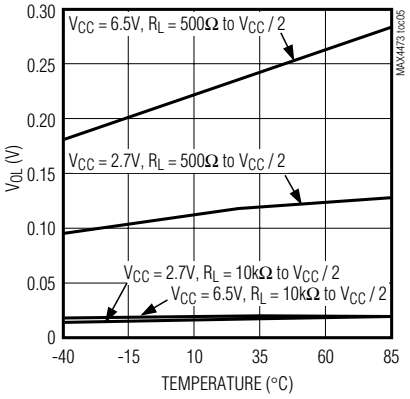
ERROR-AMPLIFIER RESPONSE



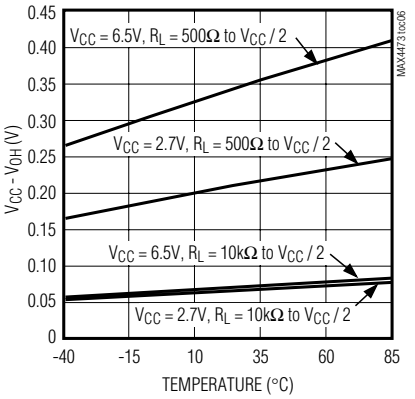
ENABLE/DISABLE TIME



ERROR-AMPLIFIER OUTPUT LOW VOLTAGE vs. TEMPERATURE



ERROR-AMPLIFIER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	SR1	Inverting Input of Error Amplifier and Drain of V-to-I FET, Q1. Connect to supply side of current-sense resistor, R_{SENSE}, through gain resistor RG1.
2	SR2	Noninverting Input of Error Amplifier. Connect to load side of current-sense resistor, R_{SENSE}, through gain resistor RG2. Set RG2 equal to RG1.
3	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to disable all amplifiers, pull OUT to GND, set the gate-to-source voltage of the V-to-I FET (Q1) to 0, and reduce supply current to less than 1µA. Drive high or connect to V_{CC} for normal operation.
4	PC	Power Control Input. Apply a voltage to PC to set a DC current through the sense resistor to control PA bias.
5	GND	Ground
6	SR3	Inverting Input to V-to-I Converter and Source of V-to-I FET, Q1. Connect to ground through gain resistor RG3.
7	OUT	Output of Error Amplifier. Connect to gain control pin of power amplifier in bias control applications.
8	VCC	+2.7V to +6.5V Voltage Supply Input. Bypass to ground with a 0.1µF capacitor.

Detailed Description

The MAX4473 is a voltage-controlled, unidirectional, high-side current setting amplifier for applications where accurate control of PA supply current is desired. This device is intended for wireless TDMA based systems (GSM, DECT), where tight restrictions over the PA's transmit burst and output power require closed-loop control over the PA's output power. When used with a PA, the MAX4473 functions as a voltage-controlled constant current source, accurately setting PA supply current by varying the gain of the PA. If you know the output power versus supply current profile for the PA, you can set the PA's output power by controlling the amount of supply current delivered to the PA.

The MAX4473 is composed of an input buffer (A1), a voltage-to-current converting amplifier (A2), and a rail-to-rail output error amplifier (A3) (see *Typical Operating Circuit*). External gain and sense resistors allow programmability for a wide range of applications.

In the *Typical Operating Circuit*, PA supply current flows from the system supply, through the external current-sense resistor (R_{SENSE}), to the PA. The rail-to-rail outputs of the error amplifier, A3, adjust the gain of the PA until the voltage drop across R_{SENSE} equals the voltage drop across external gain resistor, RG1. The voltage drop across RG1 sets the voltage drop across R_{SENSE}, with a larger voltage drop resulting in more current delivered to the PA. The voltage drop across RG1 is set by A1, A2, and the V-to-I FET, Q1. A voltage applied to the PC input of the input buffer is divided by four by a resistor-divider network. A2 forces its inverting input and the source of Q1 to V_{PC} / 4, thus setting a voltage across RG3. The resulting current through RG3 sets the current through RG1. This unique architecture allows the supply current to be set independent of supply voltage. Set PA supply current according to the following equation:

$$I_{CCPA} = (V_{PC} \cdot RG1) / (4 \cdot R_{SENSE} \cdot RG3)$$

Shutdown Mode

When $\overline{SHDN}$ is a logic-level low ($\overline{SHDN}$ < 0.4V), amplifiers A1, A2, and A3 are off, Q1 is turned off, and the output of A3 is actively pulled to ground with an N-channel FET. Supply current is reduced to less than 1µA in shutdown mode. Typical power-up time is 0.9µs and typical power-down time is 0.3µs, using the MAX4473 test circuit.

Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

Applications Information

Gain Resistor Selection (RG1, RG2, RG3)

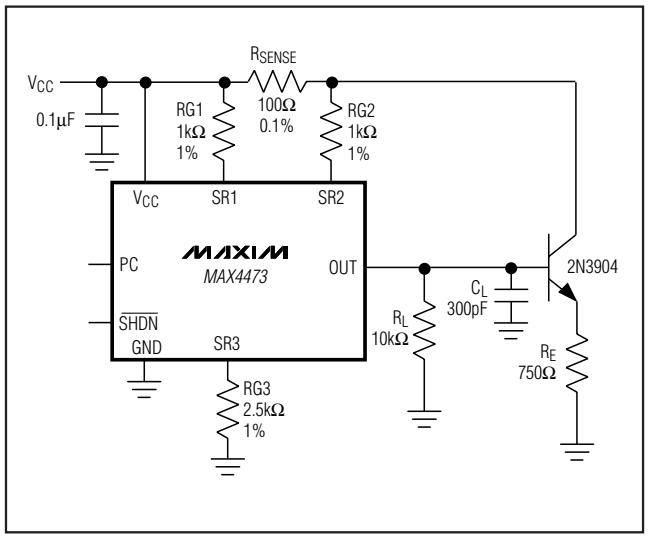
For proper operation, do not make the value of external gain resistors RG1 and RG2 larger than twice the value of RG3. In most practical applications, choose RG1 smaller than RG3 to limit the voltage drop over RG1 and RSENSE. A large voltage drop over RSENSE substantially reduces the voltage applied to the PA, thus reducing PA output power. Set RG2 equal to RG1 to compensate for the input bias currents of A3. Recommended values for RG3 are between 1kΩ and 10kΩ.

Sense Resistor Selection (RSENSE)

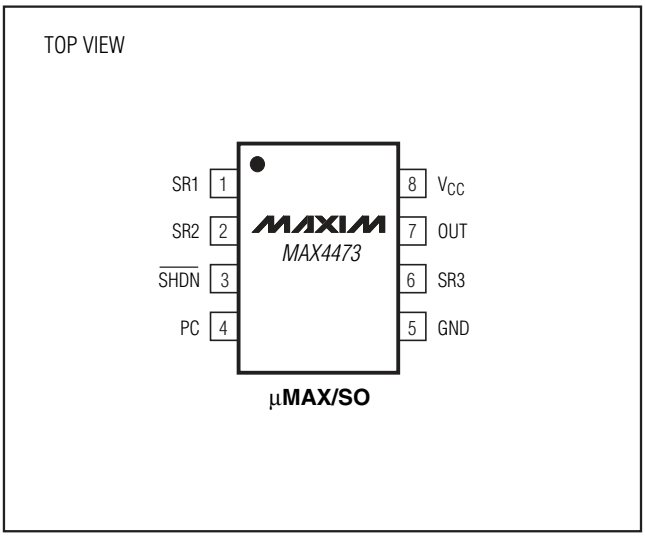
Choose RSENSE based on the following criteria:

- **Voltage Loss:** A high RSENSE value causes the power-source voltage to degrade through IR loss. For minimal voltage loss, use low RSENSE values.
- **Accuracy:** A high RSENSE value allows lower currents to be measured more accurately because input offset voltages become less significant when the sense voltage is larger. For best performance, select RSENSE to provide approximately 100mV of sense voltage for the full-scale current in each application.
- **Efficiency and Power Dissipation:** At high current levels, the I^2R losses in RSENSE are significant. Take this into consideration when choosing the resistor value and its power dissipation (wattage) rating. Also, the sense resistor's value may drift if it is allowed to heat up excessively.

Test Circuit



Pin Configuration



Chip Information

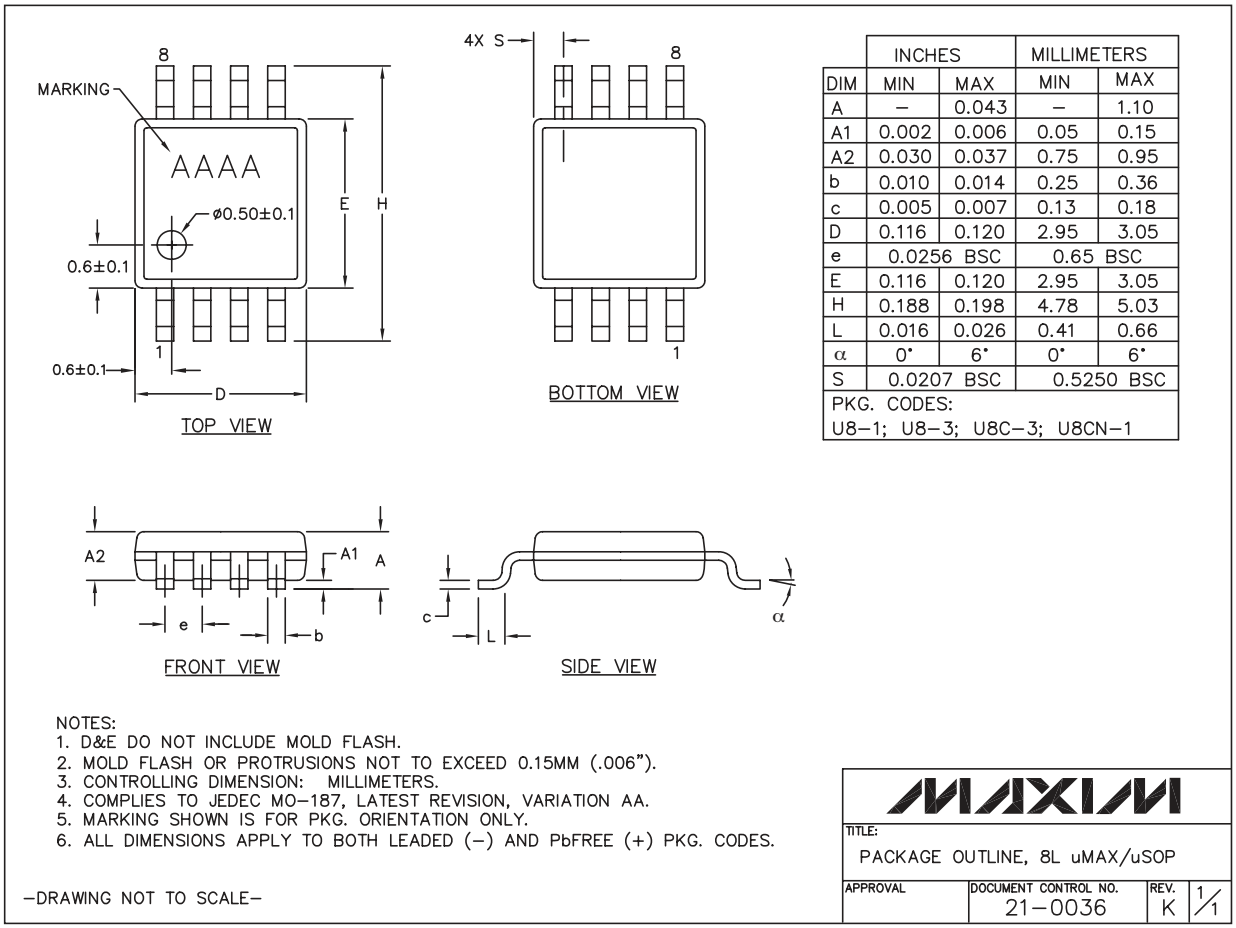
TRANSISTOR COUNT: 348

Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 µMAX	U8-1	**21-0036**
8 SO	S8-2	**21-0041**



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8-1; U8-3; U8C-3; U8CN-1

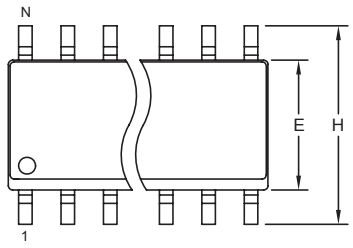
Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

SOICN .EPS

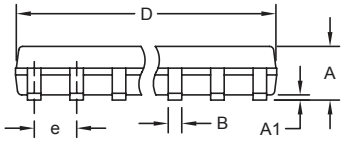
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



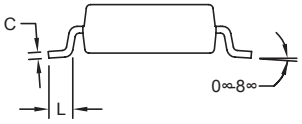
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Low-Cost, Low-Voltage, PA Power Control Amplifier for GSM Applications

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	11/08	Removed QFN package	1–9