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Evaluation Board for the ADP2442 36 V, 1 A, Synchronous, Step-Down DC-to-DC Regulator with External Clock Synchronization

FEATURES

Full featured evaluation board for the ADP2442
Configurable synchronous step-down dc-to-dc switching regulator
Operating voltage range: V_{IN} = 6 V to 36 V
Output voltage: 5 V or adjustable
1 A maximum load
Switching frequency: 500 kHz or adjustable switching frequency of 300 kHz to 1 MHz
Power saving mode at light load
Precision enabled input pin
Current limit protection
Power good output
SYNC/MODE pin for external synchronization or mode selection
53 mm × 53 mm board size

DOCUMENTS NEEDED

ADP2442 data sheet
UG-407 user guide

GENERAL DESCRIPTION

The ADP2442-EVALZ evaluation board is a complete, dc-to-dc switching regulator design based on the ADP2442, a configurable, 1 A, synchronous, step-down dc-to-dc regulator.

The ADP2442 is a synchronous, step-down dc-to-dc switching regulator that uses a current mode pulse-width modulation (PWM) control scheme. The ADP2442 can be configured for pulse skip mode at light load or forced PWM mode. The power switch and synchronous rectifier are integrated for minimal external part count and high efficiency. The ADP2442 is optimized for operation with small ferrite core inductors and ceramic capacitors to deliver the maximum output power per square millimeter of the printed circuit board (PCB) area.

The ADP2442-EVALZ is available with 5 V at a 1 A output, with a switching frequency set to 500 kHz. If needed, the ADP2442-EVALZ configuration can be modified by changing the values of the appropriate passive components.

Complete specifications for the ADP2442 device can be found in the ADP2442 data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

ADP2442-EVALZ

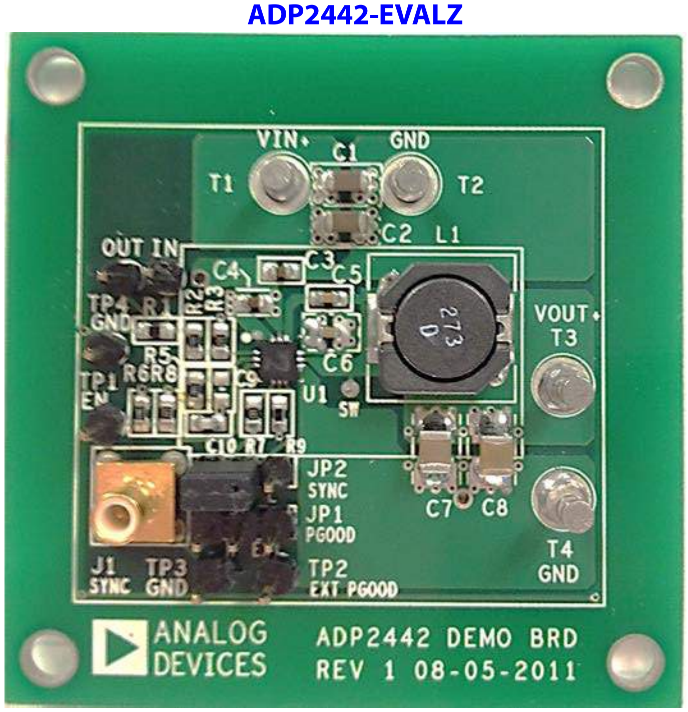

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Figure 1.

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REVISION HISTORY

11/12—Revision 0: Initial Version

USING THE EVALUATION BOARD

POWERING UP THE EVALUATION BOARD

The ADP2442-EVALZ evaluation board is provided fully assembled and tested. Before applying power to the evaluation board, follow the procedures in the following sections.

Input Power Source

The power source voltage must not exceed 36 V, the maximum operation input voltage of the ADP2442.

Ensure that the power source is switched off before connecting it to the ADP2442-EVALZ evaluation board. Connect the positive terminal of the power source to the evaluation board V_{IN} terminal (T1), and the negative terminal of the power source to the evaluation board GND terminal (T2). If the power source includes an ammeter, connect the ammeter in series with the input source voltage. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (−) of the ammeter to the evaluation board V_{IN} terminal (T1), and the negative lead (−) of the power source to the evaluation board GND terminal (T2).

Output Load

Ensure that the evaluation board is switched off before connecting the load. Connect the load directly to the evaluation board, with the positive (+) load connection to the VOUT terminal (T3) and the negative (−) load connection to the PGND terminal (T4). If an ammeter is used, connect it in series with the load: connect the positive (+) ammeter terminal to the evaluation board VOUT terminal (T3), the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board PGND terminal (T4).

When the load is connected, ensure that it is set to the proper current before powering the ADP2442-EVALZ evaluation board. Before connecting a load to the output of the evaluation board, ensure that the output voltage does not exceed the maximum operating voltage range of the load.

Enabling and Disabling the DC-to-DC Switching Regulator

In the evaluation board, a voltage divider is used to generate an enable signal for the IC. As soon as voltage is applied to VIN (24 V), IC is enabled.

Alternatively, the TP1 (EN) header is available to enable and disable the evaluation board. To enable the output, connect the TP1 header to the VIN supply or to an external voltage source. To disable the output, connect the TP1 header to the GND.

PGOOD Signals

When the output is enabled and the output voltage, V_{OUT}, is in regulation, the logic signal at the PGOOD test point is high. In a typical application, a pull-up resistor from the PGOOD pin to the external supply is used to generate this logic signal.

On the evaluation board, the pull-up resistor (R7) is available to connect to the external supply through the jumper (JP1). The TP2 test point is available to connect the external supply of 5 V.

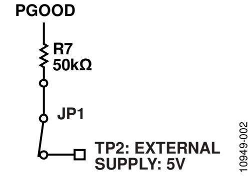


Figure 2. PGOOD Signal

SYNC/MODE Pin

The SYNC/MODE pin is a multifunctional pin. When the SYNC/MODE pin is connected to VCC or a high logic, the PWM mode is enabled. When the SYNC pin is connected to AGND, the pulse skip mode is enabled. The external clock can be applied for the synchronization.

On the evaluation board, the SYNC/MODE pin can be connected to VCC or AGND through JP2 (as shown in Figure 3). Users can apply a clock input to the SMB connector, which is connected to the SYNC pin.

Table 1. Mode Selection

SYNC Pin	Mode of Operation
Low	Pulse skip mode
High	Forced PWM mode
Clock signal	Forced PWM mode

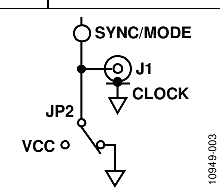


Figure 3. SYNC/MODE Signal

MEASURING EVALUATION BOARD PERFORMANCE

Output Voltage Ripple

To observe the output voltage ripple, place an oscilloscope probe tip at the T3 terminal and connect the probe ground lead at the negative (−) the T4 terminal. Set the oscilloscope to an ac-coupled, 100 mV/division and 2 μs/division time base.

Switching Waveform

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor that is connected to the SW pin with the probe ground at Terminal T4, PGND. Set the scope to dc, 5 V/division, and 2 μs/division time base. Alternate the switching waveform between 0 V and approximately the input voltage.

Measuring Load Regulation

Measure the load regulation by increasing the load at the output and looking at the change in the output voltage. To minimize voltage drop, use short low resistance wires, especially for heavy loads.

Measuring Line Regulation

Vary the input voltage and examine the change in the output voltage. In PWM mode, ensure that the output voltage ripple is small (<50 mV); however, in pulse skip mode, the output voltage ripple can be as large as 100 mV.

Measuring Efficiency

The efficiency, η, is measured by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of IR drops.

Inductor Current

By removing one end of the inductor from its pad and connecting a current loop in series with it, the inductor current can be measured. Once this is done, a current probe can be used to measure the current flowing through the current loop.

Line Transient Response

Generate a step input voltage (V_{IN}) and observe the behavior of the output voltage, with an oscilloscope.

Load Transient Response

Generate a load current transient at the output, V_{OUT}, and observe the output voltage response with an oscilloscope. Use a current probe attached to the wire between the output and the load to visualize the current transient.

Loop Stability Measurement

Closed-loop response can be measured using a network analyzer. To measure the loop response, the IN and OUT headers are available.

MODIFYING THE EVALUATION BOARD

The ADP2442-EVALZ evaluation board is provided fully assembled and tested for proper operation. The evaluation board has a fixed 5 V output voltage.

CHANGING THE OUTPUT VOLTAGE

The ADP2442-EVALZ output regulation voltage is set by a resistive voltage divider consisting of the R2 and R3 resistors. R2 corresponds to the R_{TOP} resistor in the ADP2442 data sheet, and R3 corresponds to the R_{BOTTOM} resistor in the ADP2442 data sheet. The output regulation voltage is determined by

$$V_{OUT} = 0.6\text{ V} \times \left[\frac{R2 + R3}{R3}\right]$$

where:
R2 is the value of the top resistor of the voltage divider (R_{TOP}).
R3 is the value of the bottom resistor of the voltage divider (R_{BOTTOM}).
V_{OUT} is the output regulation voltage in volts.

To set the output regulation voltage to the desired value, first determine the value of the bottom resistor, R3, by

$$R3 = \frac{V_{FB}}{I_{STRING}}$$

where:
V_{FB} = 0.6 V, the internal reference.
I_{STRING} is the resistor divider string current (greater than 20 µA nominally).

Once R3 is determined, calculate the value of the top resistor, R2, by

$$R2 = R3\left[\frac{V_{OUT} - V_{FB}}{V_{FB}}\right]$$

For example, to set the output regulation voltage of the ADP2442-EVALZ to 3.3 V, calculate the R2 and R3 values as shown in the following equations:

$$R3 = \frac{V_{FB}}{I_{STRING}} = \frac{0.6\text{ V}}{60\ \mu\text{A}} = 10\text{ k}\Omega$$

$$R2 = R3 \times \left[\frac{V_{OUT} - V_{FB}}{V_{FB}}\right]$$

$$= 10\text{ k}\Omega \times \left[\frac{3.3\text{ V} - 0.6\text{ V}}{0.6\text{V}}\right] = 45.3\text{ k}\Omega$$

When the output voltage of the ADP2442-EVALZ is changed, the output capacitors (C7 and C8), inductor (L1), and compensation components (R5 and C10) must be recalculated and changed to ensure stable operation according to the Applications Information section in the ADP2442 data sheet.

Table 2. Programming Output Voltage

Voltage (V)	R2 (kΩ)	R3 (kΩ)
12	190	10
5	73	10
3.3	45	10
1.2	10	10

CHANGING THE SWITCHING FREQUENCY

The switching frequency (f_{SW}) setpoint can be changed by replacing the R9 resistor with a different value by using following equation:

$$R9 = \frac{92{,}500}{f_{SW}}$$

where:
R9 is the frequency resistor in kΩ.
f_{SW} is the switching frequency in kHz.

Table 3. Programming Frequency

R9 (kΩ)	Frequency (kHz)
308	300
132	700
92.5	1000

When the switching frequency (f_{SW}) is changed, the L1, C7, C8, R5, and C10 values must be recalculated and changed to ensure stable operation (see the ADP2442 data sheet for details on external component selection).

TYPICAL PERFORMANCE CHARACTERISTICS

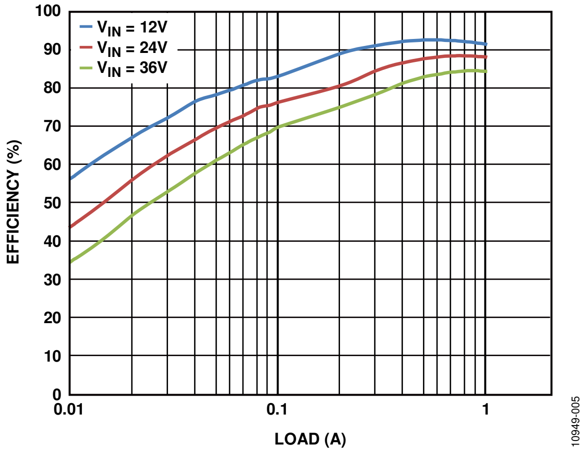


Figure 4. Efficiency vs. Load Current, V_{OUT} = 5 V, f_{SW} = 500 kHz, Pulse Skip Mode

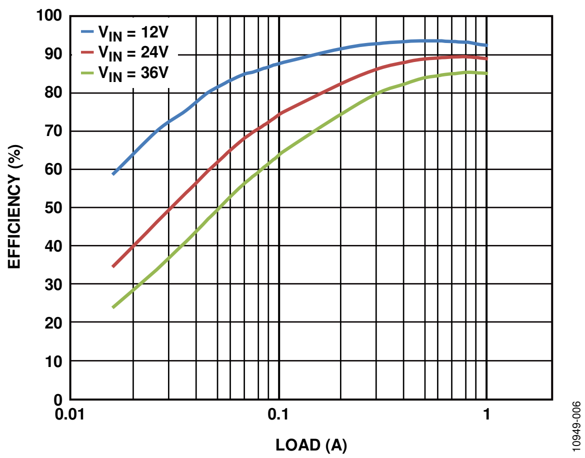


Figure 5. Efficiency vs. Load Current, V_{OUT} = 5 V, f_{SW} = 500 kHz, PWM Mode

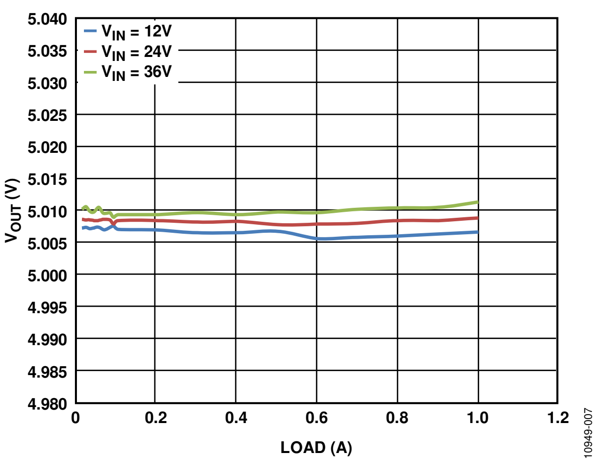


Figure 6. Load Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

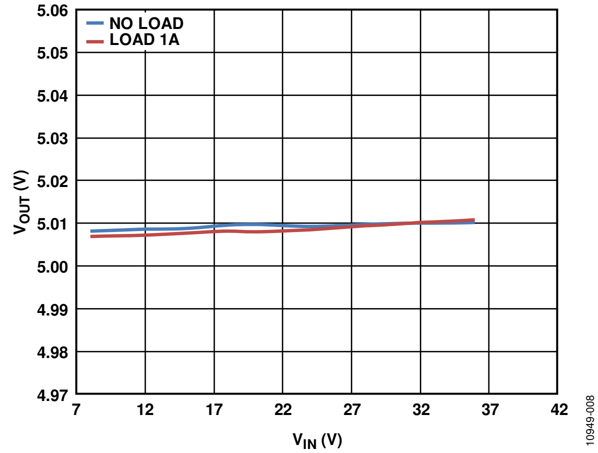


Figure 7. Line Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

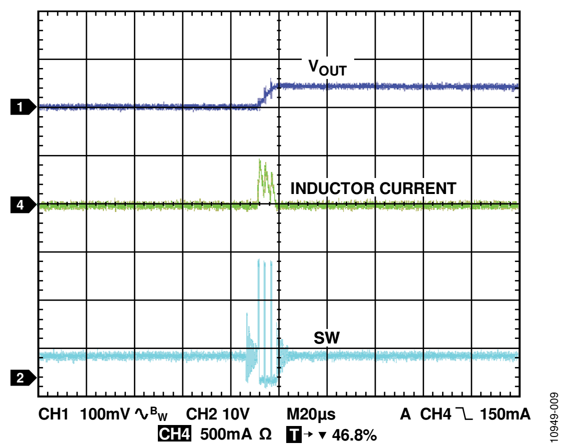


Figure 8. Pulse Skip Mode Waveforms, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 500 kHz, No Load, SYNC/MODE: AGND

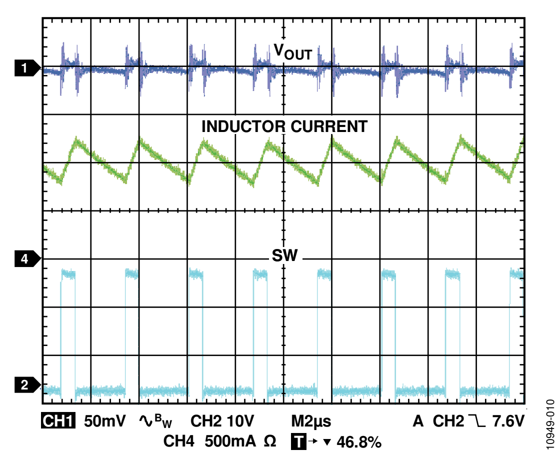


Figure 9. PWM Waveform, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 500 kHz, Load = 1 A

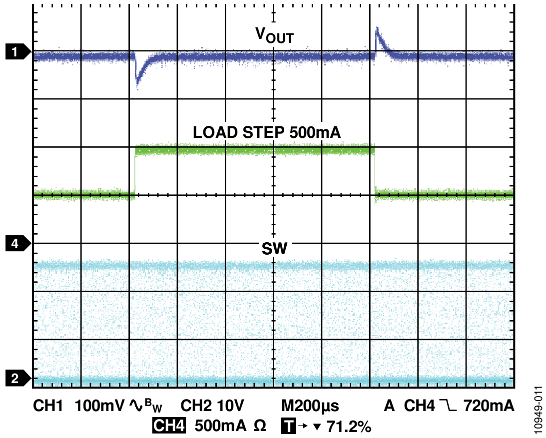


Figure 10. Load Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 500 mA Step

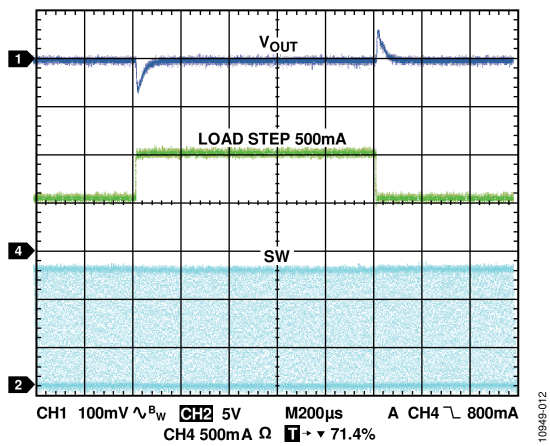
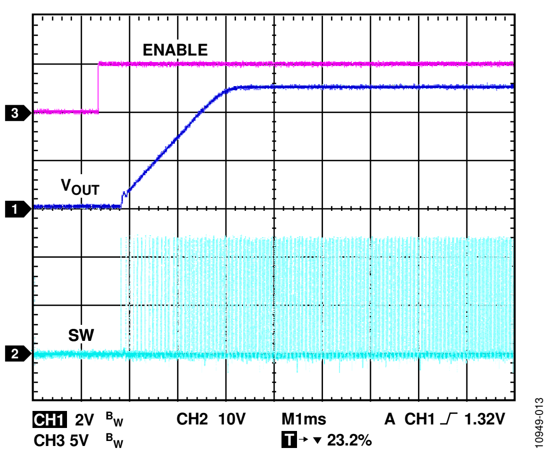


Figure 11. Load Transient, V_{IN} = 12 V, V_{OUT} = 5 V, 500 mA



ENABLE, CHANNEL 1 VOUT, AND CHANNEL 2 SW

Figure 12. Startup, V_{IN} = 24 V, V_{OUT} = 5 V, Load 5 Ω, PWM Mode

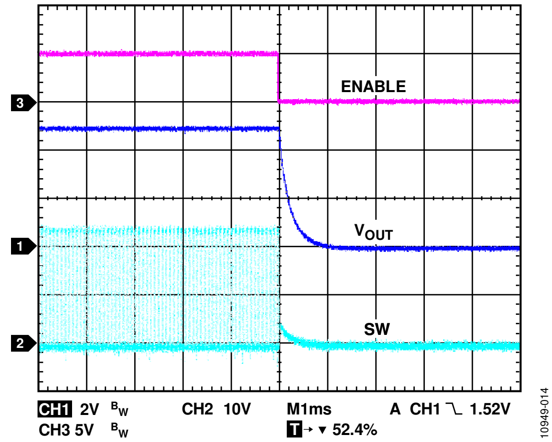


Figure 13. Shutdown, V_{IN} = 24 V, V_{OUT} = 5 V, Load 5 Ω

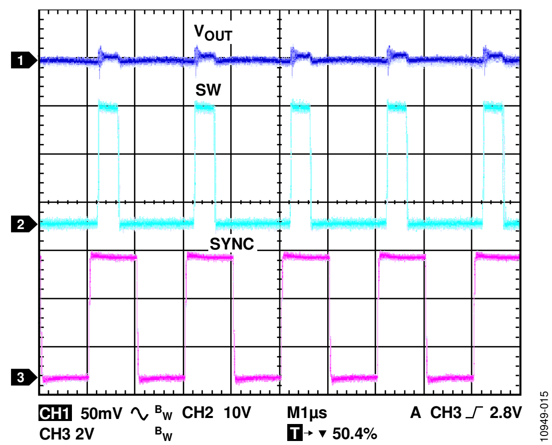


Figure 14. Clock Synchronization, V_{IN} = 24 V, V_{OUT} = 5 V

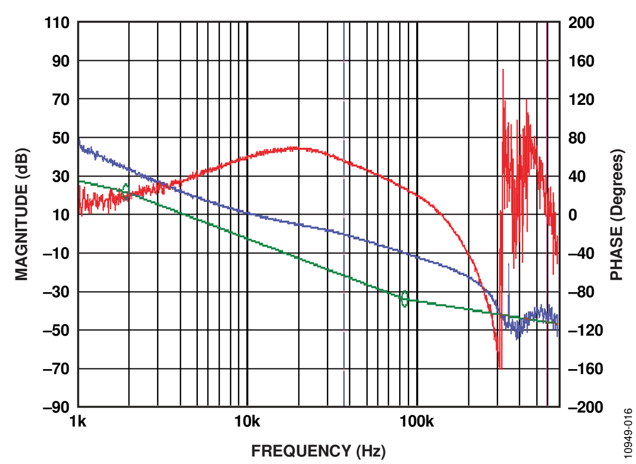


Figure 15. Bode Plot, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 500 kHz, Load = 1 A, f_{CO} = 37 kHz, Phase Margin = 55

EVALUATION BOARD SCHEMATIC AND ARTWORK

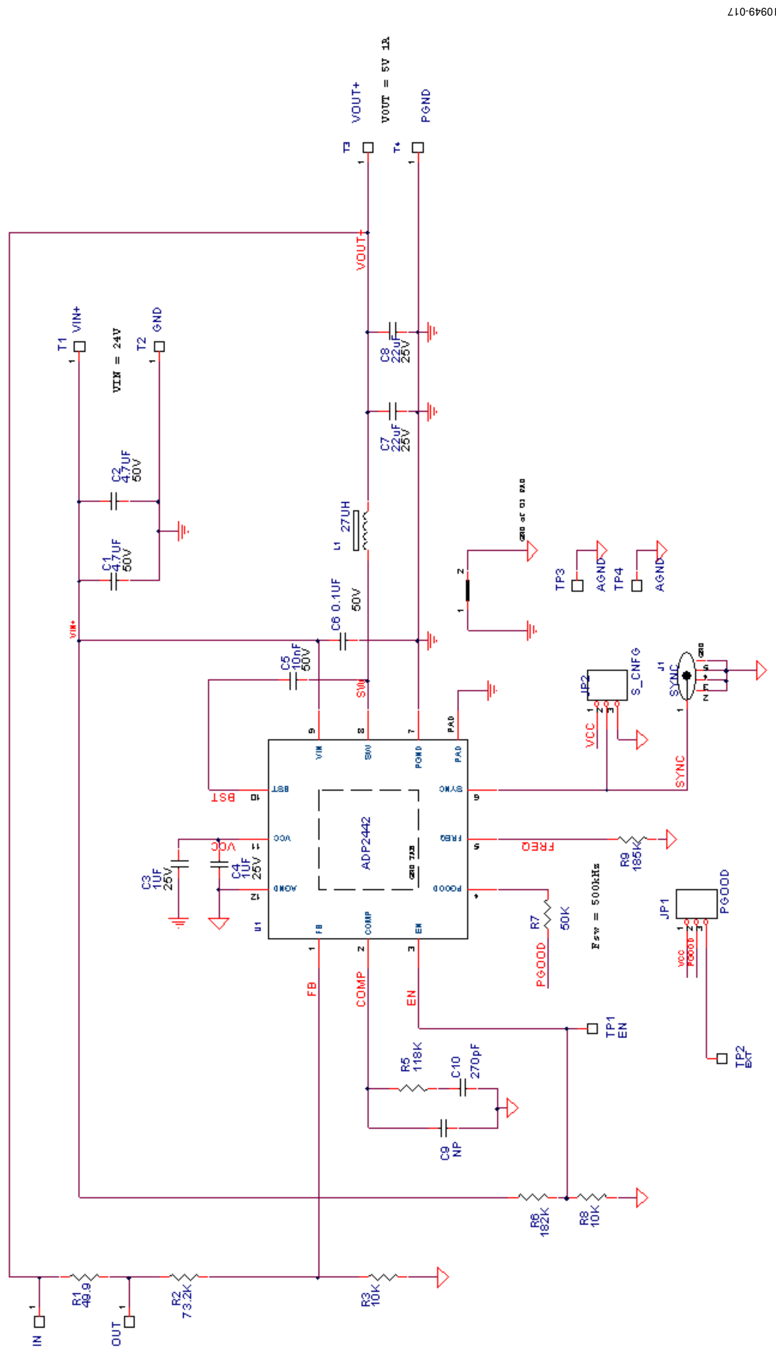


Figure 16. ADP2442-EVALZ Evaluation Board Schematic

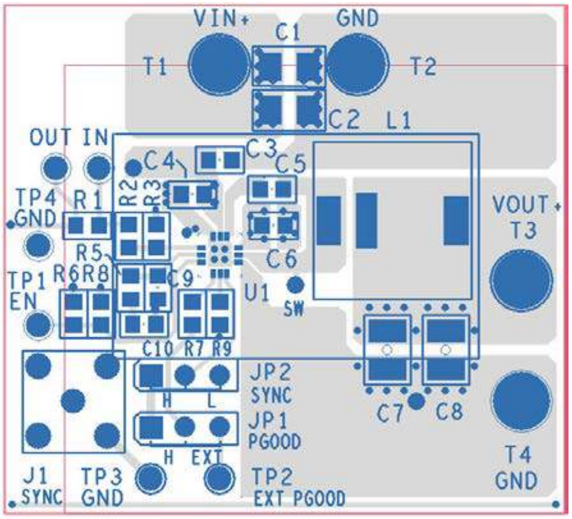


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Figure 17. ADP2442-EVALZ Evaluation Board Top Layer

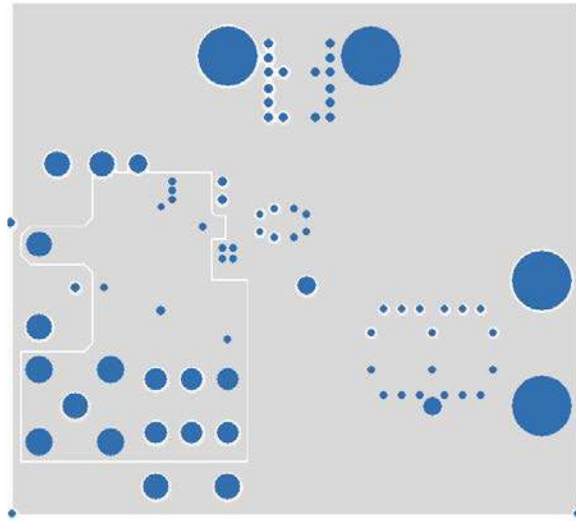

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Figure 19. ADP2442-EVALZ Evaluation Board Second Layer

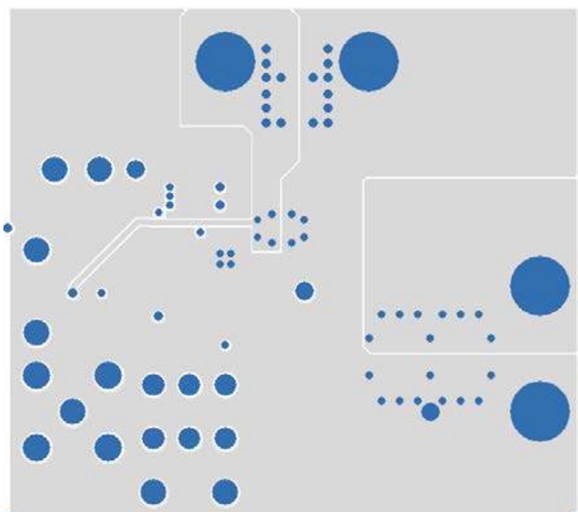

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Figure 18. ADP2442-EVALZ Evaluation Board Third Layer

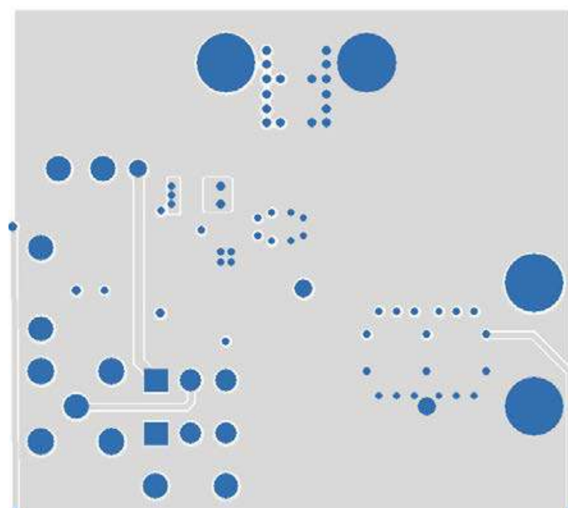

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Figure 20. ADP2442-EVALZ Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Quantity	Reference Designator	Description	Manufacturer/Part Number
2	C1, C2	Capacitor MLCC, 4.7 µF, 50 V, 1206, X7R	Murata GRM31CR71H475KA12L
2	C3, C4	Capacitor MLCC, 1 µF, 25 V, 0603, X7R	Murata GRM188R71E105KA12D
1	C5	Capacitor, MLCC, 10 nF, 50 V, 0603, X7R	Murata GRM188R71H103KA01D
2	C7, C8	Capacitor, MLCC, 22 µF, 25 V, 1210, X7R	Murata GRM32ER71E226K
1	L1	Shielded surface-mount power inductor	Coilcraft MSS1038T-273
1	C6	Capacitor MLCC, 0.1 µF, 50 V, 0603, X7R	Murata GRM188R71H104KA93D
1	C10	Capacitor MLCC, 270 pF, 50 V, 0603, X7R	Determine by the user
1	R1	Resistor, 49.9 Ω, 1/10 W, 1%, 0603, SMD	Determined by user
2	R3, R8	Resistor, 10 kΩ, 1/10 W, 1%, 0603, SMD	Determined by user
1	R7	Resistor, 50 kΩ, 1/10 W, 1%, 0603, SMD	Determined by user
1	R2	Resistor, 73.2 kΩ, 1/10 W, 1%, 0603, SMD	Determined by user
1	R5	Resistor, 118 kΩ, 1/10 W, 1%, 0603, SMD	Determined by user
1	R6	Resistor, 182 kΩ, 1/10 W, 11%, 0603, SMD	Determined by user
1	R9	Resistor, 185 kΩ, 1/10 W, 1%, 0603, SMD	Determined by user
2	IN, OUT	Headers	Sullins PBC01SAAN
1	J1 SYNC	SMB5PIN_JACK	Johnson J613-ND
4	TP1, TP2, TP3, TP4	Headers	Sullins PBC01SAAN
1	JP1 PGOOD	Jumper	Sullins PBC03SAAN
1	JP2 SYNC	Jumper	Sullins PBC03SAAN
4	T1, T2, T3, T4	Terminal, double turret, brass, 0.078"	Keystone 1502-1
1	U1	36 V, 1 A, synchronous, step-down DC-to-DC regulator	Analog Devices ADP2442

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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