12×12 DOTS MATRIX LED DRIVER WITH INDIVIDUAL AUTO BREATH FUNCTION

March 2022

GENERAL DESCRIPTION

The IS31FL3737B is a general purpose 12×12 LEDs matrix driver with 1/12 cycle rate. The device can be programmed via an I2C compatible interface. Each LED can be dimmed individually with 8-bit PWM data which allowing 256 steps of linear dimming.

IS31FL3737B features 3 Auto Breathing Modes which are noted as ABM-1, ABM-2 and ABM-3. For each Auto Breathing Mode, there are 4 timing characters which include current rising / holding / falling / off time and 3 loop characters which include Loop-Beginning / Loop-Ending / Loop-Times. Every LED can be configured to be any Auto Breathing Mode or No-Breathing Mode individually.

Additionally each LED open and short state can be detected, IS31FL3737B store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3737B operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3737B is available in QFN-40 (5mm×5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 12 current source outputs for row control
- 12 switch current inputs for column scan control
- Up to 144 LEDs (12×12) in dot matrix
- Programmable 12×12 (48 RGBs) matrix size with de-ghost function
- 1MHz I2C-compatible interface
- Selectable 3 Auto Breath Modes for each dot
- Auto Breath Loop Features interrupt pin inform MCU Auto Breath Loop completed
- Auto Breath offers 128 steps gamma current, interrupt and state look up registers
- 1.05kHz/ 2.1kHz/ 4.2kHz/ 8.4kHz/ 26.7kHz PWM frequency option
- 256 steps Global Current Setting
- Individual on/off control
- Individual 256 PWM control steps
- Individual Auto Breath Mode select
- Individual open and short error detect function
- Cascade for synchronization of chips
- QFN-40 (5mm×5mm) package

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Keyboard, Mouse etc.)
- LED in white goods application

TYPICAL APPLICATION CIRCUIT

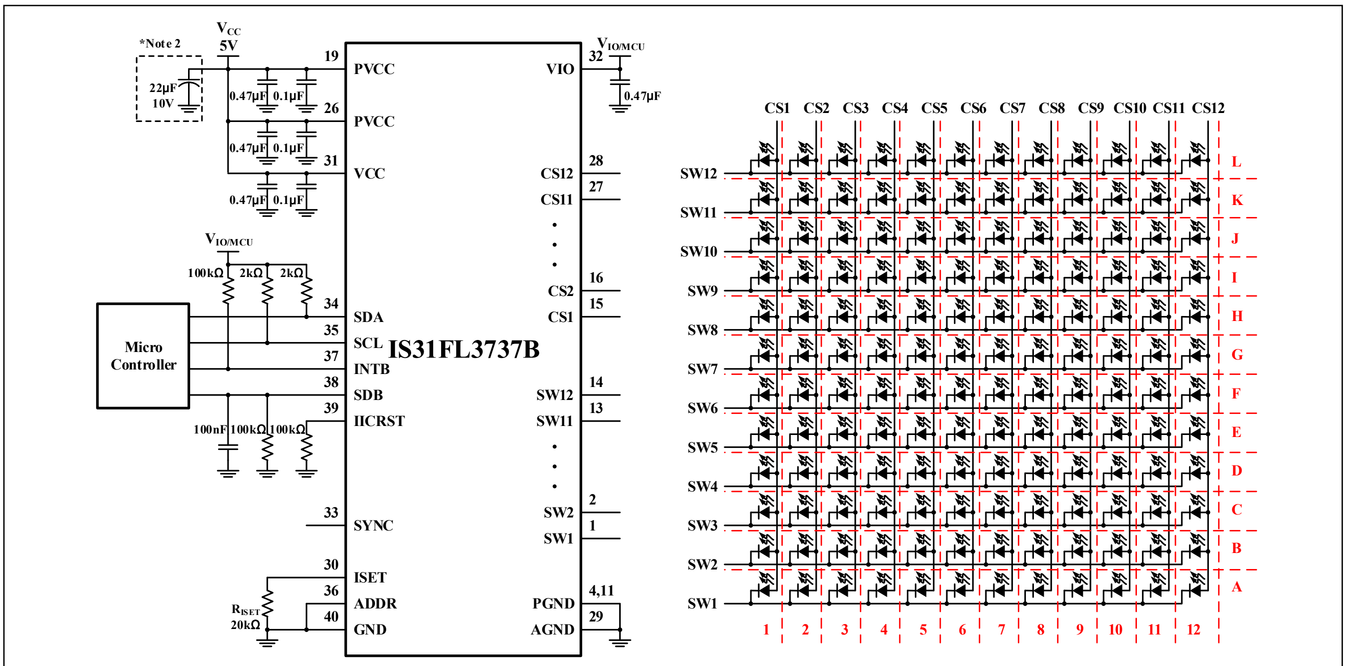


Figure 1 Typical Application Circuit (12×12)

TYPICAL APPLICATION CIRCUIT (CONTINUED)

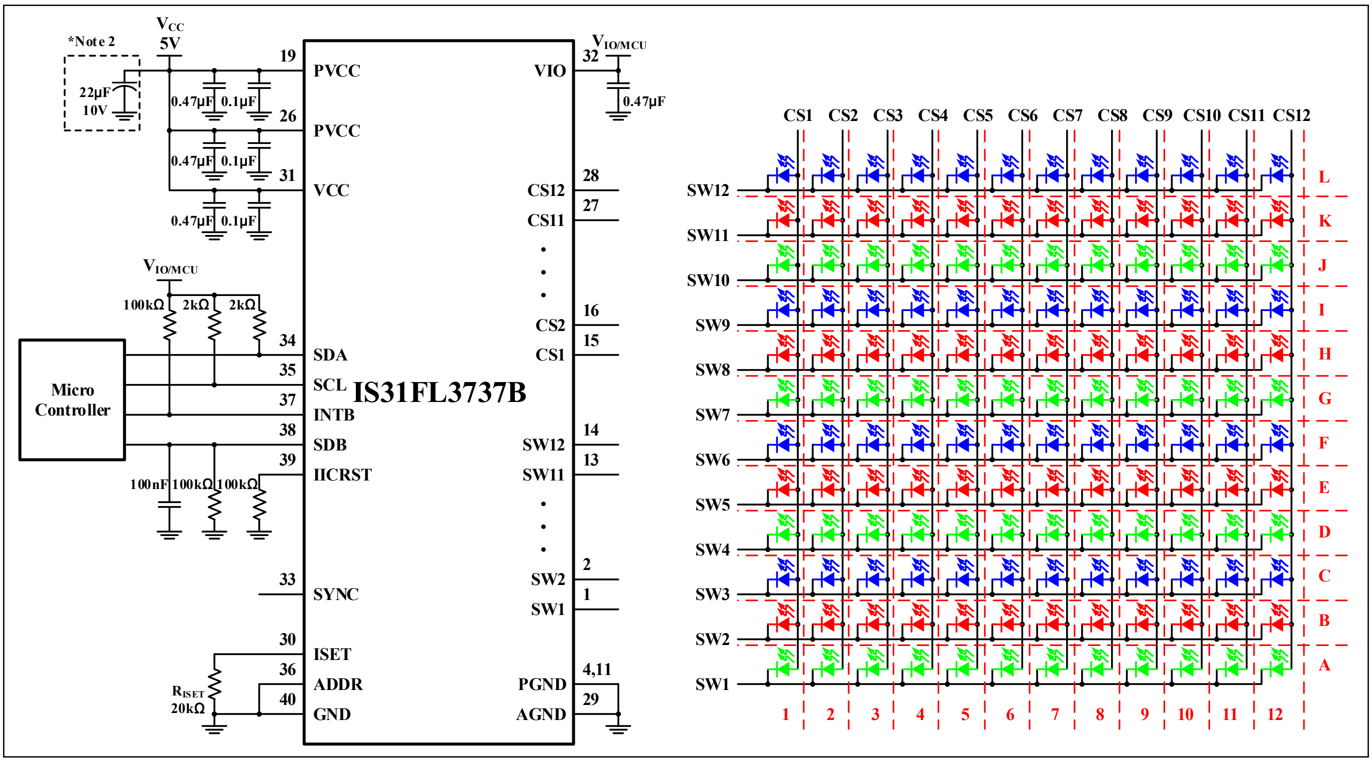


Figure 2 Typical Application Circuit (RGB)

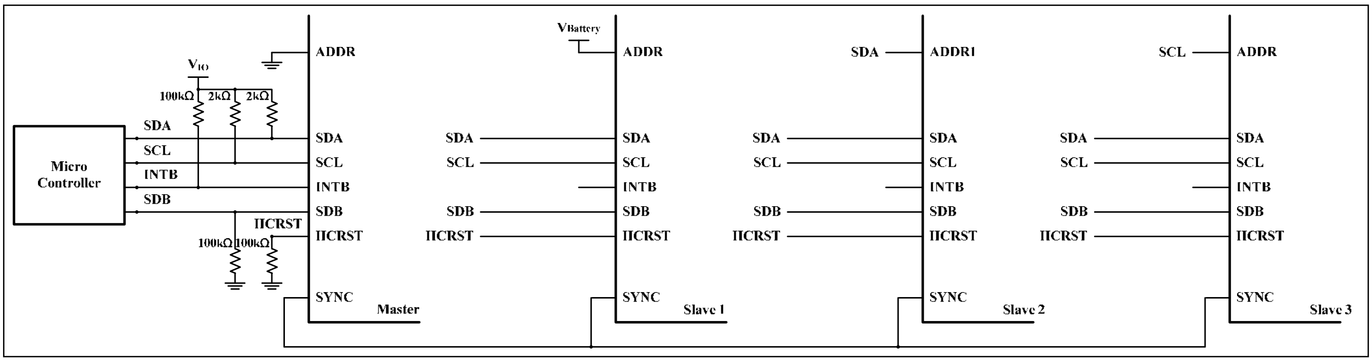


Figure 3 Typical Application Circuit (Four Parts Synchronization-Work)

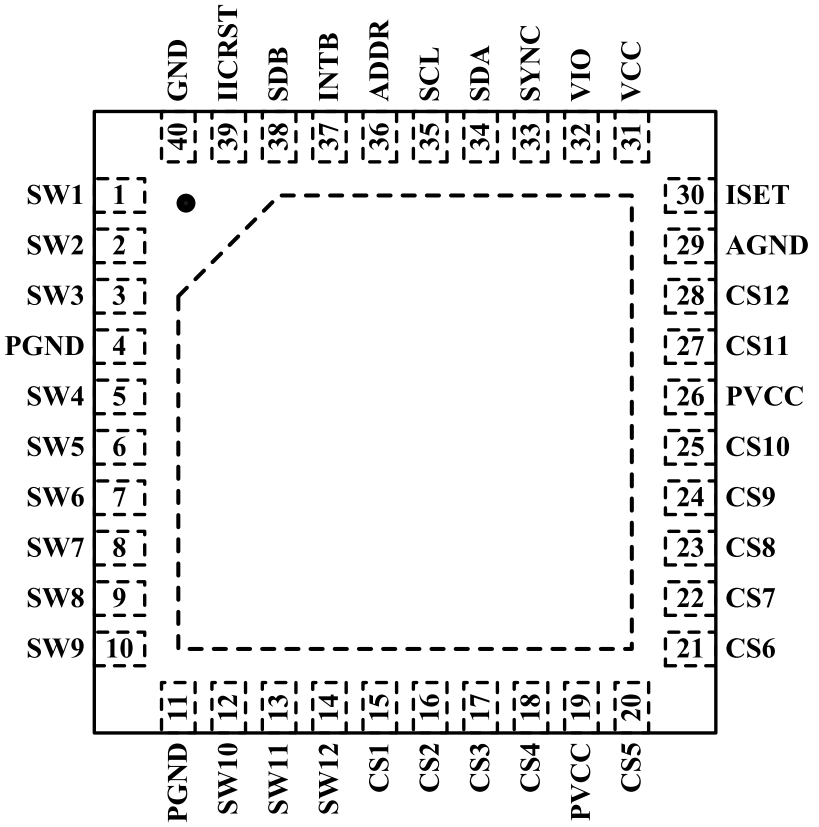
Note 1: IC should be placed far away from the antenna in order to prevent the EMI.

Note 2: Electrolytic/Tantalum Capacitor may be considered for high current application to avoid audible noise interference.

Note 3: The V_{IO} should be 1.8V≤V_{IO} ≤V_{CC}. And it is recommended to be equal to V_{OH} of the micro controller. For example, if V_{OH}=1.8V, set V_{IO}=1.8V, if V_{OH}=3.3V, set V_{IO}=3.3V.

Note 4: One system should contain only one master, all slave parts should be configured as slave mode before the master is configured as master mode. Work as master mode or slave mode specified by Configuration Register (Function register, address 00h). Master part output master clock, and all the other parts which work as slave input this master clock.

PIN CONFIGURATION

<table>
<tr><th>Package</th><th>Pin Configuration (Top View)</th></tr>
<tr><td>QFN-40</td><td>
</td></tr>
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PIN DESCRIPTION

No.	Pin	Description
1~3,5~10, 12~14	SW1~SW12	Switch pin for LED matrix scanning.
4,11	PGND	Power GND.
15~18,20~25, 27,28	CS1~CS12	Current Source.
19,26	PVCC	Power for current source.
29	AGND	Analog GND.
30	ISET	Input terminal used to connect an external resistor. This regulates current source DC current value.
31	VCC	Power for analog and digital circuits.
32	VIO	Input logic reference voltage.
33	SYNC	Synchronize pin. It is used for more than one part work synchronize. If it is not used please float this pin.
34	SDA	I2C compatible serial data.
35	SCL	I2C compatible serial clock.
36	ADDR	I2C address setting.
37	INTB	Interrupt output pin. Register F0h sets the function of the INTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function no used.
38	SDB	Shutdown the chip when pull to low.
39	IICRST	Reset I2C when pull high, need to pull down when normal operation.
40	GND	Connect to GND.
	Thermal Pad	Need to connect to GND pins.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3737B-QFLS4-TR	QFN-40, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A= T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	31°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 5: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= V_{CC}, all LEDs off		2	3	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		2	5	μA
		V_{SDB}= V_{CC}, Configuration Register written “0000 0000		2	5	
I_{OUT}	Maximum constant current of CS1~CS12	R_{ISET}= 20kΩ	39	42	45	mA
I_{LED}	Average current on each LED I_{LED} = I_{OUT}/12.75	R_{ISET}= 20kΩ, GCC= 255, PWM= 255	3.06	3.29	3.53	mA
V_{HR}	Current sink headroom voltage SW1~SW12	I_{SINK}= 504mA (Note 6, 7)		250	350	mV
	Current source headroom voltage CS1~C12	I_{SOURCE}= 42mA (Note 6)		150	200	
t_{SCAN}	Period of scanning	PFS= “000” (8.4kHz)	90	110	130	μs
		PFS= “010” (26.7kHz)	30	35	40	
		PFS= “011” (2.1kHz)	360	440	520	
t_{NOL}	Non-overlap blanking time during scan, the SWy and CSx are all off during this time	PFS= “000” (8.4kHz)	6.14	6.875	8.87	μs
		PFS= “010” (26.7kHz)	2.08	2.43	2.77	
		PFS= “011” (2.1kHz)	24.5	30	35.5	
T_{SD}	Thermal shutdown			160		°C
T_{SD_HYS}	Thermal shutdown hysteresis			25		°C
Logic Electrical Characteristics (SDA, SCL, ADDR, SYNC, SDB)						
V_{IL}	Logic “0” input voltage	V_{IO}= 3.6V	GND		0.2V_{IO}	V
V_{IH}	Logic “1” input voltage	V_{IO}= 3.6V	0.75V_{IO}		V_{IO}	V
V_{HYS}	Input schmitt trigger hysteresis	V_{IO}= 3.6V		0.2		V
V_{OL}	Logic “0” output voltage for SYNC	I_{OL}= 8mA			0.4	V
V_{OH}	Logic “1” output voltage for SYNC	I_{OH}= 8mA	0.75V_{IO}			V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 8)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{IO} (Note 8)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 8)

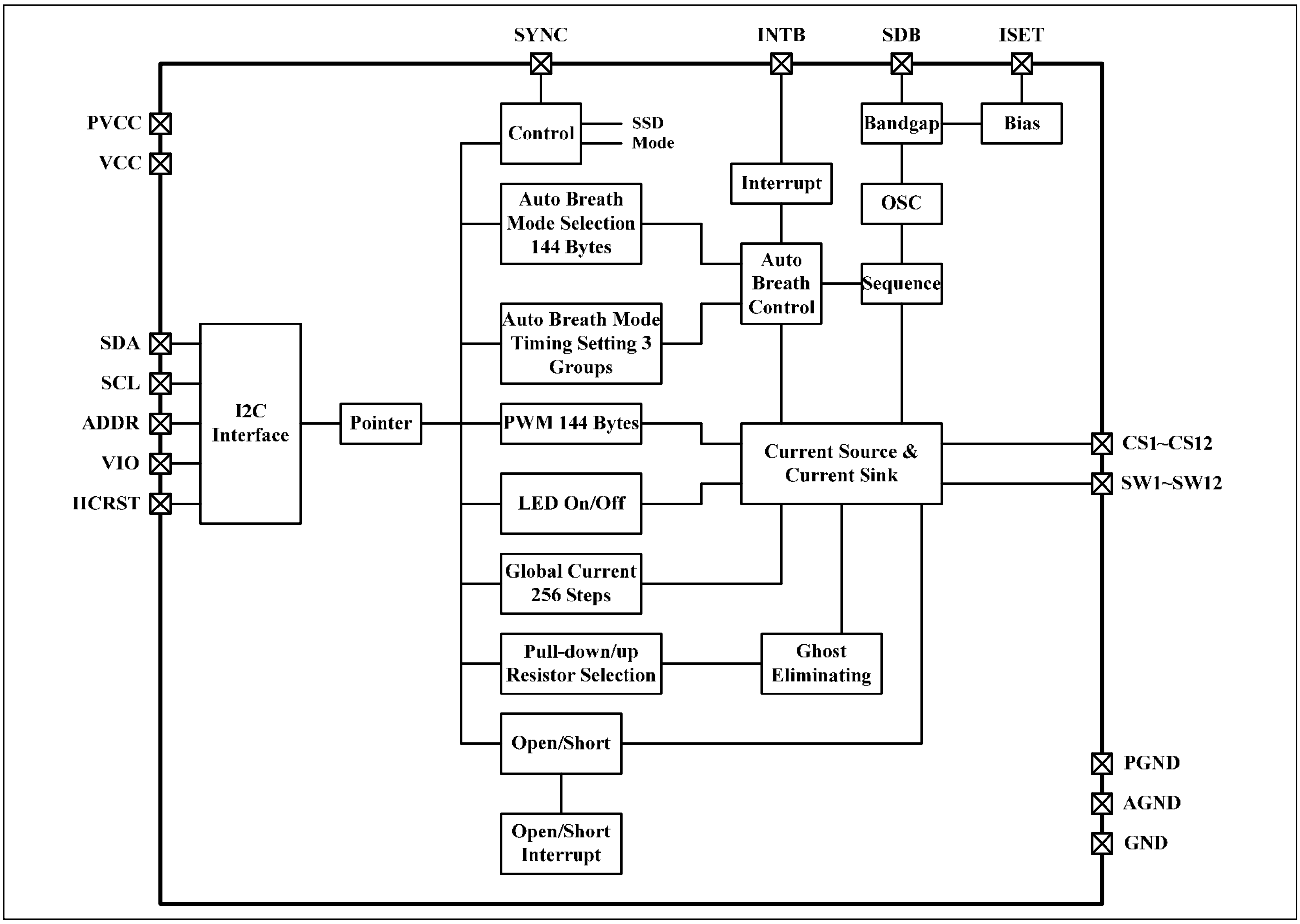
Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 6: In case of R_{ISET} = 20kΩ, Global Current Control Register (PG3, 01h) written "1111 1111", GCC = "1111 1111".

Note 7: All LEDs are on and PWM = "1111 1111", GCC = "1111 1111".

Note 8: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3737B uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3737B has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A4:A1 are decided by the connection of the ADDR pin.

The complete slave address is:

Table 1 Slave Address

ADDR	A7:A5	A4:A1	A0
GND	101	0000	0/1
SCL		0101	
SDA		1010	
VCC		1111	

ADDR connected to GND, (A4:A1)= 0000;
ADDR connected to VCC, (A4:A1)= 1111;
ADDR connected to SCL, (A4:A1)= 0101;
ADDR connected to SDA, (A4:A1)= 1010;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3737B.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3737B's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3737B has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3737B, the register address byte is sent, most significant bit first. IS31FL3737B must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3737B must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3737B, load the address of the data register that the first data byte is intended for. During the IS31FL3737B acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3737B will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3737B (Figure 7).

READING OPERATION

FEh, F1h and 18h~47h of Page 0 can be read.

To read the FEh and F1h, after I2C start condition, the bus master must send the IS31FL3737B device address with the $R/\overline{W}$ bit set to "0", followed by the register address (FEh or F1h) which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3737B device address with the $R/\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3737B to the master (Figure 8).

To read the 18h~47h of Page 0, the FDh should write with 00h before follow the Figure 8 sequence to read the data, that means, when you want to read 18h~47h of Page 0, the FDh should point to Page 0 first and you can read the Page 0 data.

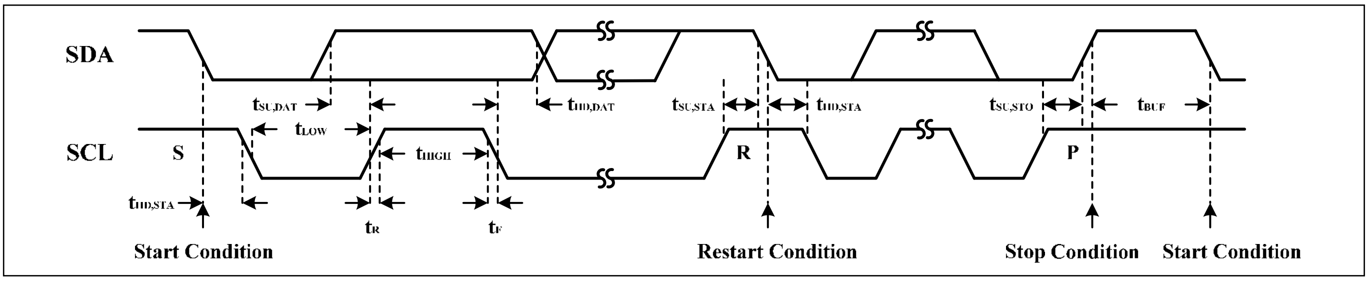


Figure 4 Interface Timing

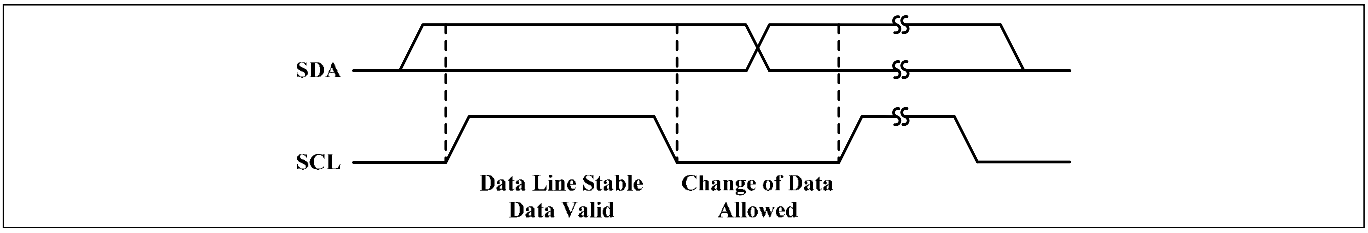


Figure 5 Bit Transfer

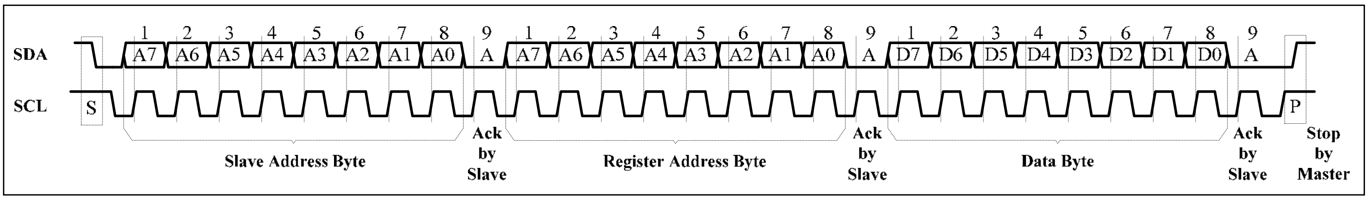


Figure 6 Writing to IS31FL3737B (Typical)

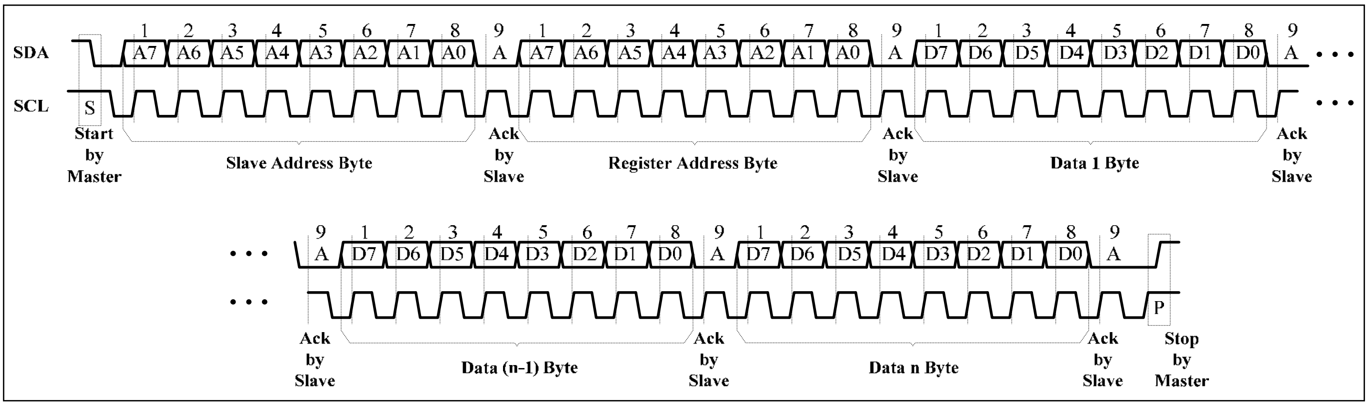


Figure 7 Writing to IS31FL3737B (Automatic address increment)

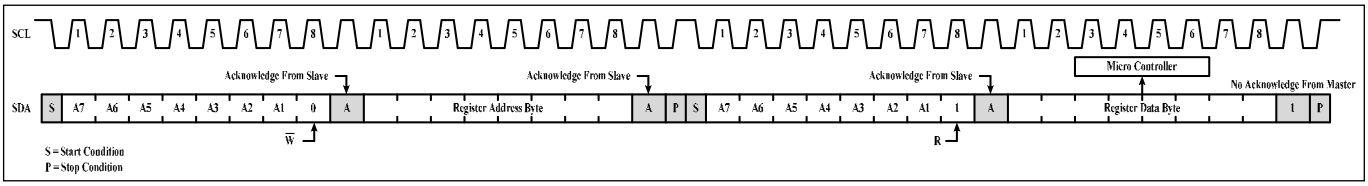


Figure 8 Reading from IS31FL3737B

REGISTER DEFINITION-1

Address	Name	Function	Table	R/W	Default
FDh	Command Register	Available Page 0 to Page 3 Registers	2	W	xxxx xxxx
FEh	Command Register Write Lock	To lock/unlock Command Register	3	R/W	0000 0000
F0h	Interrupt Mask Register	Configure the interrupt function	4	W	
F1h	Interrupt Status Register	Show the interrupt status	5	R	

REGISTER CONTROL

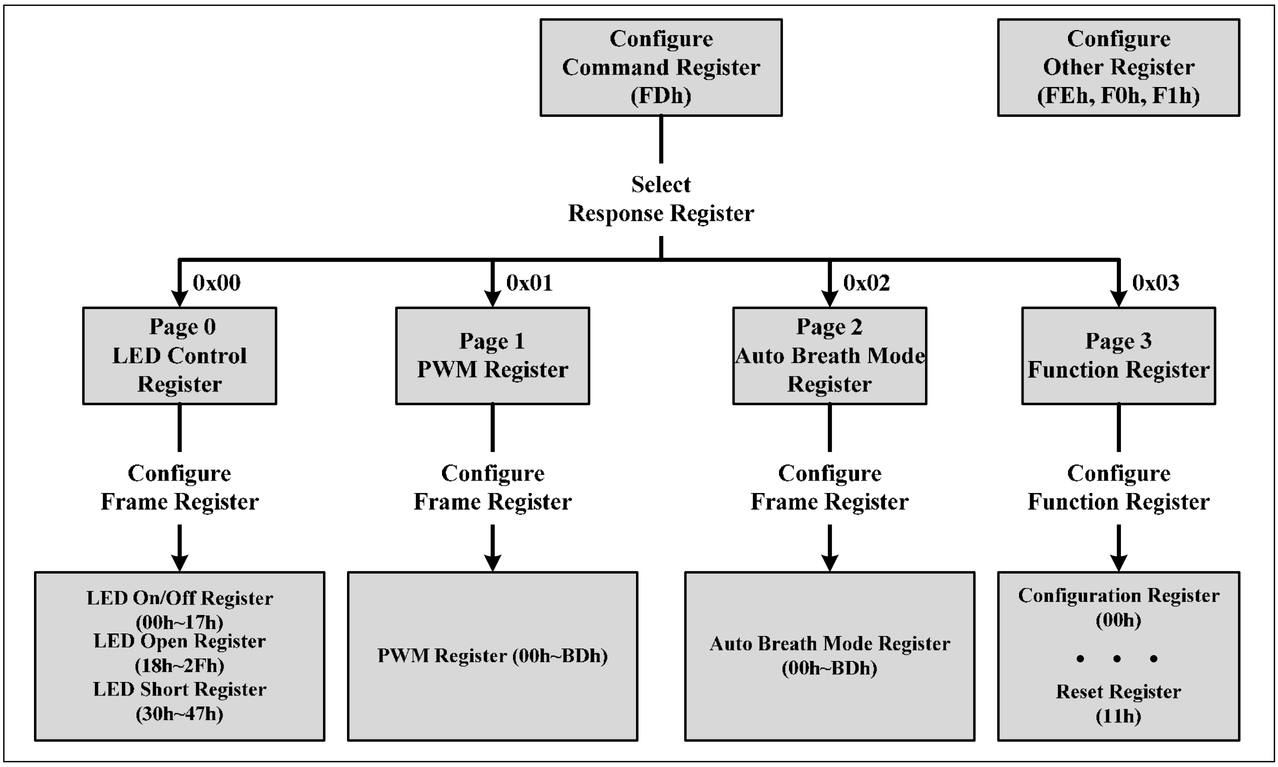


Table 2 FDh Command Register (Write Only)

Data	Function
0000 0000	Point to Page 0 (PG0, LED Control Register is available)
0000 0001	Point to Page 1 (PG1, PWM Register is available)
0000 0010	Point to Page 2 (PG2, Auto Breath Mode Register is available)
0000 0011	Point to Page 3 (PG3, Function Register is available)
Others	Reserved

Note: FDh is locked when power up, need to unlock this register before write command to it. See Table 3 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is “0000 0000”.

For example, when write “0000 0001” in the Command Register (FDh), the data which writing after will be stored in the PWM Register (Page1).

Table 3 FEh Command Register Write Lock (Read/Write)

Bit	D7:D0
Name	CRWL
Default	0000 0000 (FDh write disable)

To select the PG0~PG3, need to unlock this register first, with the purpose to avoid misoperation of this register. When FEh is written with 0xC5, FDh is allowed to modify once, after the FDh is modified the FEh will reset to be 0x00 at once.

CRWL Command Register Write Lock
0x00 FDh write disable
0xC5 FDh write enable once

Table 4 F0h Interrupt Mask Register (Write Only)

Bit	D7:D4	D3	D2	D1	D0
Name	-	IAC	IAB	IS	IO
Default	0000	0	0	0	0

Configure the interrupt function for IC.

IAC Auto Clear Interrupt Bit
0 Interrupt could not auto clear
1 Interrupt auto clear when INTB stay low exceeds 8ms

IAB Auto Breath Interrupt Bit
0 Disable auto breath loop finish interrupt
1 Enable auto breath loop finish interrupt

IS Dot Short Interrupt Bit
0 Disable dot short interrupt
1 Enable dot short interrupt

IO Dot Open Interrupt Bit
0 Disable dot open interrupt
1 Enable dot open interrupt

Table 5 F1h Interrupt Status Register (Read Only)

Bit	D7:D5	D4	D3	D2	D1	D0
Name	-	ABM3	ABM2	ABM1	SB	OB
Default	000	0	0	0	0	0

Show the interrupt status for IC.

ABM3 Auto Breath Mode 3 Finish Bit
0 ABM3 not finish
1 ABM3 finish

ABM2 Auto Breath Mode 2 Finish Bit
0 ABM2 not finish
1 ABM2 finish

ABM1 Auto Breath Mode 1 Finish Bit
0 ABM1 not finish
1 ABM1 finish

SB Short Bit
0 No short
1 Short happens

OB Open Bit
0 No open
1 Open happens

REGISTER DEFINITION-2

Address	Name	Function	Table	R/W	Default
PG0 (0x00): LED Control Register					
00h ~ 17h	LED On/Off Register	Set on or off state for each LED	7	W	0000 0000
18h ~ 2Fh	LED Open Register	Store open state for each LED	8	R	
30h ~ 47h	LED Short Register	Store short state for each LED	9	R	
PG1 (0x01): PWM Register					
00h~BDh	PWM Register	Set PWM duty for LED	10	W	0000 0000
PG2 (0x02): Auto Breath Mode Register					
00h~BDh	Auto Breath Mode Register	Set operating mode of each dot	11	W	xxxx xx00
PG3 (0x03) : Function Register					
00h	Configuration Register	Configure the operation mode	13	W	0000 0000
01h	Global Current Control Register	Set the global current	14	W	
02h	Auto Breath Control Register 1 of ABM-1	Set fade in and hold time for breath function of ABM-1	15	W	
03h	Auto Breath Control Register 2 of ABM-1	Set the fade out and off time for breath function of ABM-1	16	W	
04h	Auto Breath Control Register 3 of ABM-1	Set loop characters of ABM-1	17	W	
05h	Auto Breath Control Register 4 of ABM-1	Set loop characters of ABM-1	18	W	
06h	Auto Breath Control Register 1 of ABM-2	Set fade in and hold time for breath function of ABM-2	15	W	
07h	Auto Breath Control Register 2 of ABM-2	Set the fade out and off time for breath function of ABM-2	16	W	
08h	Auto Breath Control Register 3 of ABM-2	Set loop characters of ABM-2	17	W	
09h	Auto Breath Control Register 4 of ABM-2	Set loop characters of ABM-2	18	W	
0Ah	Auto Breath Control Register 1 of ABM-3	Set fade in and hold time for breath function of ABM-3	15	W	
0Bh	Auto Breath Control Register 2 of ABM-3	Set the fade out and off time for breath function of ABM-3	16	W	
0Ch	Auto Breath Control Register 3 of ABM-3	Set loop characters of ABM-3	17	W	
0Dh	Auto Breath Control Register 4 of ABM-3	Set loop characters of ABM-3	18	W	
0Eh	Time Update Register	Update the setting of 02h ~ 0Dh registers	-	W	
0Fh	SWy Pull-Up Resistor Selection Register	Set the pull-up resistor for SWy	19	W	
10h	CSx Pull-Down Resistor Selection Register	Set the pull-down resistor for CSx	20	W	
11h	Reset Register	Reset all register to POR state	-	R	

Table 6 Page 0 (PG0, 0x00): LED Control Register

LED Location		LED On/Off Register		LED Open Register		LED Short Register	
SW1(CS1~ CS6)	SW1(CS7~ CS12)	**00h**	01h	**18h**	19h	**30h**	31h
SW2(CS1~ CS6)	SW2(CS7~ CS12)	**02h**	03h	**1Ah**	1Bh	**32h**	33h
SW3(CS1~ CS6)	SW3(CS7~ CS12)	**04h**	05h	**1Ch**	1Dh	**34h**	35h
SW4(CS1~ CS6)	SW4(CS7~ CS12)	**06h**	07h	**1Eh**	1Fh	**36h**	37h
SW5(CS1~ CS6)	SW5(CS7~ CS12)	**08h**	09h	**20h**	21h	**38h**	39h
SW6(CS1~ CS6)	SW6(CS7~ CS12)	**0Ah**	0Bh	**22h**	23h	**3Ah**	3Bh
SW7(CS1~ CS6)	SW7(CS7~ CS12)	**0Ch**	0Dh	**24h**	25h	**3Ch**	3Dh
SW8(CS1~ CS6)	SW8(CS7~ CS12)	**0Eh**	0Fh	**26h**	27h	**3Eh**	3Fh
SW9(CS1~ CS6)	SW9(CS7~ CS12)	**10h**	11h	**28h**	29h	**40h**	41h
SW10(CS1~ CS6)	SW10(CS7~ CS12)	**12h**	13h	**2Ah**	2Bh	**42h**	43h
SW11(CS1~ CS6)	SW11(CS7~ CS12)	**14h**	15h	**2Ch**	2Dh	**44h**	45h
SW12(CS1~ CS6)	SW12(CS7~ CS12)	**16h**	17h	**2Eh**	2Fh	**46h**	47h

Table 7 00h ~ 17h LED On/Off Register

Bit	D7:D6	D5:D0
Name	-	$C_{CS6}:C_{CS1}$ or $C_{CS12}:C_{CS7}$
Default	00	00 0000

The LED On/Off Registers store the on or off state of each LED in the Matrix.

$C_{X\text{-}Y}$ LED State Bit
0 LED off
1 LED on

Table 8 18h ~ 2Fh LED Open Register

Bit	D7:D6	D5:D0
Name	-	$OP_6:OP_1$ or $OP_{12}:OP_7$
Default	00	00 0000

The LED Open Registers store the open or normal state of each LED in the Matrix.

OPx LED Open Bit
0 LED normal
1 LED open

Table 9 30h ~ 47h LED Short Register

Bit	D7:D6	D5:D0
Name	-	$ST_6:ST_1$ or $ST_{12}:ST_7$
Default	00	0000 0000

The LED Short Registers store the short or normal state of each LED in the Matrix.

STx LED Short Bit
0 LED normal
1 LED short

Page 1 (PG1, 0x01): PWM Register

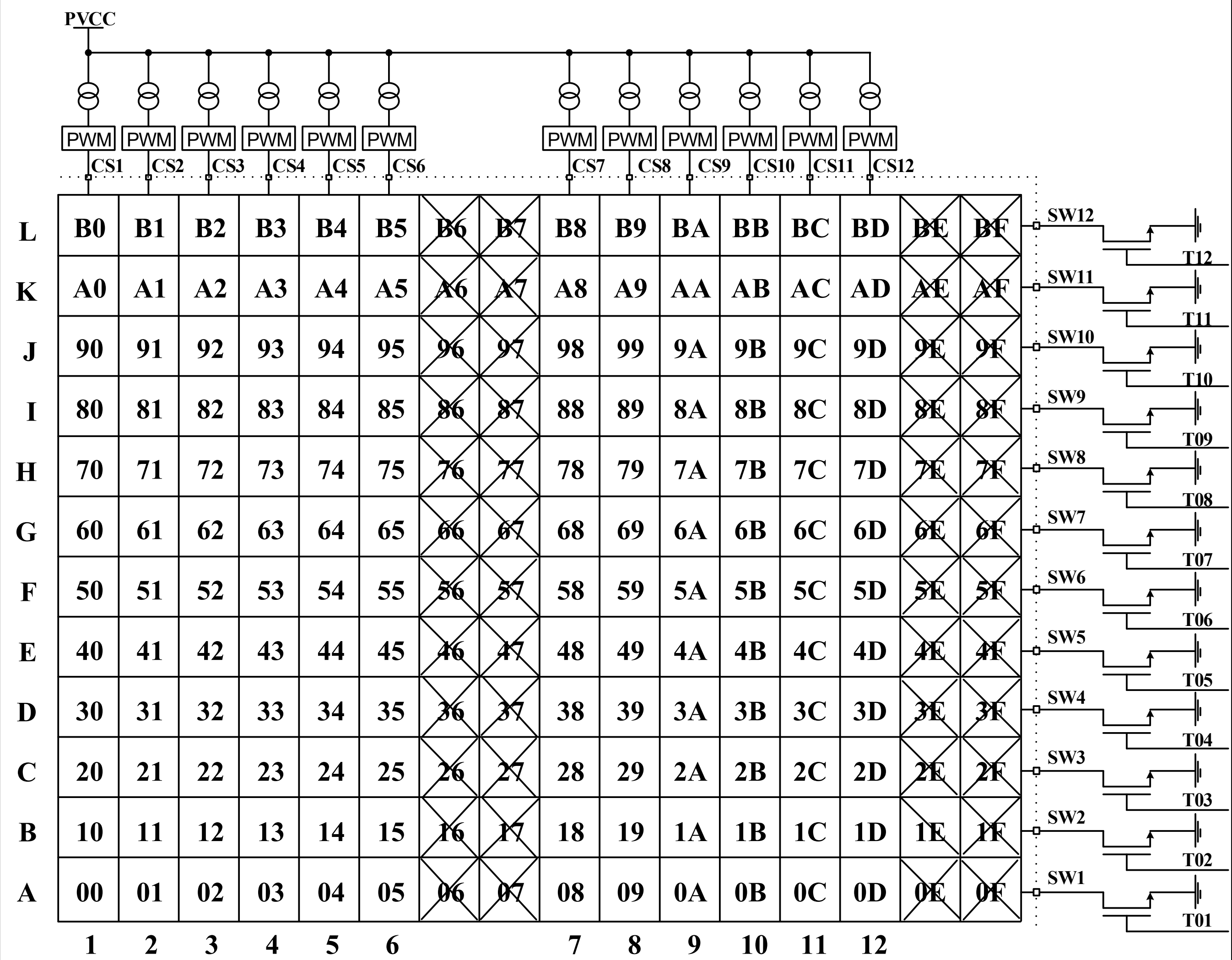


Figure 9 PWM Register

Table 10 00h ~ BDh PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has a byte to modulate the PWM duty in 256 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT} \times Duty \qquad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWy (PFS= “000”),

$$Duty = \frac{110\mu s}{(110\mu s + 6.875\mu s)} \times \frac{1}{12} = \frac{1}{12.75} \qquad (2)$$

I_{OUT} is the output current of CSx (x=1~12),

$$I_{OUT} = \frac{840}{R_{ISET}} \times \frac{GCC}{256} \qquad (3)$$

GCC is the Global Current Control register (PG3, 01h) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0= 1011 0101 (0xB5, 181), GCC= 255, R_{ISET}= 20kΩ (I_{OUT}= 42mA),

$$I_{LED} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times I_{OUT} \times \frac{1}{12.75} = 2.34mA$$

Page 2 (PG2, 0x02): Auto Breath Mode Register

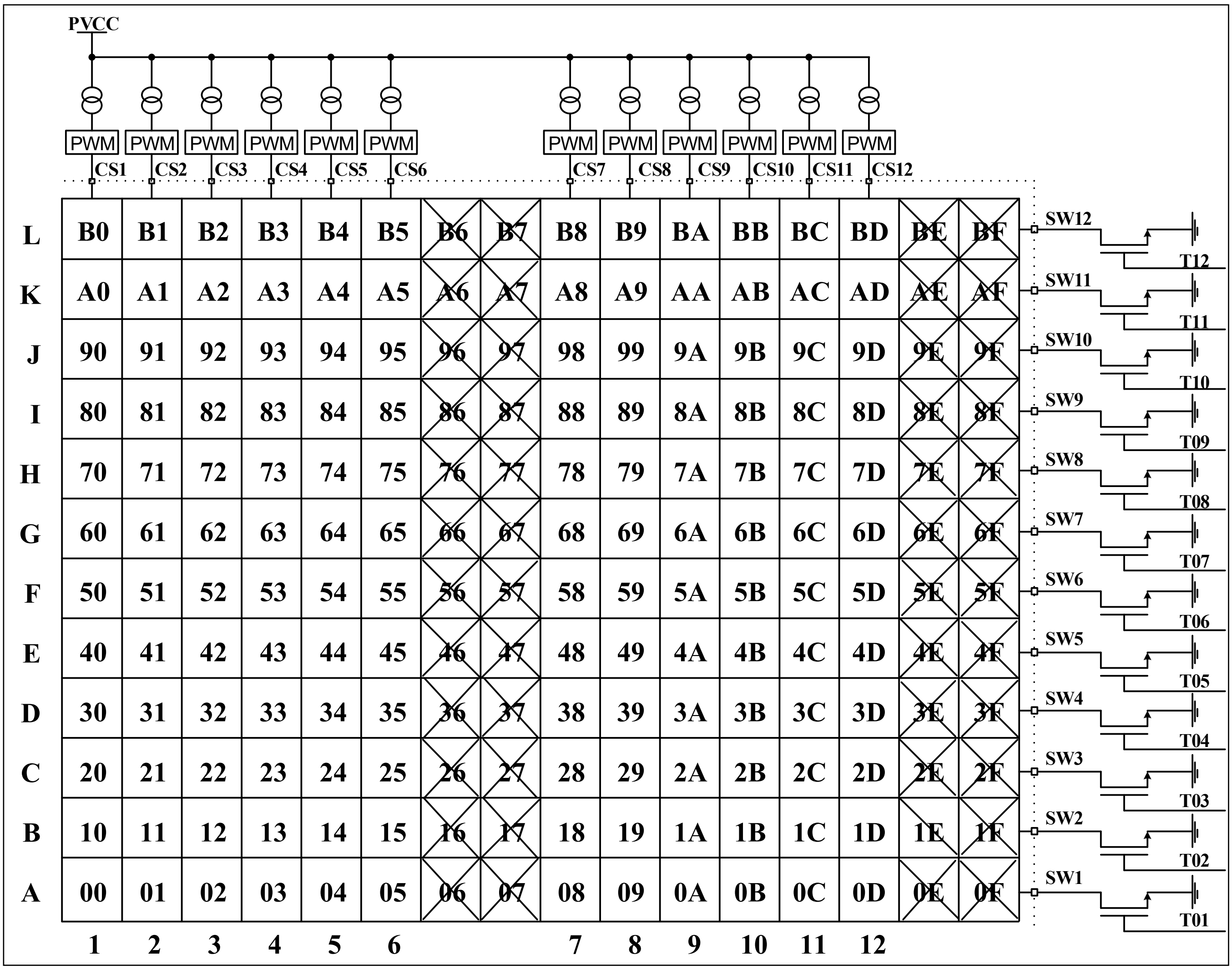


Figure 10 Auto Breath Mode Selection Register

Table 11 00h ~ BDh Auto Breath Mode Register

Bit	D7:D2	D1:D0
Name	-	ABMS
Default	-	00

The Auto Breath Mode Register sets operating mode of each dot.

ABMS Auto Breath Mode Selection Bit
00 PWM control mode
01 Select Auto Breath Mode 1 (ABM-1)
10 Select Auto Breath Mode 2 (ABM-2)
11 Select Auto Breath Mode 3 (ABM-3)

Table 12 Page 3 (PG3, 0x03): Function Register

Register	Name	Function	R/W	Default
00h	Configuration Register	Configure the operation mode	W	0000 0000
01h	Global Current Control Register	Set the global current	W	
02h	Auto Breath Control Register 1 of ABM-1	Set fade in and hold time for breath function of ABM-1	W	
03h	Auto Breath Control Register 2 of ABM-1	Set the fade out and off time for breath function of ABM-1	W	
04h	Auto Breath Control Register 3 of ABM-1	Set loop characters of ABM-1	W	
05h	Auto Breath Control Register 4 of ABM-1	Set loop characters of ABM-1	W	
06h	Auto Breath Control Register 1 of ABM-2	Set fade in and hold time for breath function of ABM-2	W	
07h	Auto Breath Control Register 2 of ABM-2	Set the fade out and off time for breath function of ABM-2	W	
08h	Auto Breath Control Register 3 of ABM-2	Set loop characters of ABM-2	W	
09h	Auto Breath Control Register 4 of ABM-2	Set loop characters of ABM-2	W	
0Ah	Auto Breath Control Register 1 of ABM-3	Set fade in and hold time for breath function of ABM-3	W	
0Bh	Auto Breath Control Register 2 of ABM-3	Set the fade out and off time for breath function of ABM-3	W	
0Ch	Auto Breath Control Register 3 of ABM-3	Set loop characters of ABM-3	W	
0Dh	Auto Breath Control Register 4 of ABM-3	Set loop characters of ABM-3	W	
0Eh	Time Update Register	Update the setting of 02h ~ 0Dh registers	W	
0Fh	SWy Pull-Up Resistor Selection Register	Set the pull-up resistor for SWy	W	
10h	CSx Pull-Down Resistor Selection Register	Set the pull-down resistor for CSx	W	
11h	Reset Register	Reset all register to POR state	R	

Table 13 00h Configuration Register

Bit	D7:D6	D5:D3	D2	D1	D0
Name	SYNC	PFS	OSD	B_EN	SSD
Default	00	000	0	0	0

The Configuration Register sets operating mode of IS31FL3737B.

When SYNC bits are set to “01”, the IS31FL3737B is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to “10”.

The PFS bits selects a fixed PWM operating frequency for all CSx, when PFS set “000”, the PWM frequency is 8.4kHz, when PFS set to “010”, the PWM frequency is 26.7kHz.

When OSD set high, open/short detection will be trigger once, the user could trigger OS detection again by set OSD from “0” to “1”.

When B_EN enable, those dots select working in ABM-x mode will start to run the pre-established timing. If it is disabled, all dots work in PWM mode. Following Figure 16 to enable the Auto Breath mode

When SSD is “0”, IS31FL3737B works in software shutdown mode and to normal operate the SSD bit should set to “1”.

SYNC Synchronize Configuration
00/11 High Impedance
01 Master
10 Slave

PFS PWM Frequency Setting
000 8.4kHz(default)
010 26.7kHz
001 4.2kHz
011 2.1kHz
100 1.05kHz

OSD Open/Short Detection Enable Bit
0 Disable open/short detection
1 Enable open/short detection

B_EN Auto Breath Enable
0 PWM Mode Enable
1 Auto Breath Mode Enable

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

Table 14 01h Global Current Control Register

Bit	D7:D0
Name	GCCx
Default	0000 0000

The Global Current Control Register modulates all CSx (x=1~12) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT} = \frac{840}{R_{ISET}} \times \frac{GCC}{256} \quad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, R_{ISET} is the external resistor of ISET pin.

For example: if D7:D0 = 1011 0101,

$$I_{OUT} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times \frac{840}{R_{ISET}}$$

Table 15 02h, 06h, 0Ah Auto Breath Control Register 1 of ABM-x

Bit	D7:D5	D4:D1	D0
Name	T1	T2	-
Default	000	0000	0

Auto Breath Control Register 1 set the T1&T2 time in Auto Breath Mode.

T1 T1 Setting

T1 \ PFS	000(s)	010(s)	001(s)	011(s)	100(s)
000	0.21	0.07	0.42	0.84	1.68
001	0.42	0.14	0.84	1.68	3.36
010	0.84	0.28	1.68	3.36	6.72
011	1.68	0.56	3.36	6.72	13.44
100	3.36	1.12	6.72	13.44	26.88
101	6.72	2.24	13.44	26.88	53.76
110	13.44	4.48	26.88	53.76	107.52
111	26.88	8.96	53.76	107.52	215.04

T2 T2 Setting

T2 \ PFS	000(s)	010(s)	001(s)	011(s)	100(s)
000	0	0	0	0	0
001	0.21	0.07	0.42	0.84	1.68
010	0.42	0.14	0.84	1.68	3.36
011	0.84	0.28	1.68	3.36	6.72
100	1.68	0.56	3.36	6.72	13.44
101	3.36	1.12	6.72	13.44	26.88
110	6.72	2.24	13.44	26.88	53.76
111	13.44	4.48	26.88	53.76	107.52
1000	26.88	8.96	53.76	107.52	215.04
Others	Unavailable				

Table 16 03h, 07h, 0Bh Auto Breath Control Register 2 of ABM-x

Bit	D7:D5	D4:D1	D0
Name	T3	T4	-
Default	000	0000	0

Auto Breath Control Register 2 set the T3&T4 time in Auto Breath Mode.

T3 T3 Setting

PFS / T3	000(s)	010(s)	001(s)	011(s)	100(s)
000	0.21	0.07	0.42	0.84	1.68
001	0.42	0.14	0.84	1.68	3.36
010	0.84	0.28	1.68	3.36	6.72
011	1.68	0.56	3.36	6.72	13.44
100	3.36	1.12	6.72	13.44	26.88
101	6.72	2.24	13.44	26.88	53.76
110	13.44	4.48	26.88	53.76	107.52
111	26.88	8.96	53.76	107.52	215.04

T4 T4 Setting

PFS / T4	000(s)	010(s)	001(s)	011(s)	100(s)
0000	0	0	0	0	0
0001	0.21	0.07	0.42	0.84	1.68
0010	0.42	0.14	0.84	1.68	3.36
0011	0.84	0.28	1.68	3.36	6.72
0100	1.68	0.56	3.36	6.72	13.44
0101	3.36	1.12	6.72	13.44	26.88
0110	6.72	2.24	13.44	26.88	53.76
0111	13.44	4.48	26.88	53.76	107.52
1000	26.88	8.96	53.76	107.52	215.04
1001	53.76	17.92	107.52	215.04	430.08
1010	107.52	35.84	215.04	430.08	860.16
Others	Unavailable				

Note: Do not set T4= "0000" in Auto Breath Mode when the PWM frequency is 26.7kHz (PFS= "010").

Table 17 04h, 08h, 0Ch Auto Breath Control Register 3 of ABM-x

Bit	D7:D6	D5:D4	D3:D0
Name	LE	LB	LTA
Default	00	00	0000

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

For the counting of breathing times, do follow Figure 16 to enable the Auto Breath Mode.

If the loop start from T4,

T4->T1->T2->T3(1)->T4->T1->T2->T3(2)->T4->T1->... and so on.

If the loop not start from T4,

Tx->T3(1) ->T4->T1->T2->T3(2)->T4-> T1->... and so on.

If the loop ends at off state (End of T3), the LED will be off state at last. If the loop ends at on state (End of T1), the LED will run an extra T4&T1, which are not included in loop.

LB Loop Beginning Time
00 Loop begin from T1
01 Loop begin from T2
10 Loop begin from T3
11 Loop begin from T4

LE Loop End Time
00 Loop end at off state (End of T3)
01 Loop end at on state (End of T1)
Others Unavailable

LTA 8-11 Bits Of Loop Times
0000 Endless loop
0001 1
0010 2
… …
1111 15

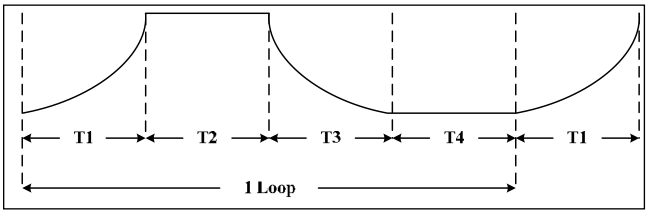


Figure 11 Auto Breathing Function

Table 18 05h, 09h, 0Dh Auto Breath Control Register 4 of ABM-x

Bit	D7:D0
Name	LTB
Default	0000 0000

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

LTB 0-7 Bits Of Loop Times
0000 0000 Endless loop
0000 0001 1
0000 0010 2
… …
1111 1111 255

0Eh Time Update Register (02h~0Dh)

The data sent to the time registers (02h~0Dh) will be stored in temporary registers. A write operation of "0000 0000" data to the Time Update Register is required to update the registers (02h~0Dh). Please follow Figure 16 to enable the Auto Breath mode and update the time parameters.

Table 19 0Fh SWy Pull-Up Resistor Selection Register

Bit	D7:D3	D2:D0
Name	-	PUR
Default	00000	000

Set pull-up resistor for SWy.

PUR SWy Pull-up Resistor Selection Bit
000 No pull-up resistor
001 0.5kΩ pull-up in t_{NOL}
010 0.5kΩ pull-up in t_{NOL}
011 3.0kΩ pull-up all the time
100 4.0kΩ pull-up all the time
101 8.0kΩ pull-up all the time
110 16kΩ pull-up all the time
111 32kΩ pull-up in t_{NOL}

Table 20 10h CSx Pull-Down Resistor Selection Register

Bit	D7:D3	D2:D0
Name	-	PDR
Default	00000	000

Set the pull-down resistor for CSx.

PDR CSx Pull-down Resistor Selection Bit
000 No pull-down resistor
001 0.5kΩ pull-down in t_{NOL}
010 0.5kΩ pull-down in t_{NOL}
011 3.0kΩ pull-down all the time
100 68kΩ pull-down all the time
101 8.0kΩ pull-down all the time
110 16kΩ pull-down all the time
111 32kΩ pull-down in t_{NOL}

11h Reset Register

Once user read the Reset Register, IS31FL3737B will reset all the IS31FL3737B registers to their default value. On initial power-up, the IS31FL3737B registers are reset to their default values for a blank display.

APPLICATION INFORMATION

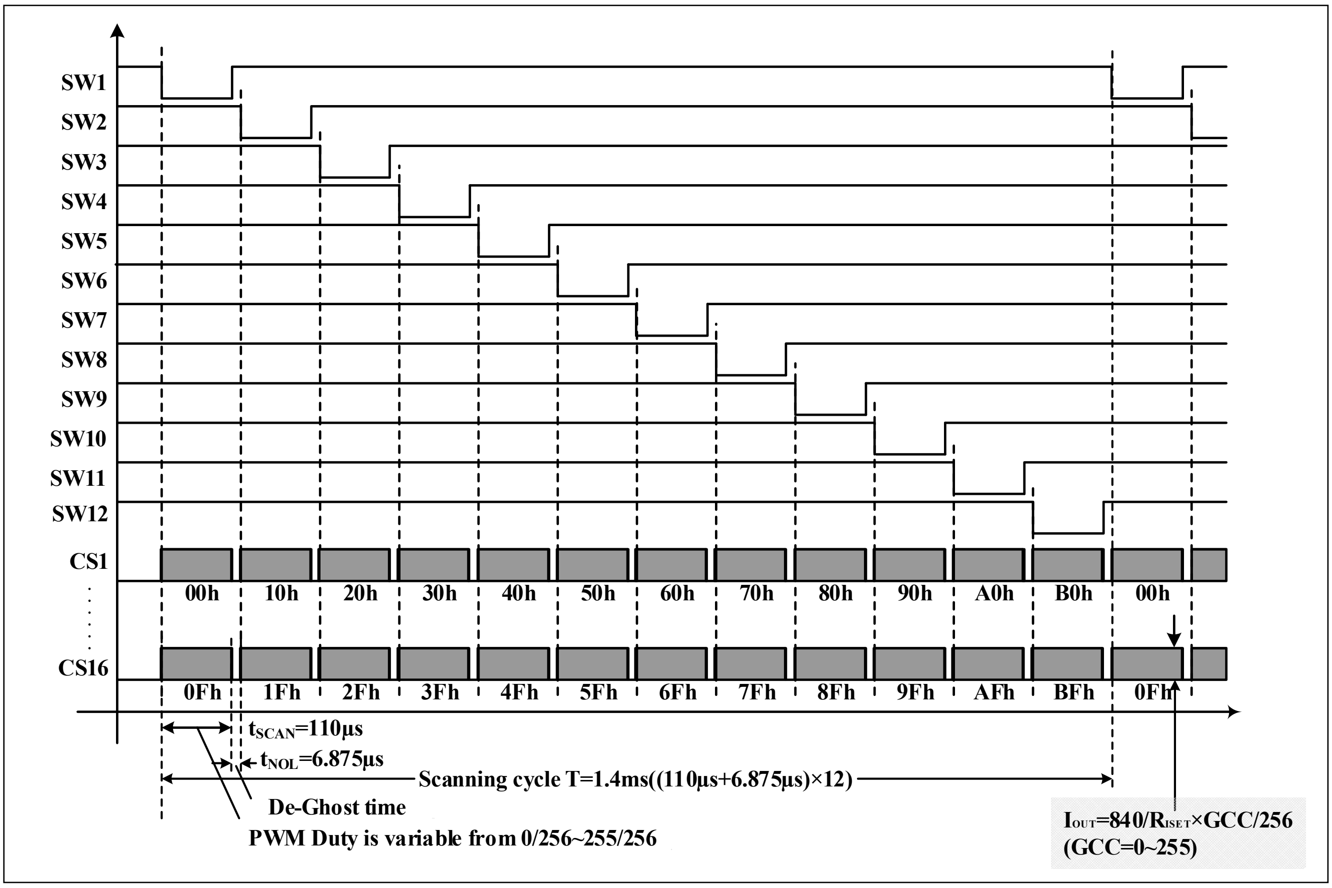


Figure 12 Scanning Timing (PFS="000")

SCANING TIMING

As shown in Figure 12, the SW1~SW12 is turned on by serial, LED is driven 12 by 12 within the SWy (x=1~12) on time (SWy, y=1~12) is sink and pull low when LED on) , including the non-overlap blanking time during scan, the duty cycle of SWy (active low, y=1~12) is (PFS= "000"):

$$Duty = \frac{110\mu s}{(110\mu s + 6.875\mu s)} \times \frac{1}{12} = \frac{1}{12.75} \qquad (2)$$

Where 128μs is t_{SCAN}, the period of scanning and 8μs is t_{NOL}, the non-overlap time.

When PFS="010" or others, the duty result is same.

EXTERNAL RESISTOR (R_{ISET})

The output current for each CSx can be can be set by a single external resistor, R_{ISET}, as described in Formula (3).

$$I_{OUT} = \frac{840}{R_{ISET}} \times \frac{GCC}{256} \qquad (3)$$

GCC is Global Current Control Register (PG3, 01h) data showing in Table 14.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT} \times Duty \qquad (1)$$

Where PWM is PWM Registers (PG1, 00h~BDh) data showing in Table 10.

For example, in Figure 1, R_{ISET} = 20kΩ, if PWM=255, and GCC=255, then

$$I_{LED} = \frac{255}{256} \times \frac{840}{20k\Omega} \times \frac{255}{256} \times \frac{1}{12.75} = 3.27mA$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

LED AVERAGE CURRENT (I_{LED})

As described in Formula (1), the LED average current (I_{LED}) is effected by 3 factors:

1. R_{ISET}, resistor which is connected ISET pin and GND. R_{ISET} sets the current of all CSx (x=1~12) based on Formula (3).

2. Global Current Control Register (PG3, 01h). This register adjusts all CSx (x=1~12) output currents by 256 steps as shown in Formula (3).

3. PWM Registers (PG1, 00h~BFh), every LED has an own PWM register. PWM Registers adjust individual LED average current by 256 steps as shown in Formula (1).

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3737B can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 21 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

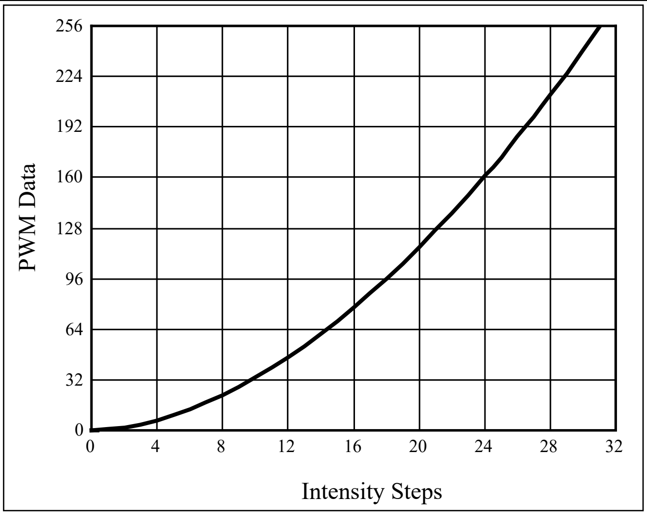


Figure 13 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 22 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

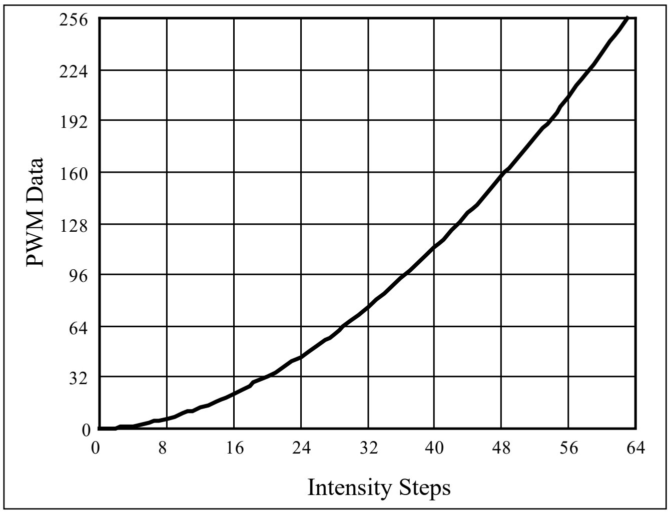


Figure 14 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

Each dot of IS31FL3737B has two selectable operating modes, PWM Mode and Auto Breath Mode.

PWM Mode

By setting the Auto Breath Mode Register bits of the Page 2 (PG2, 00h~BFh) to "00", or disable the B_EN bit of Configure Register (PG3, 00h), the

IS31FL3737B operates in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

Auto Breath Mode

By setting the B_EN bit of the Configuration Register (PG3, 00h) to "1", breath function enables. When set the B_EN bit to "0", breath function disables.

By setting the Auto Breath Mode Register bits of the Page 2 (PG2, 00h~BFh) to "01" (ABM-1), "10" (ABM-2) or "11" (ABM-3), the IS31FL3737B operates in Auto Breath Mode.

IS31FL3737B has three auto breath modes, Auto Breath Mode 1, Auto Breath Mode 2 and Auto Breath Mode 3. Each ABM has T1, T2, T3 and T4, as shown below:

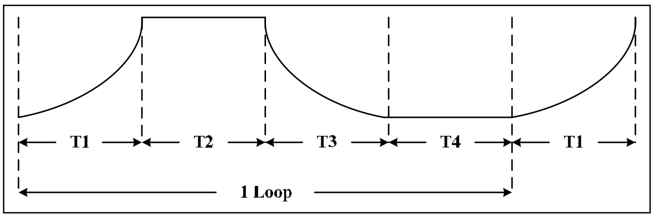


Figure 15 Auto Breathing Function

T1/T3 is variable from 0.21s to 26.88s, T2/T4 is variable from 0s to 26.88s, for each loop, the start point can be T1~T4 and the stop point can be on state (T2) and off state (T4), also the loop time can be set to 1~2^{12} times or endless. Each LED can select ABM-1~ABM-3 to work.

The setting of ABM-1~ABM-3 (PG2, 02h~0Dh) need to write the 0Eh in PG3 to update before effective.

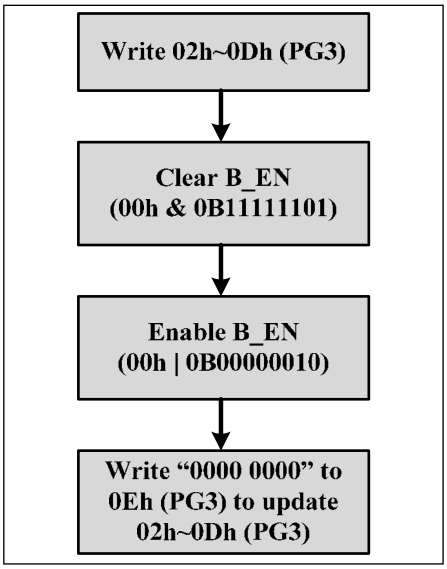


Figure 16 Enable Auto Breath Mode

If not follow this flow, first loop's start point may be wrong.

OPEN/SHORT DETECT FUNCTION

IS31FL3737B has open and short detect bit for each LED.

By setting the OSD bit of the Configuration Register (PG3, 00h) from "0" to "1", the LED Open Register and LED Short Register will start to store the open/short information and after at least 2 scanning cycle (3.264ms) the MCU can get the open/short information by reading the 18h~2fh/30h~47h, for those dots are turned off via LED On/Off Registers (PG0, 00h~17h), the open/short data will not get refreshed when setting the OSD bit of the Configuration Register (PG3, 00h) from "0" to "1".

The Global Current Control Register (PG3, 01h) needs to set to 0x01 in order to get the right open/short data.

The detect action is one-off event and each time before reading out the open/short information, the OSD bit of the Configuration Register (PG3, 00h) need to be set from "0" to "1" (clear before set operation).

INTERRUPT CONTROL

IS31FL3737B has an INTB pin, by setting the Interrupt Mask Register (F0h), it can be the flag of LED open, LED short or the finish flag of ABM-1, ABM-2, and ABM-3.

For example, if the IO bit of the Interrupt Mask Register (F0h) set to "1", when LED open happens, the INTB will pull be pulled low and the OB bit of Interrupt Status Register (F1h) will store open status at the same time.

The INTB pin will be pulled high after reading the Interrupt Status Register (F1h) operation or it will be pulled high automatically after it stays low for 8ms (Typ.) if the IAC bit of Interrupt Mask Register (F0h) is set to "1". The bits of Interrupt Status Register (F1h) will be reset to "0" after INTB pin pulled high.

SYNCHRONIZE FUNCTION

SYNC bits of the Configuration Register (PG3, 00h) sets SYNC pin input or output synchronize clock signal. It is used for more than one part working synchronize. When SYNC bits are set to "01", SYNC pin output synchronize clock to synchronize other parts as master. When SYNC bits are set to "10", SYNC pin input synchronize clock and work synchronization with this input signal as slave. When SYNC bits are set to "00/11", SYNC pin is high impedance, and synchronize function is disabled. SYNC bit default state is "00" and SYNC pin is high impedance when power up.

DE-GHOST FUNCTION

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3737B has integrated pull-up resistors for each SWy (y=1~12) and pull-down resistors for each CSx (x=1~12). Select the right SWy pull-up resistor (PG3, 0Fh) and CSx pull-down resistor (PG3, 10h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 32kΩ will be sufficient to eliminate the LED ghost phenomenon.

The SWy pull-up resistors and CSx pull-down resistors are active only when the CSx/SWy outputs are in the OFF state and therefore no power is lost through these resistors

I2C RESET

The I2C will be reset if the IICRST pin is pull-high, when normal operating the I2C bus, the IICRST pin need to keep low.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG3, 00h) to "0", the IS31FL3737B will operate in software shutdown mode. When the IS31FL3737B is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 3μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 3μA.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

TEST MODE

In order to test or adjust some items of the IC, the IS31FL3737B has some registers in test mode. In test mode, the scanning of the SW can be stopped and some parameters can be adjusted by setting the register bits of certain registers. Test mode is not allowed to enter in normal operations, but in some bad conditions like keep doing EFT (Electrical Fast Transient) test in power system, very low risk that the I2C bus will mis-write those registers and let the IC stop scanning, and keep working in test mode. So we recommend for white goods applications, writing these registers repeatedly like every 5 seconds to prevent the IC entering test mode without quitting.

1. Write FDh with 0x03 enter page 3, if it is in page 3, skip this step.
2. Write E0h with 0xF7 to enter test mode
3. Write E1h with 0x00 to quit the 'SWy stop scanning' status.
4. Write E2h with 0x00 to default value
5. Write E3h with 0x00 to default value
6. Write E0h with 0x00 to quit and prevent entering test mode.

Below tables are definition of test related registers.

Table 23 E0h Test Mode Enable Register

Bit	D7:D0
Name	TEST_PT
Default	0000 0000

Test mode enable register has two functions, first it is the entrance of the test mode, second it also protect the other test registers been miswritten.

TEST_PT Test mode protect bit
1111 0111 Enable test mode, E1h~E3h, 12h can be accessed
Others Disable test mode, E1h~E3h, 12h cannot be accessed

Table 24 E1h Test Mode Data Register 1

Bit	D7:D4	D3:D0
Name	-	SW_S
Default	0000	0000

When normal operation, SW1~SW12 are always scanning as the timing of Figure 12, if SW_S bits are set to "0001"~"0111", SWy stop scanning' status and one of the SWy will be selected as the power output all the time.

SW_S SWy setting
0001 SW1 always on, other SWy float
0010 SW2 always on, other SWy float
0011 SW3 always on, other SWy float
0100 SW4 always on, other SWy float
0101 SW5 always on, other SWy float
0110 SW6 always on, other SWy float
0111 SW7 always on, other SWy float
1000 SW8 always on, other SWy float
1001 SW9 always on, other SWy float
1010 SW10 always on, other SWy float
1011 SW11 always on, other SWy float
1100 SW12 always on, other SWy float

Table 25 E2h Test Mode Data Register 2

Bit	D7:D3	D2:D0
Name	-	TRIM_CS
Default	00000	000

Table 26 E3h Test Mode Data Register 3

Bit	D7:D4	D3:D0
Name	TRIM_BG	TRIM_OSC
Default	0000	0000

Data register 2 and 3 can change the voltage of ISET pin (TRIM_BG), adjust the internal oscillator frequency (TRIM_OSC) and trim the average output current of all CSx (TRIM_CS), when normal operation, these registers must keep default value, otherwise those parameters will be changed permanently.

Table 27 12h Test Mode Data Register 4

Bit	D7:D5	D4	D3:D1	D0
Name	-	TSD_ADJ	-	TSD_SD
Default	000	0	000	0

Test Mode Data Register 4 stores thermal shutdown function bit and can change the thermal shutdown temperature.

TSD_ADJ Thermal shutdown temperature adjust bit
0 T_{SD} = 160°C
1 T_{SD} = 160°C + 16°C

TSD_SD Thermal shutdown function disable bit
0 Thermal shutdown function enable
1 Thermal shutdown function disable

POWER DISSIPATION

The power dissipation of the IS31FL3737B can calculate as below:

$$P_{3737B}=I_{PVCC}\times PV_{CC}+ I_Q\times DV_{CC}(AV_{CC}) - I_{PVCC}\times V_{F(AVR)} \quad (4)$$

$$\approx I_{PVCC}\times PV_{CC} - I_{PVCC}\times V_{F(AVR)}$$

$$\approx I_{PVCC}\times (PV_{CC} - V_{F(AVR)})$$

Where I_{PVCC} is the current of PVCC and $V_{F(AVR)}$ is the average forward of all the LED.

For example, if R_{ISET}=20kΩ, GCC=255, PWM=255, PV_{CC}=5V, $V_{F(AVR)}$=3.5V@42mA, then the I_{PVCC}=42mA×12×12/12.75=474.4mA.

P_{3737B}=474.4mA ×(5V-3.5V)=0.806W

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (5):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \quad (5)$$

So, $$P_{D(MAX)} = \frac{125°C - 25°C}{31°C/W} \approx 3.26W$$

Figure 17 shows the power derating of the IS31FL3737B on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

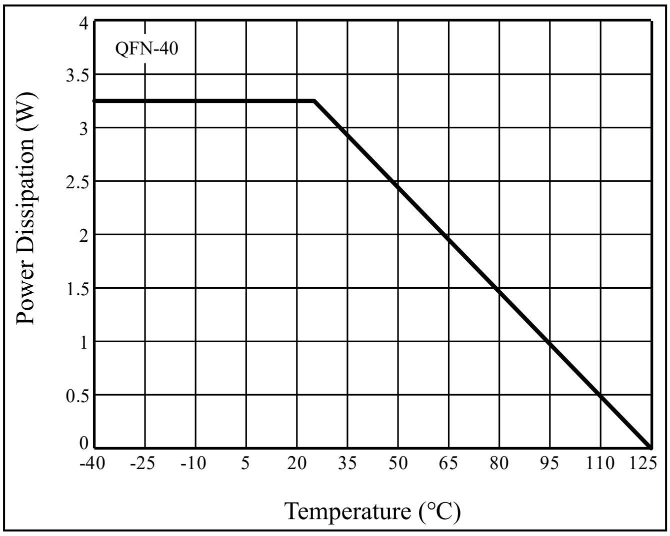


Figure 17 Dissipation Curve

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, DVCC, AVCC, VIO) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side's ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSx pins maximum current is 42mA (R_{ISET}=20kΩ), and the SWy pins maximum current is 672mA (R_{ISET}=20kΩ), the width of the trace, SWy should have wider trace then CSx.

5. In the middle of SDA and SCL trace, a ground line is recommended to avoid the effect between these two lines.

PWM FREQUENCY SELECT

The IS31FL3738B output channels operate with a default PWM frequency of 8.4kHz. Because all the CSx channels are synchronized, the DC supply will experience large instantaneous current surges when the CSx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors.

When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3737B's output PWM frequency above the audible range. The Output Frequency Setting Register (00h)'s bit D4 can be used to set the switching frequency to 26.7kHz, which is beyond the audible range. Figure 18 below shows the variation of output PWM frequency across supply voltage and temperature.

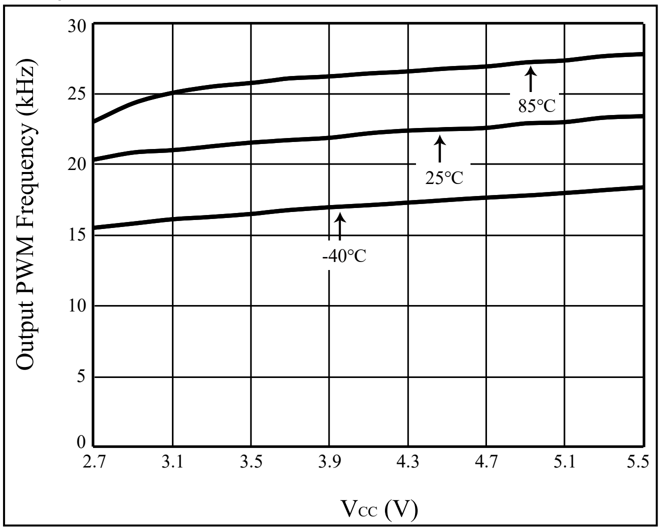


Figure 18 V_{CC} vs. CSx PWM Frequency

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

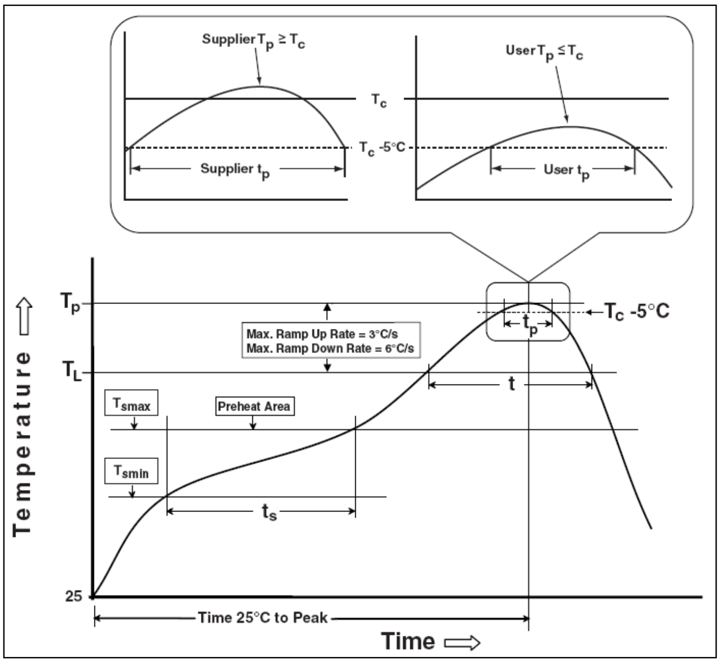
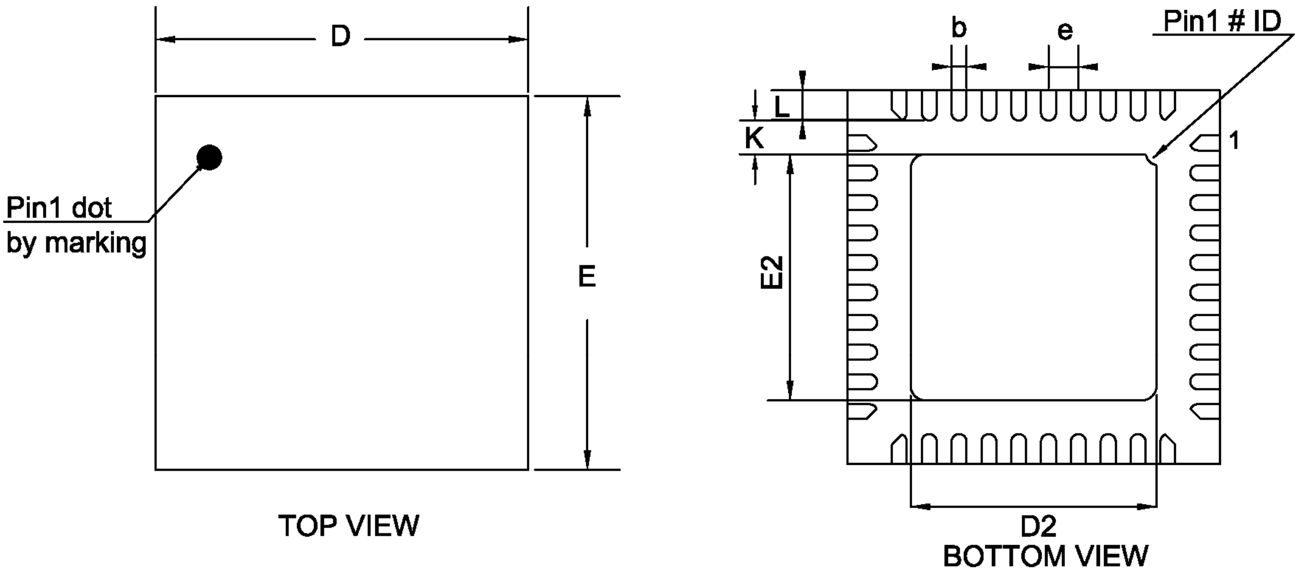
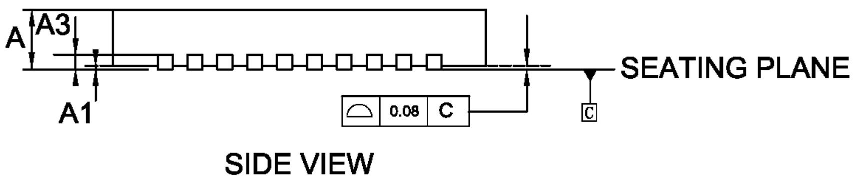


Figure 19 Classification Profile

PACKAGE INFORMATION

QFN-40





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.25
K	0.20	-	-
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.15	-	3.80
E2	3.15	-	3.80
L	0.30	0.40	0.50
e	0.40BSC		

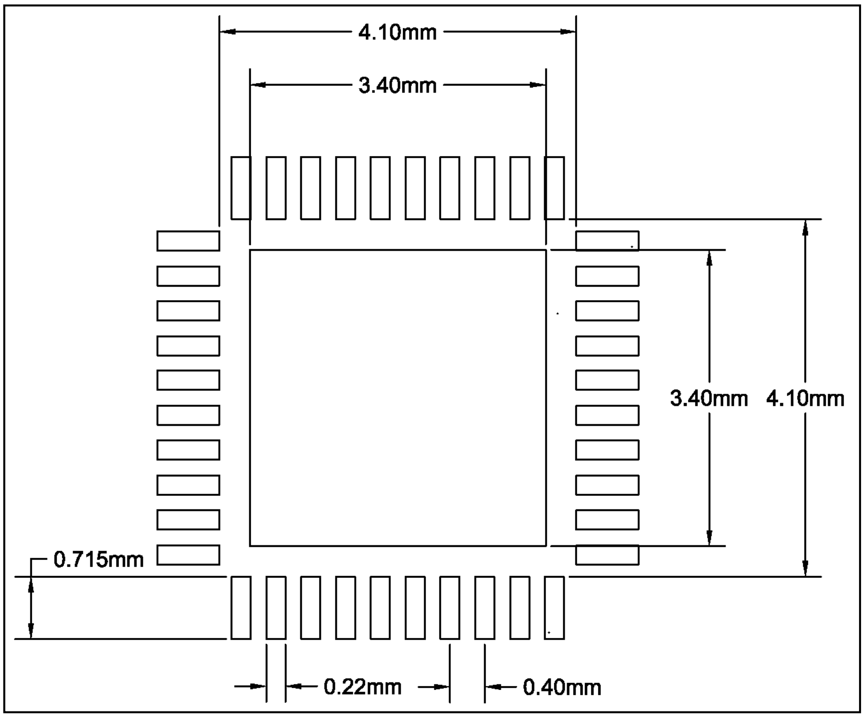
233-570-291 Rev.B

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-40



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
00A	Initial release	2019.07.11
0A	Update PWM Frequency Setting	2019.09.03
A	Release to mass production	2019.11.06
B	Correct PUR bit's mistake	2020.10.23
C	1. Add Note for T4 setting 2. Add revision for POD	2022.02.21