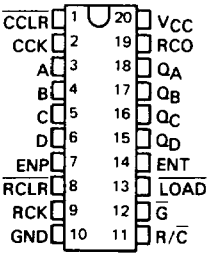
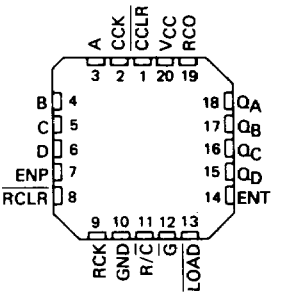
- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . Decade Counter, Direct Clear
  'LS691 . . Binary Counter, Direct Clear
  'LS692 . . Decade Counter, Synchronous Clear
  'LS693 . . Binary Counter, Synchronous Clear

SN54LS690 THRU SN54LS693 . . . J PACKAGE
SN74LS690 THRU SN74LS693 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS690 THRU SN54LS693 . . . FK PACKAGE
SN74LS690 THEU SN74LS693 . . . FN PACKAGE
(TOP VIEW)



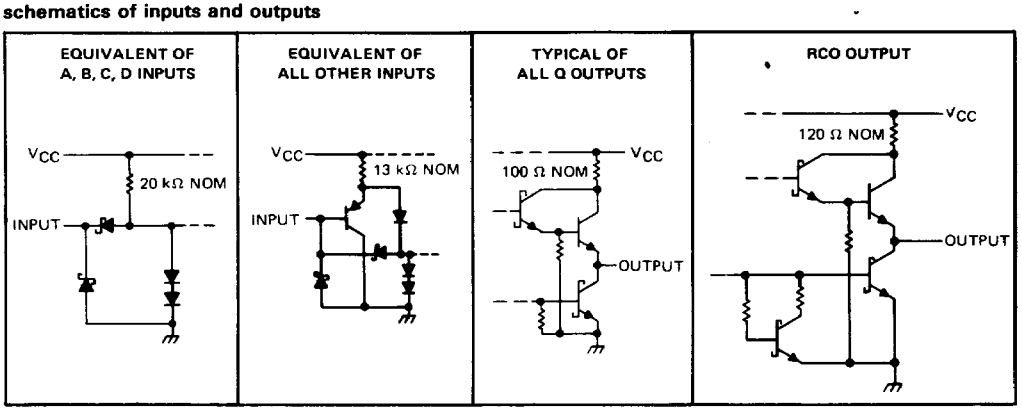
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P inputs and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

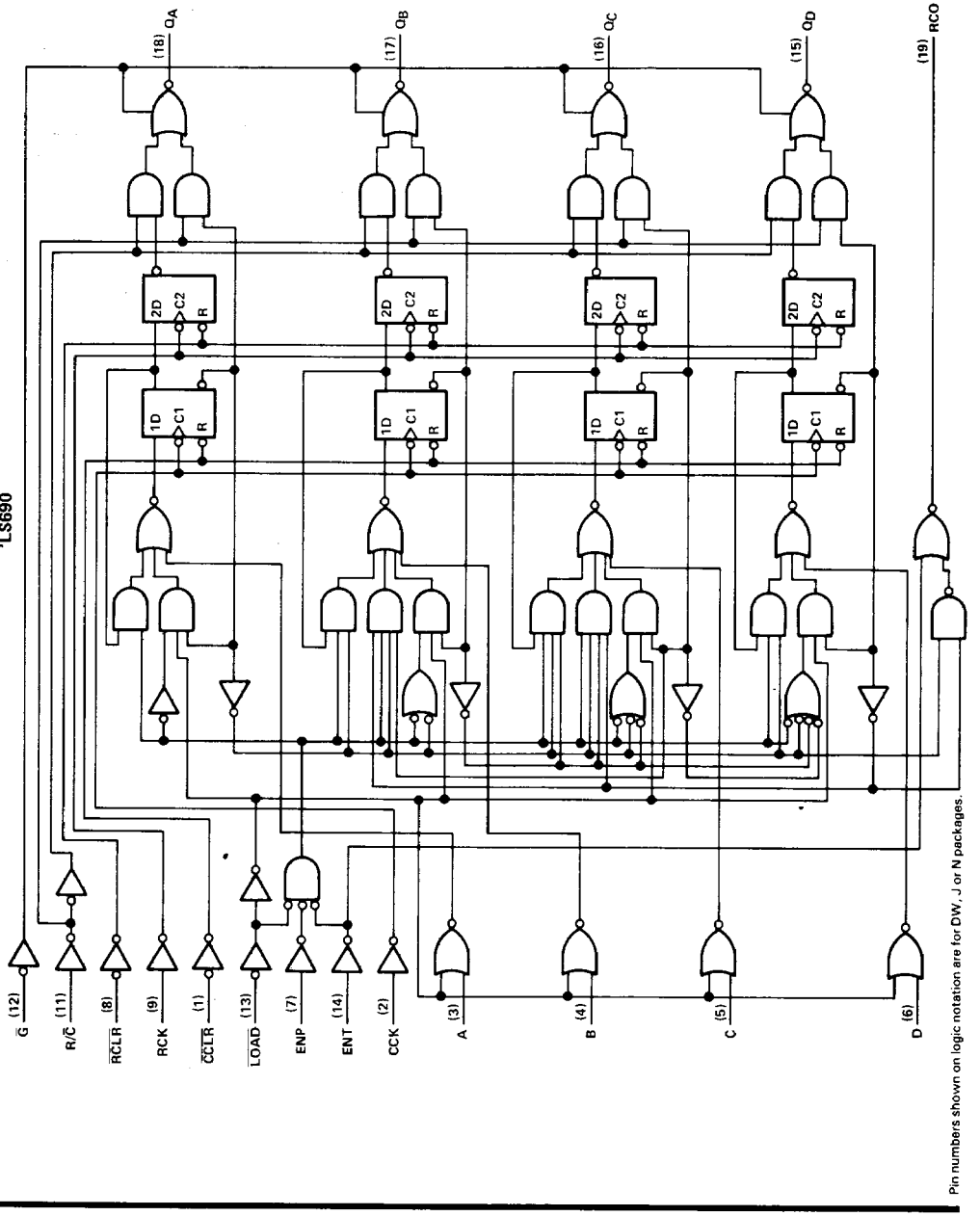
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered: The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS692 and 'LS693. Loading of the counter is accomplished when $\overline{LOAD}$ is taken low and a positive-transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting RCO of the first stage to ENT of the second stage, etc. All ENP inputs can be tied common and used as a master enable or disable control.

schematics of inputs and outputs



logic diagrams



Pin numbers shown on logic notation are for DW, J or N packages.

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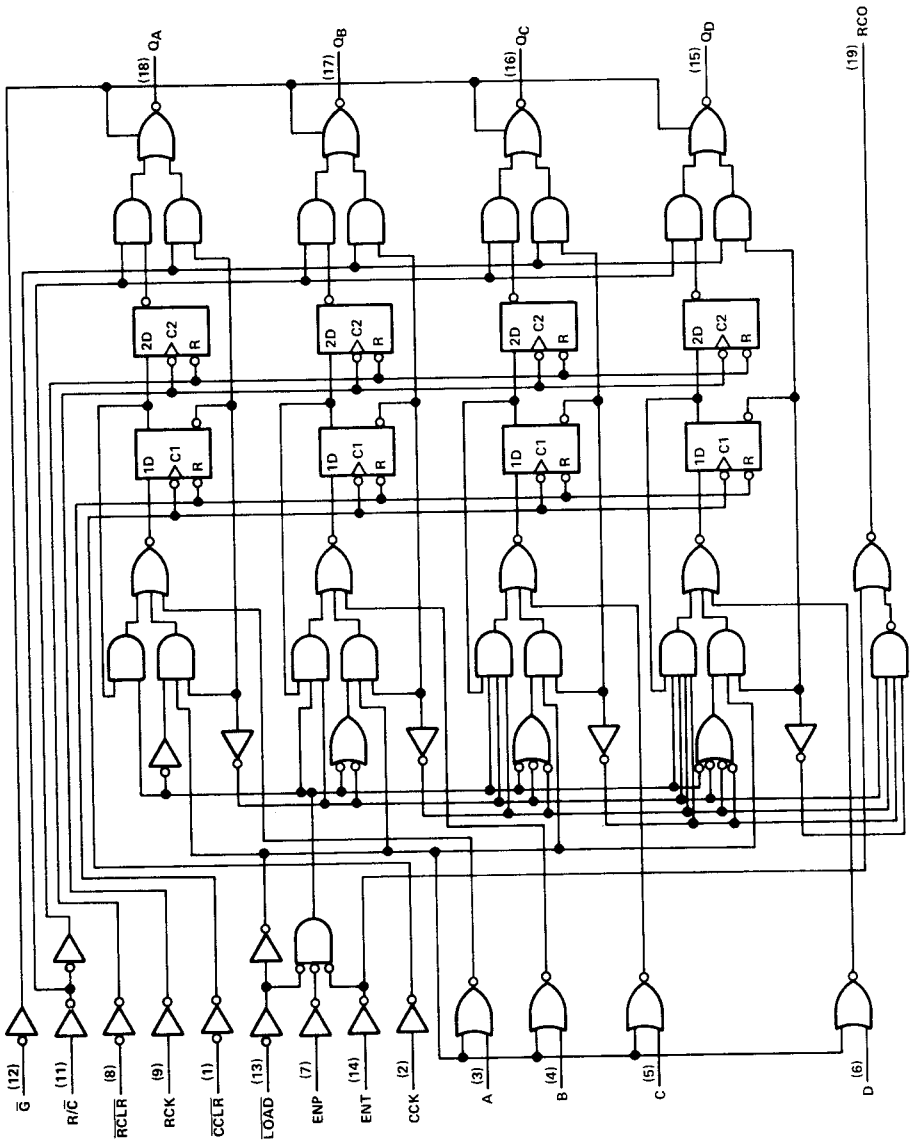
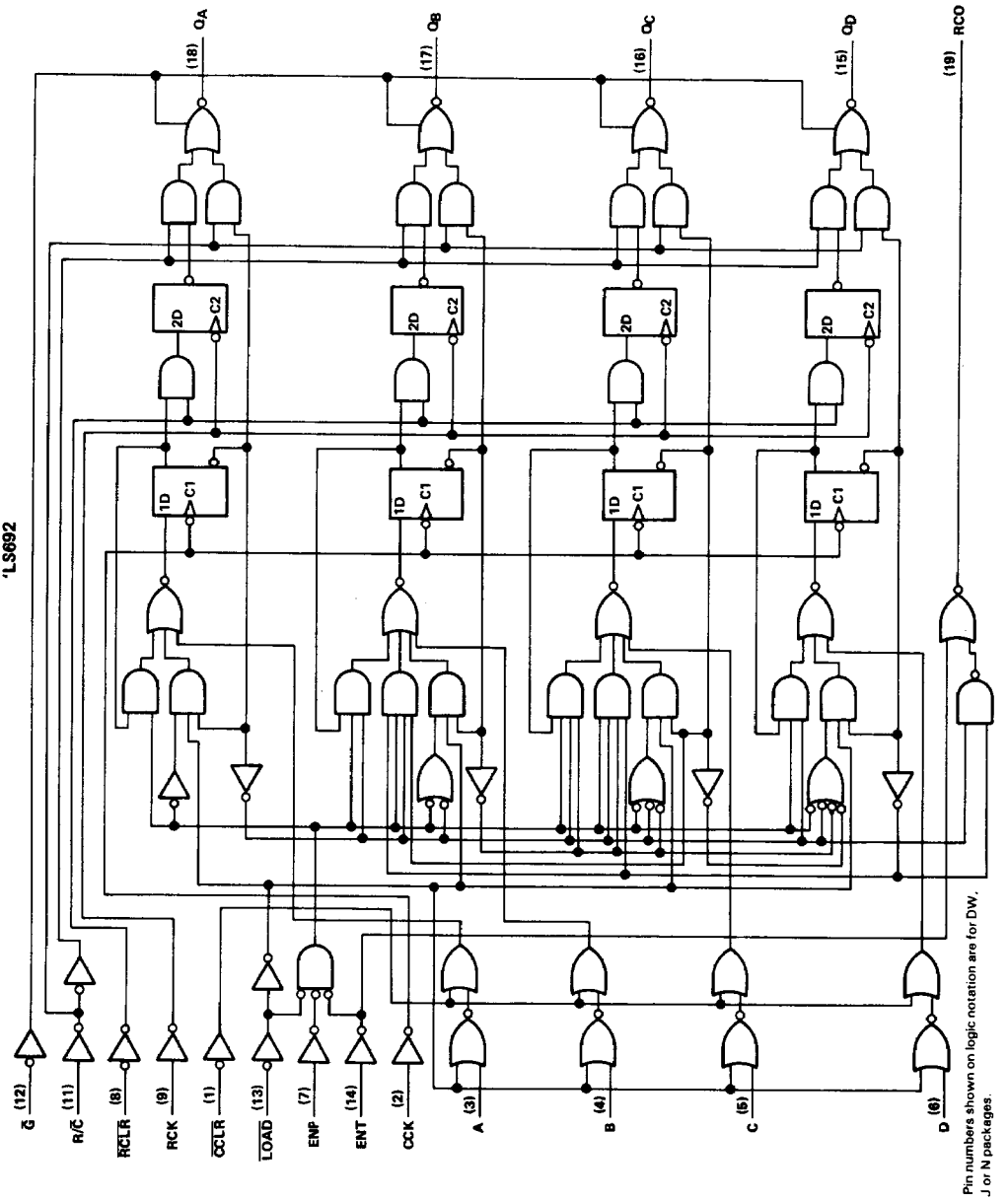
logic diagrams (continued)

'LS691



Pin numbers shown on logic notation are for DW, J or N packages.

logic diagrams (continued)



Pin numbers shown on logic notation are for DW, J or N packages.

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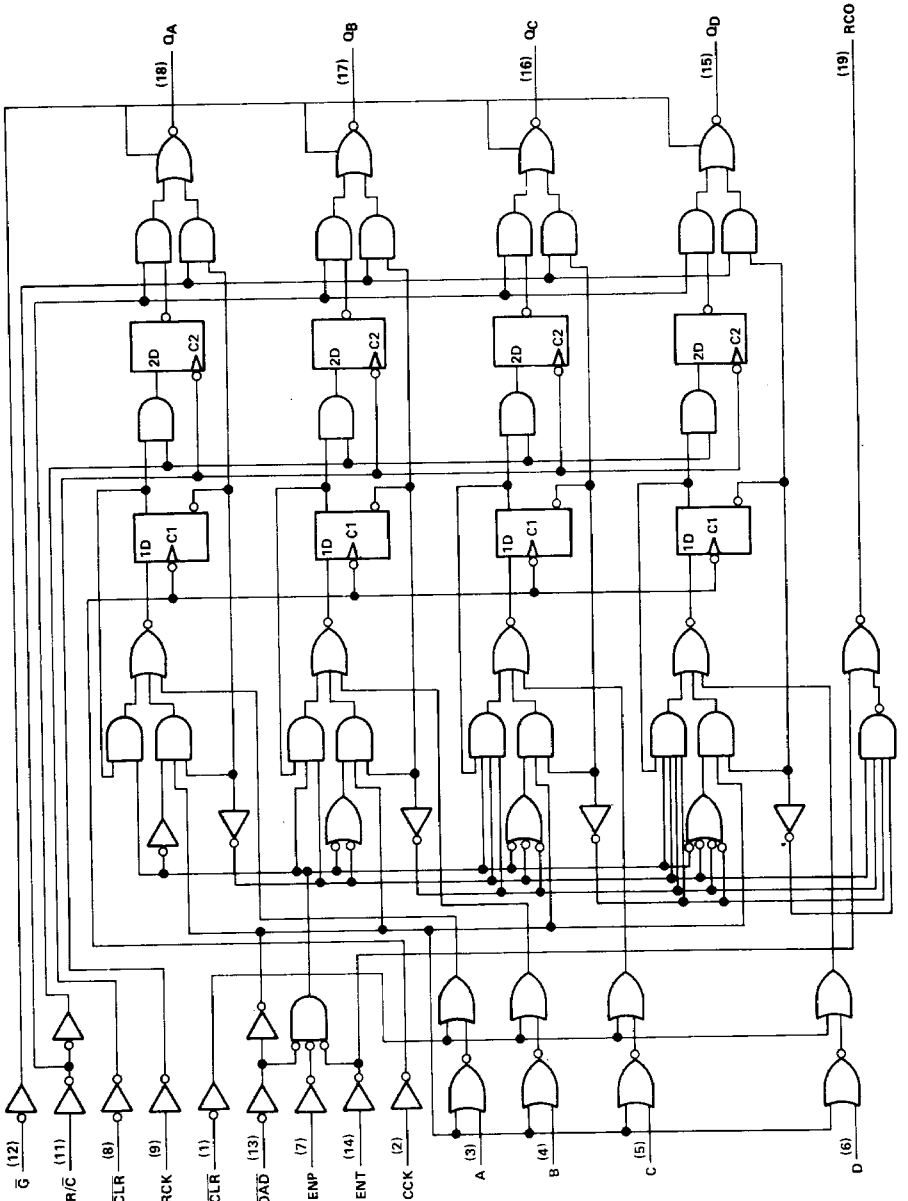
logic diagrams (continued)

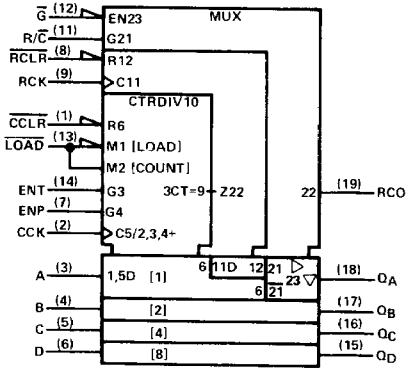
'LS693



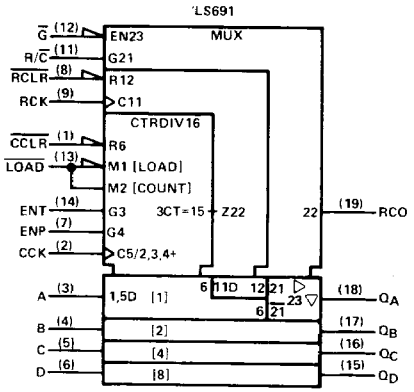
Pin numbers shown on logic notation are for DW, J or N packages.

logic symbols

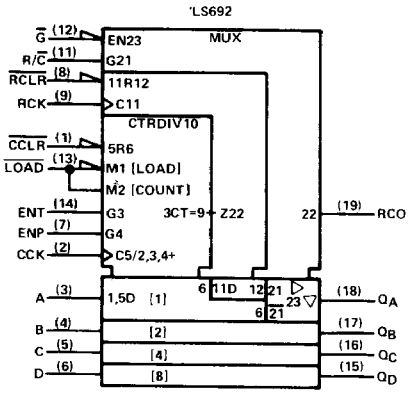
'LS690



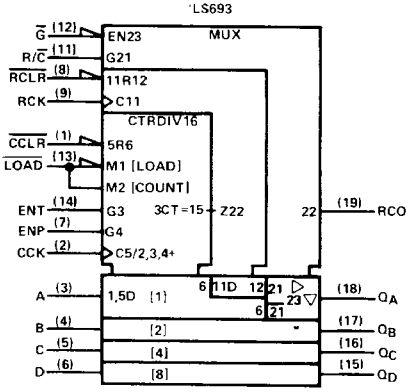
'LS691



'LS692



'LS693



Pin numbers shown on logic notation are for DW, J or N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS690 thru SN54LS693 . . . . . −55°C to 125°C
SN74LS690 thru SN74LS693 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current		Q			−1			−2.6	mA
			RCO			−0.4			−0.4	mA
I_{OL}	Low-level output current		Q			12			24	mA
			RCO			4			8	mA
f_{clock}	Clock frequency		CCK	0		20	0		20	MHz
			RCK	0		20	0		20	MHz
t_w	Pulse duration		CCK high or low	25			25			ns
			RCK high or low	25			25			
		'LS690, 'LS691	$\overline{RCLR}$ low	20			20			
			$\overline{CCLR}$ low	20			20			
t_{su}	Setup time before CCK ↑		A thru D	30			30			ns
			ENP or ENT	30			30			
			$\overline{LOAD}$ ↓	30			30			
		'LS692, 'LS693	$\overline{CCLR}$ ↓	40			40			
		'LS690, 'LS691	$\overline{CCLR}$ ↑ inactive	25			25			
t_{su}	Setup time before RCK ↑		CCK ↑ (see Note 2)	30			30			ns
		'LS690, 'LS691	$\overline{RCLR}$ ↑ inactive	25			25			
		'LS692, 'LS693	RCLR ↓	20			20			
th	Hold time	Any input from CCK ↑ or RCK ↑		0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	Any Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −1 mA	2.4	3.1					V
	Any $\overline{Q}$		I_{OH} = −2.6 mA				2.4	3.1		
	RCO		I_{OH} = −0.4 mA	2.5	3.2		2.7	3.2		
V_{OL}	Any Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	Any $\overline{Q}$		I_{OL} = 24 mA					0.35	0.5	
	RCO		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
	RCO		I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Any Q	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 2.7 V				20			20	μA
I_{OZL}	Any Q	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 0.4 V				−20			−20	μA
I_I		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	A thru D	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_{OS}§	Any Q	V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
	RCO			−20		−100	−20		−100	
I_{CCH}		V_{CC} = MAX, All outputs open	See Note 3		46	65		46	65	mA
I_{CCL}			See Note 4		48	70		48	70	
I_{CCZ}			See Note 5		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTES: 3. I_{CCH} is measured after two 4.5-V to 0-V to 4.5-V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.
4. I_{CCL} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while all other inputs are grounded.
5. I_{CCZ} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

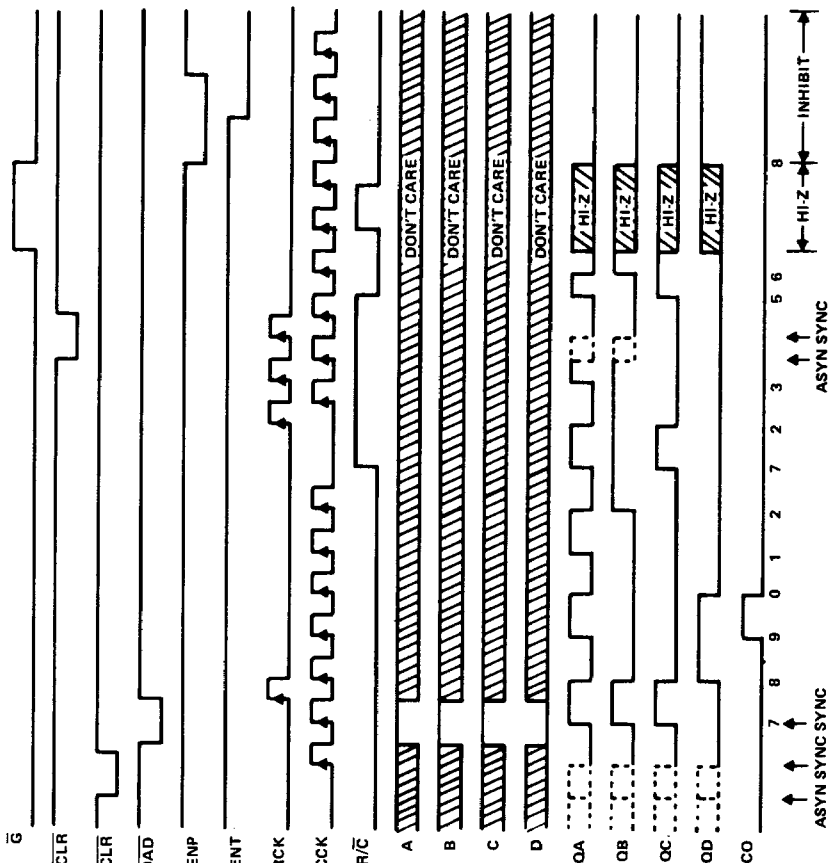
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS690, 'LS691			'LS692, 'LS693			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CCK↑	RCO	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	
t_{PLH}	ENT	RCO			13	20		13	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PHL}	$\overline{RCLR}$↓	Q			20	30				ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	

NOTE 6: See General Information Section for load circuits and voltage waveforms.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

typical operating sequences

'LS690 DECADE COUNTER, Asynchronous Clear
'LS692 DECADE COUNTER, Synchronous Clear



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typical operating sequences (continued)

'LS691 BINARY COUNTER, Asynchronous Clear
'LS693 BINARY COUNTER, Synchronous Clear