



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1 24	DIV_SELB0 DIV_SELB1	Input	Pulldown	Division select pin for Bank B. Default = Low. LVCMOS/LVTTL interface levels.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or TEST_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V <sub>DDO_A</sub>	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
7	OEB	Input	Pullup	Output enable Bank B. Active High outputs are enable. When logic HIGH, the output pairs on Bank B are enabled. When logic LOW, the output pairs are in a high impedance state. Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
8	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the output pair in Bank A is enabled. When logic LOW, the output pair is in a high impedance state. Has an internal pullup resistor so the default power-up state of output is enabled. LVCMOS/LVTTL interface levels.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷20. When HIGH, the feedback divider is set for ÷24. LVCMOS/LVTTL interface levels.
10	V <sub>DDA</sub>	Power		Analog supply pin.
11	V <sub>DD</sub>	Power		Core supply pin.
12 13	DIV_SELA0 DIV_SELA1	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
14	GND	Power		Power supply ground.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	TEST_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended TEST_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
21, 22	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
23	V <sub>DDO_B</sub>	Power		Output supply pin for Bank B outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

TABLE 3A. BANK A FREQUENCY TABLE

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELA1	DIV_SELA0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	64.8	125

TABLE 3B. BANK B FREQUENCY TABLE

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB0/nQB0 Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELB1	DIV_SELB0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

TABLE 3C. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs	Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA	DIV_SELB1	DIV_SELB0	QB
0	0	÷1	0	0	÷1
0	1	÷2	0	1	÷2
1	0	÷4	1	0	÷4
1	1	÷5	1	1	÷5

TABLE 3D. FEEDBACK DIVIDER CONFIGURATION SELECT FUNCTION TABLE

Inputs	
FB_DIV	Feedback Divide
0	÷20
1	÷24

TABLE 3E. OEA SELECT FUNCTION TABLE

Inputs	Outputs	
OEA	QA0	nQA0
0	LOW	HIGH
1	Active	Active

TABLE 3F. OEB SELECT FUNCTION TABLE

Inputs	Outputs	
OEB	QB0:QB1	nQB0:nQB1
0	LOW	HIGH
1	Active	Active

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, $\theta_{JA}$	70°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	$V_{DD}$	V
$V_{DDO\_A,B}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current			99		mA
$I_{DDA}$	Analog Supply Current			10		mA
$I_{DDO\_A,B}$	Output Supply Current			52		mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	TEST_CLK, MR, FB_DIV DIV_SELA1, DIV_SELB0 $V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
		DIV_SELB1, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB $V_{DD} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	TEST_CLK, MR, FB_DIV DIV_SELA1, DIV_SELB0 $V_{DD} = 3.465V, V_{IN} = 0V$	-5			$\mu A$
		DIV_SELB1, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB $V_{DD} = 3.465V, V_{IN} = 0V$	-150			$\mu A$

TABLE 4C. LVDS DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = T_C = 0^\circ\text{C}$  TO  $70^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage			350		mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			0	40	mV
$V_{OS}$	Offset Voltage			1.4		V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			0	50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency	FB_DIV = $\pm 20$	28		35	MHz
	FB_DIV = $\pm 24$	23.33		29.16	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency Range	Output Divider = $\div 1$	560		700	MHz
		Output Divider = $\div 2$	280		350	MHz
		Output Divider = $\div 4$	140		175	MHz
		Output Divider = $\div 5$	112		140	MHz
$t_{sk}(b)$	Bank Skew, NOTE 1			3	ps	
$t_{sk}(o)$	Output Skew; NOTE 2, 4	Outputs @ Same Frequency		15		ps
		Outputs @ Different Frequencies		30		ps
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 3	625MHz (1.875MHz - 20MHz)		0.55		ps
		312.5MHz (1.875MHz - 20MHz)		0.59		ps
		156.25MHz (1.875MHz - 20MHz)		0.63		ps
		125MHz (1.875MHz - 20MHz)		0.64		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		325		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

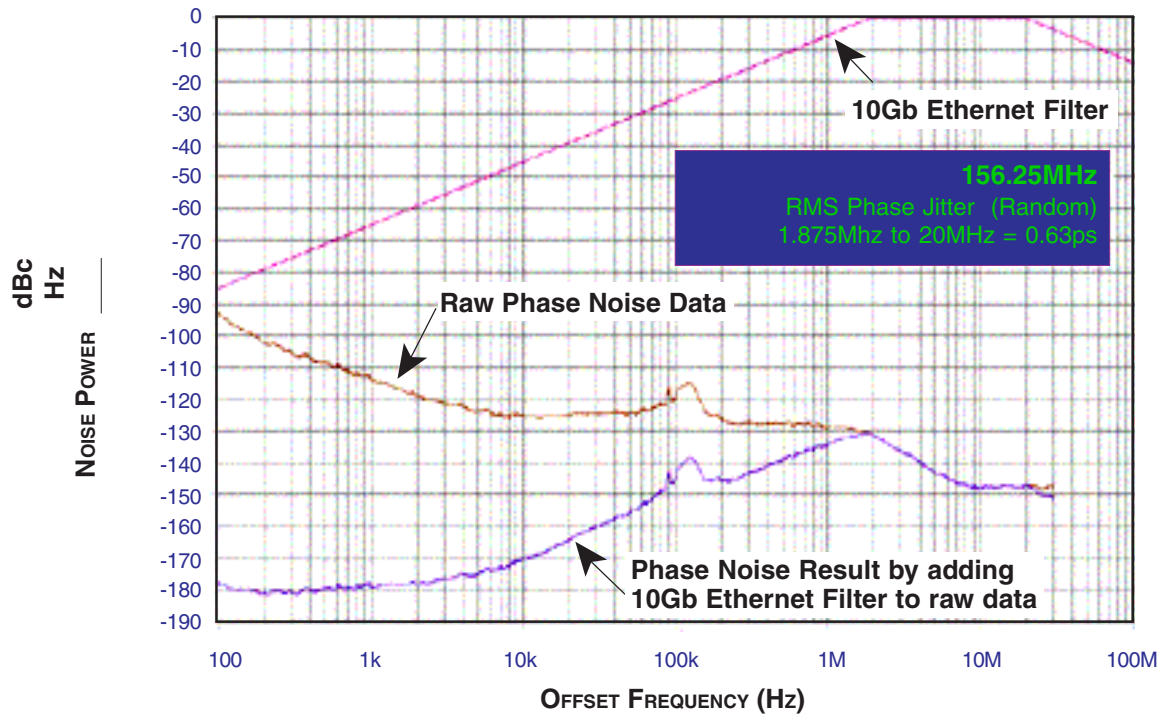
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at the output differential cross points.

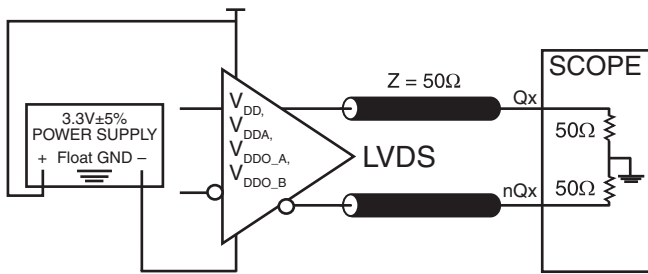
NOTE 3: Please refer to the Phase Noise Plots.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

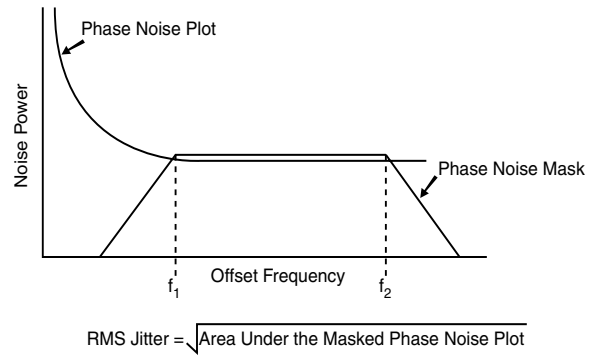
### TYPICAL PHASE NOISE AT 156.25MHz



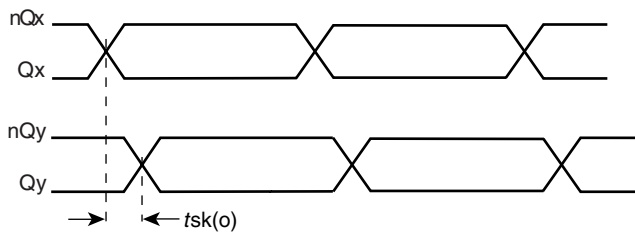
# PARAMETER MEASUREMENT INFORMATION



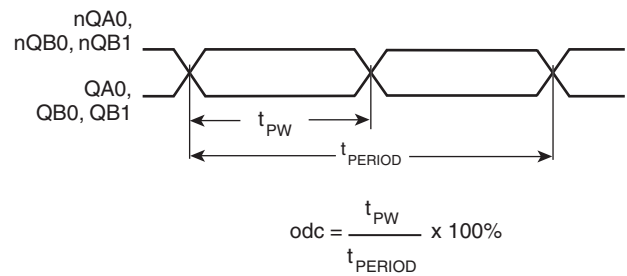
**LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT**



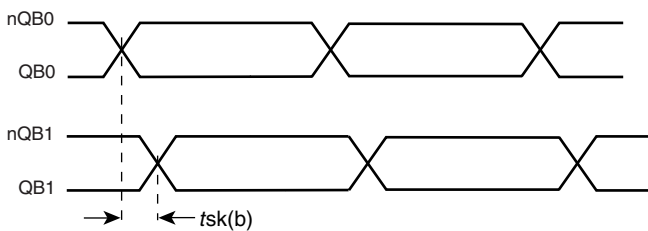
**RMS PHASE JITTER**



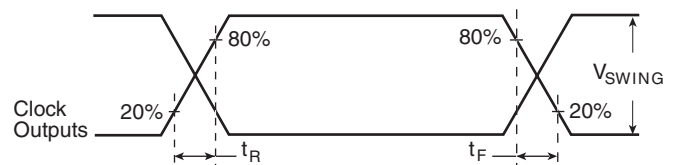
**OUTPUT SKEW**



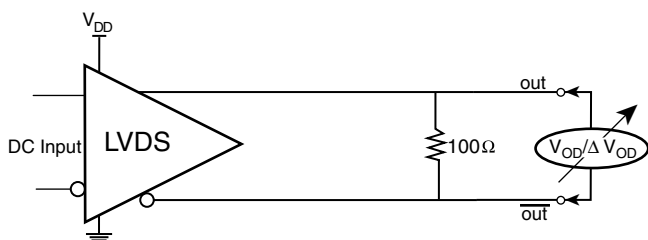
**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



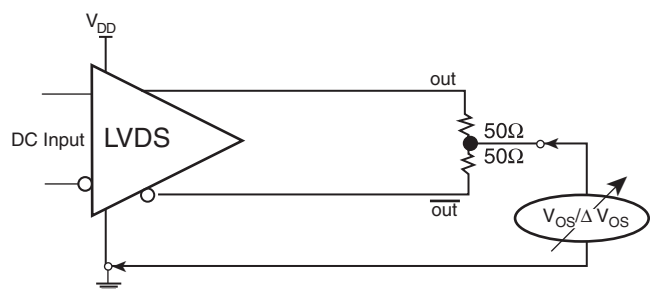
**BANK SKEW**



**OUTPUT RISE/FALL TIME**



**DIFFERENTIAL OUTPUT VOLTAGE SETUP**



**OFFSET VOLTAGE SETUP**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844003 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDOX}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$  pin.

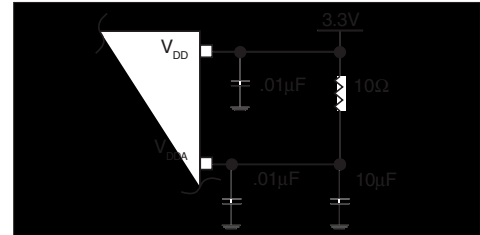


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The ICS844003 has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a  $31.25\text{MHz}$  or  $26.041666\text{MHz}$ ,  $18\text{pF}$

parallel resonant crystal and were chosen to minimize the ppm error.

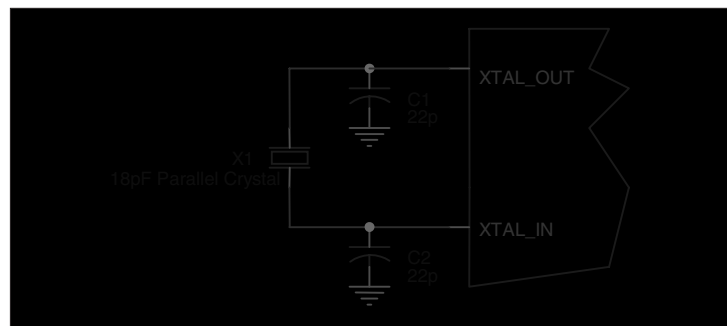


Figure 2. CRYSTAL INPUT INTERFACE

## LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ .

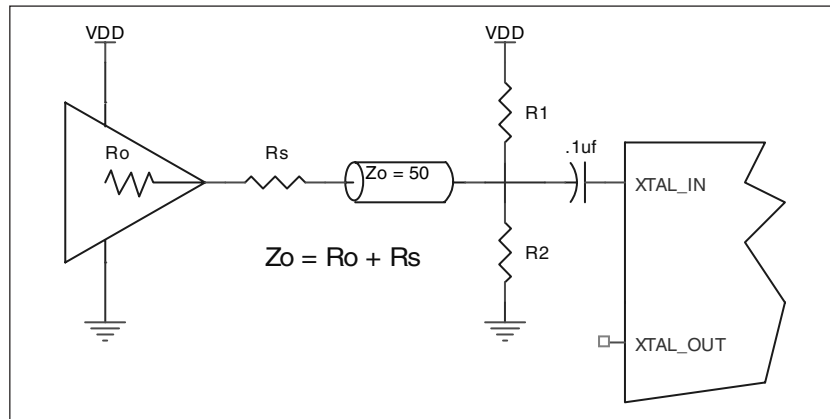


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1k\Omega$  resistor can be tied from XTAL\_IN to ground.

#### TEST\_CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a  $1k\Omega$  resistor can be tied from the TEST\_CLK to ground.

#### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1k\Omega$  resistor can be used.

### OUTPUTS:

#### LVDS

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, we recommend that there is no trace attached.

### 3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers

require a matched load termination of 100Ω across near the receiver input.

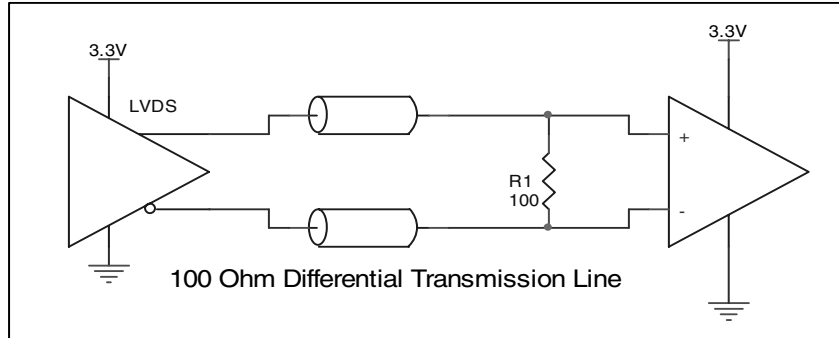


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844003. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS844003 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (99mA + 10mA) = 377.68mW$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 52mA = 180.18mW$

$$\text{Total Power}_{\_MAX} = 377.68mW + 180.18mW = 557.86mW$$

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7 below.

Therefore, T<sub>j</sub> for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.558\text{W} * 65^\circ\text{C}/\text{W} = 105.9^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 24-LEAD TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 24 LEAD TSSOP, EPAD

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

### TRANSISTOR COUNT

The transistor count for ICS844003 is: 3394

## PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

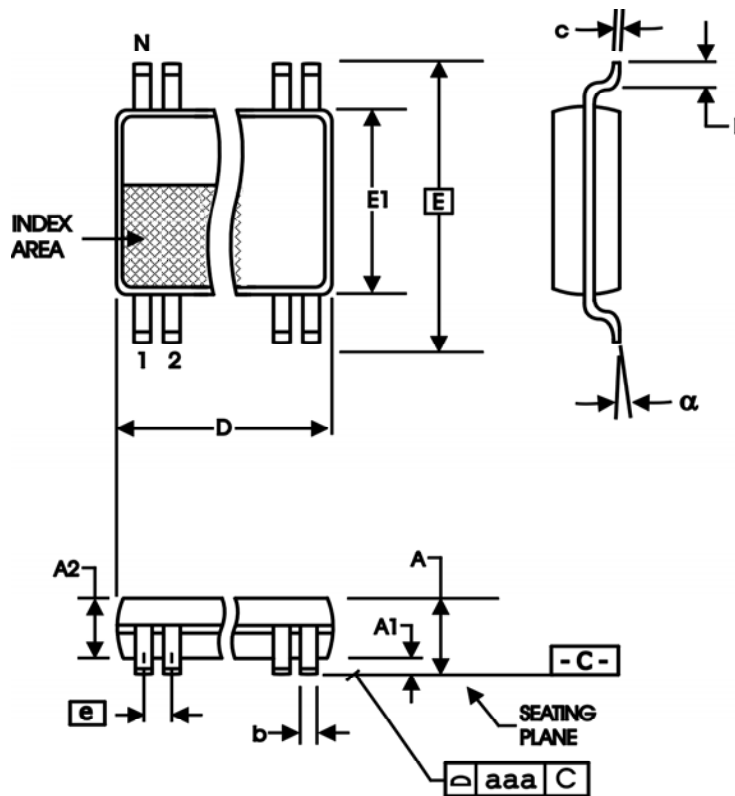


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844003AG	ICS844003AG	24 Lead TSSOP	tube	0°C to 70°C
ICS844003AGT	ICS844003AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS844003AGLF	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS844003AGTLF	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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