HARRIS

# RFL1N12L
# RFL1N15L

## N-Channel Logic Level Power Field-Effect Transistors ($L^2FET$)

August 1991

### Features

- 1A, 120V and 150V
- $r_{DS(ON)} = 1.9\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

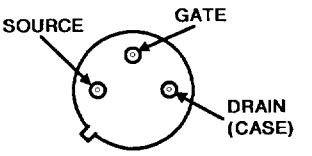
### Description

The RFL1N12L and RFL1N15L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

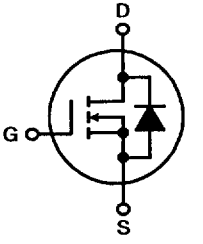
### Package

TO-205AF
BOTTOM VIEW




### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE




**Absolute Maximum Ratings** ($T_C = +25^oC$) Unless Otherwise Specified

| | | RFL1N12L | RFL1N15L | UNITS |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 120 | 150 | V |
| Drain-Gate Voltage ($R_{GS} = 1M\Omega$) | $V_{DGR}$ | 120 | 150 | V |
| Continuous Drain Current | | | | |
| RMS Continuous | $I_D$ | 1 | 1 | A |
| Pulsed Drain Current | $I_{DM}$ | 5 | 5 | A |
| Gate-Source Voltage | $V_{GS}$ | ±10 | ±10 | V |
| Maximum Power Dissipation | | | | |
| $T_C = +25^oC$ | $P_D$ | 8.33 | 8.33 | W |
| Above $T_C = +25^oC$, Derate Linearly | | 0.0667 | 0.0667 | W/°C |
| Operating and Storage Junction Temperature Range | TJ, TSTG | -55 to +150 | -55 to +150 | °C |



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.



File Number **1513.1**

**Electrical Characteristics** ($T_C$ = +25°C), Unless Otherwise Specified

| CHARACTERISTIC | SYMBOLS | TEST CONDITIONS | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | RFL1N12L | | RFL1N15L | | |
| | | | MIN | MAX | MIN | MAX | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 1mA, $V_{GS}$ = 0 | 120 | - | 150 | - | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 2mA | 1 | 2 | 1 | 2 | V |
| Zero-Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 100V | - | 1 | - | - | μA |
| | | $V_{DS}$ = 120V | - | - | - | 1 | μA |
| | | $T_C$ = +125°C<br>$V_{DS}$ = 100V | - | 50 | - | - | μA |
| | | $V_{DS}$ = 120V | - | - | - | 50 | mA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±10V, $V_{DS}$ = 0 | - | 100 | - | 100 | nA |
| Drain-Source On-Voltage | $V_{DS(on)}$* | $I_D$ = 1A, $V_{GS}$ = 5V | - | 1.9 | - | 1.9 | V |
| | | $I_D$ = 2A, $V_{GS}$ = 5V | - | 4.6 | - | 4.6 | V |
| Static Drain-Source On Resistance | $r_{DS(on)}$* | $I_D$ = 1A, $V_{GS}$ = 5V | - | 1.9 | - | 1.9 | Ω |
| Forward Transconductance | $g_{fs}$* | $I_D$ = 1A, $V_{DS}$ = 10V | 800 | - | 800 | - | S (℧) |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0V, $V_{DS}$ = 25V<br>f = 1MHz | - | 200 | - | 200 | pF |
| Output Capacitance | $C_{OSS}$ | | - | 80 | - | 80 | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | - | 35 | - | 35 | pF |
| Turn-On Delay Time | $t_{d(on)}$ | $I_D$ = 1A, $V_{DD}$ = 75V<br>$R_{GEN}$ = ∞,<br>$R_{GS}$ = 6.25Ω, $V_{GS}$ = 5V | 10 (typ) | 25 | 10 (typ) | 25 | ns |
| Rise Time | $t_r$ | | 10 (typ) | 45 | 10 (typ) | 45 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | 24 (typ) | 45 | 24 (typ) | 45 | ns |
| Fall Time | $t_f$ | | 30 (typ) | 50 | 30 (typ) | 50 | ns |
| Thermal Resistance Junction-to-Case | $R_{θJC}$ | | - | 15 | - | 15 | °C/W |

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

**Source-Drain Diode Ratings and Characteristics**

| CHARACTERISTIC | SYMBOLS | TEST CONDITIONS | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | RFL1N12L | | RFL1N15L | | |
| | | | MIN | MAX | MIN | MAX | |
| Diode Forward Voltage | $V_{SD}$* | $I_{SD}$ = -1A | - | 1.4 | - | 1.4 | V |
| Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 2A<br>$d_{IF}/dt$ = 50A/μs | 150 (typ) | 150 (typ) | 150 (typ) | 150 (typ) | ns |

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

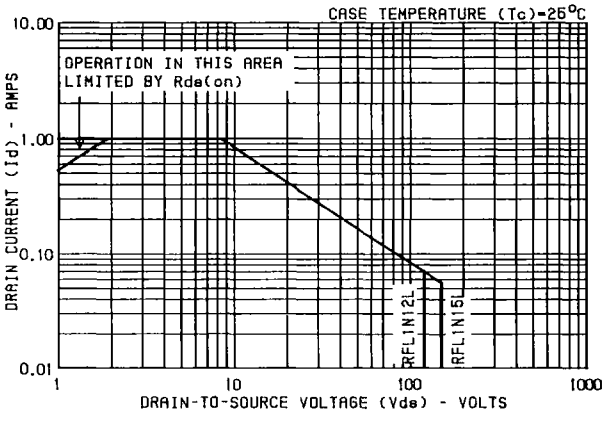



*Fig. 1 — Maximum operating areas for all types.*

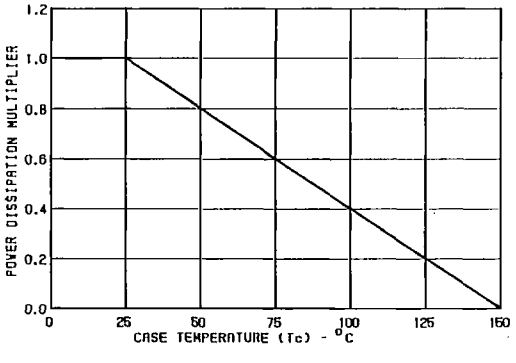



*Fig. 2 — Power dissipation vs. case temperature derating curve for all types.*

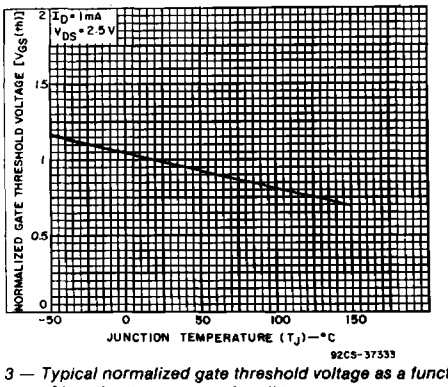



*Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.*

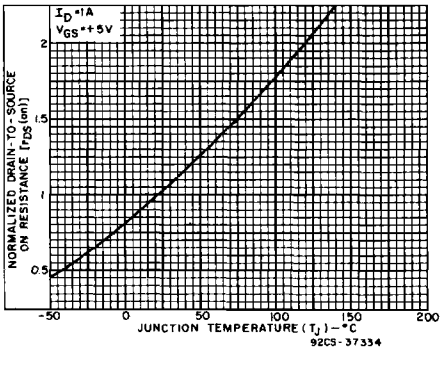



*Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.*

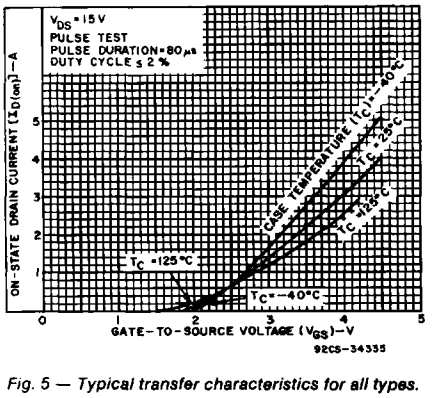



*Fig. 5 — Typical transfer characteristics for all types.*

6 LOGIC LEVEL POWER MOSFETs

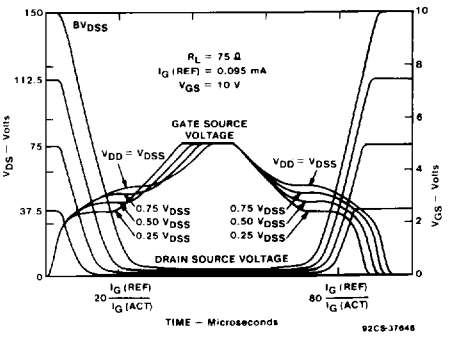



*Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.*

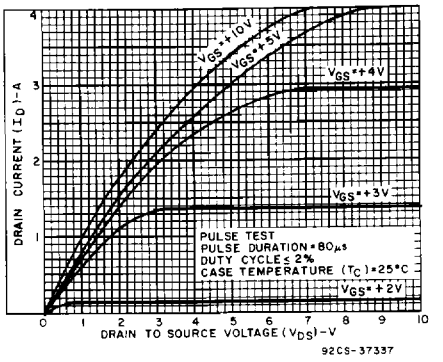



*Fig. 7 — Typical saturation characteristics for all types.*

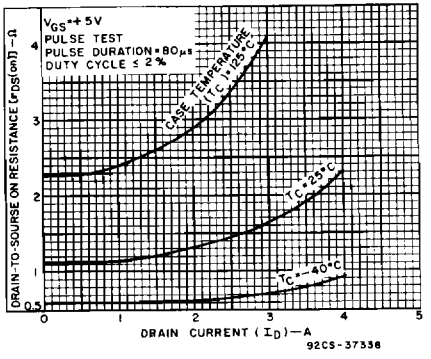



*Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.*

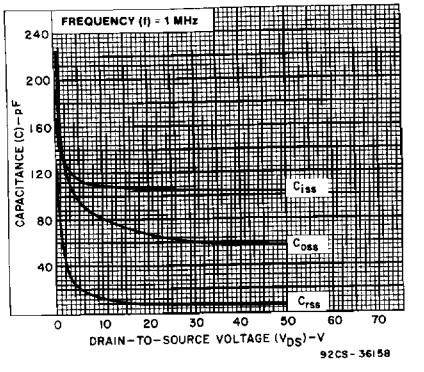



*Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.*

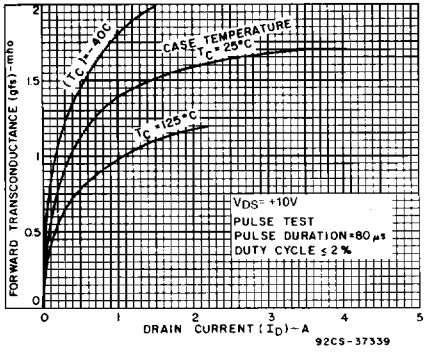



*Fig. 10 — Typical forward transconductance as a function of drain current for all types.*

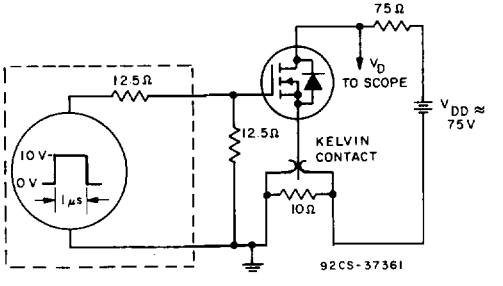



*Fig. 11 — Switching Time Test Circuit.*