PD -97693

International
IOR Rectifier

IRFB812PbF

HEXFET® Power MOSFET

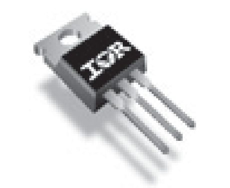
V_{DSS}	$R_{DS(on)}$ typ.	Trr typ.	I_D
500V	1.75Ω	75ns	3.6A

Applications

- Zero Voltage Switching SMPS
- Uninterruptible Power Supplies
- Motor Control applications

Features and Benefits

- Fast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Higher Gate voltage threshold offers improved noise immunity.

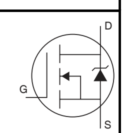


TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	3.6	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	2.3	
I_{DM}	Pulsed Drain Current ①	14.4	
P_D @T_C = 25°C	Power Dissipation	78	W
	Linear Derating Factor	0.63	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	32	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	14.4		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 3.6A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	75	110	ns	T_J = 25°C, I_F = 3.6A
		—	94	140		T_J = 125°C, di/dt = 100A/μs ④
Q_{rr}	Reverse Recovery Charge	—	135	200	nC	T_J = 25°C, I_S = 3.6A, V_{GS} = 0V ④
		—	220	330		T_J = 125°C, di/dt = 100A/μs ④
I_{RRM}	Reverse Recovery Current	—	3.2	4.8	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes ① through ⑥ are on page 2

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Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.37	——	V/°C	Reference to 25°C, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	1.75	2.2	Ω	V_{GS} = 10V, I_D = 2.2A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 500V, V_{GS} = 0V
		——	——	2.0	mA	V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	7.6	——	——	S	V_{DS} = 50V, I_D = 2.2A
Q_g	Total Gate Charge	——	——	20	nC	I_D = 3.6A
Q_{gs}	Gate-to-Source Charge	——	——	7.3		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	7.1		V_{GS} = 10V, See Fig.14a &14b ④
$t_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V_{DD} = 250V
t_r	Rise Time	——	22	——		I_D = 3.6A
$t_{d(off)}$	Turn-Off Delay Time	——	24	——		R_G = 17Ω
t_f	Fall Time	——	17	——		V_{GS} = 10V, See Fig. 15a & 15b ④
C_{iss}	Input Capacitance	——	810	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	47	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	7.3	——		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	610	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	16	——		V_{GS} = 0V, V_{DS} = 400V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	5.9	——		V_{GS} = 0V,V_{DS} = 0V to 400V ⑤
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	37	——		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	150	mJ
I_{AR}	Avalanche Current ①	——	1.8	A
E_{AR}	Repetitive Avalanche Energy ①	——	7.8	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case⑥	——	1.6	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	——	
$R_{\theta JA}$	Junction-to-Ambient⑥	——	62	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 93mH, R_G = 25Ω, I_{AS} = 1.8A. (See Figure 13).

③ I_{SD} = 3.6A, di/dt ≤ 520A/µs, $V_{DD}V_{(BR)DSS}$, T_J ≤ 150°C.

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
C_{oss} eff.(ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ R_θ is measured at T_J approximately 90°C

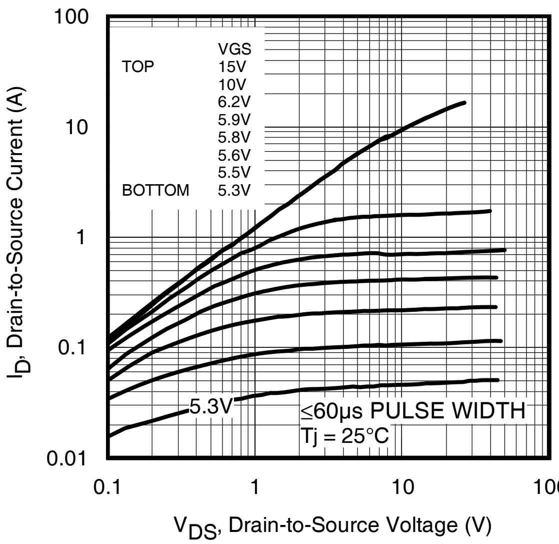


Fig 1. Typical Output Characteristics

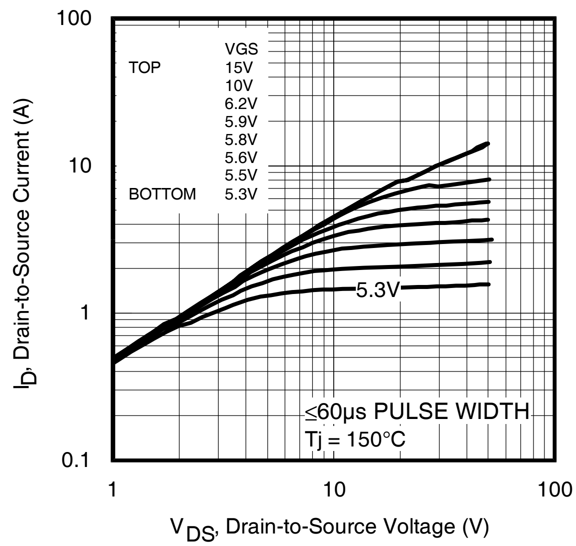


Fig 2. Typical Output Characteristics

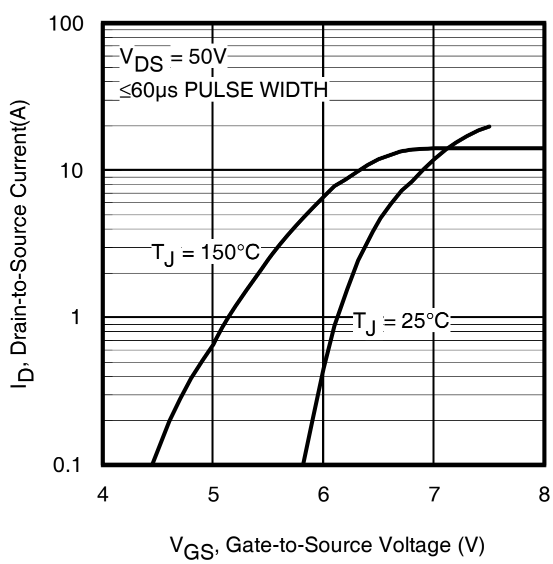


Fig 3. Typical Transfer Characteristics

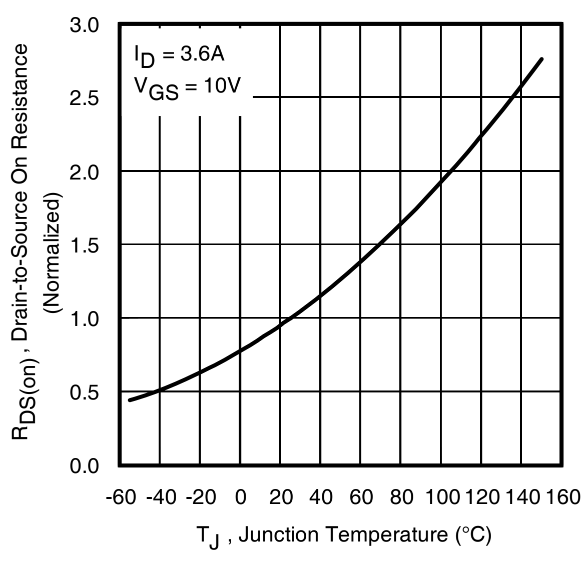


Fig 4. Normalized On-Resistance Vs. Temperature

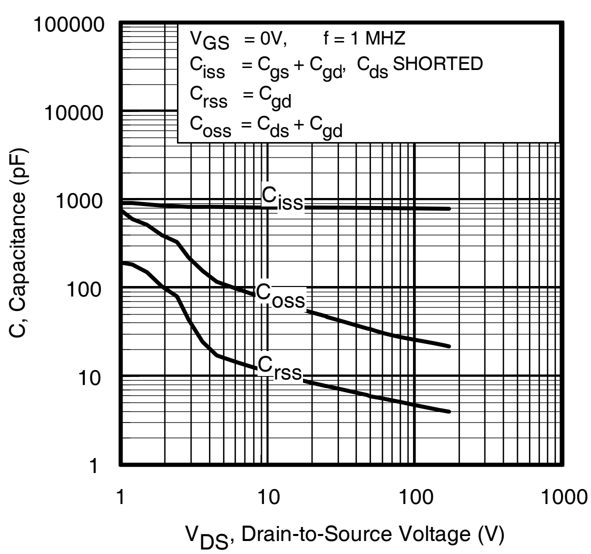


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

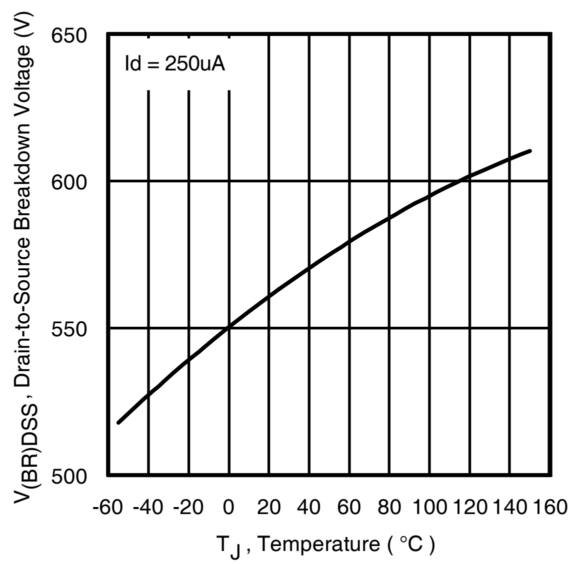
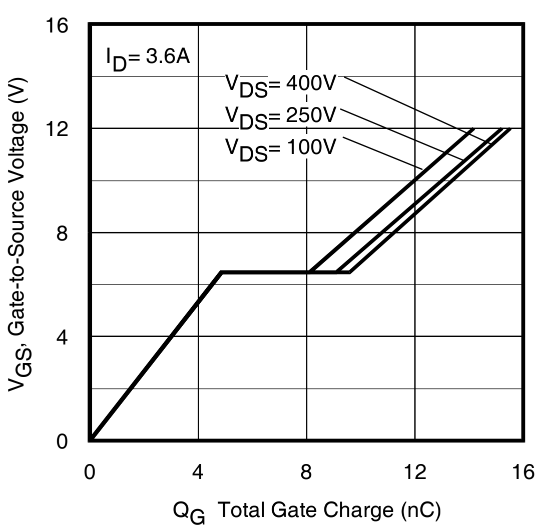
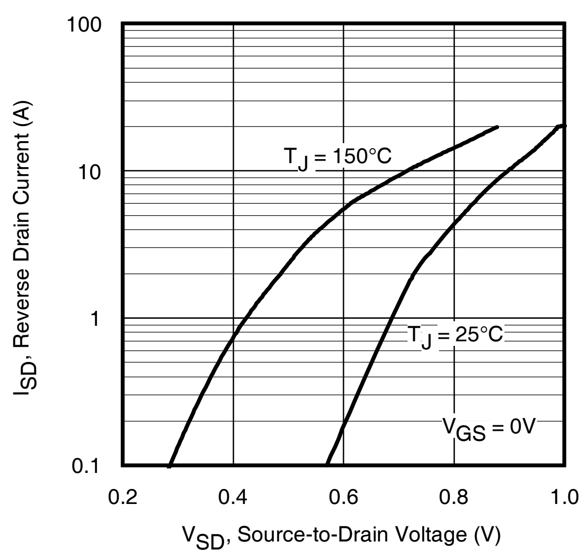


Fig 6. Typ. Breadown Voltage vs. Temperature





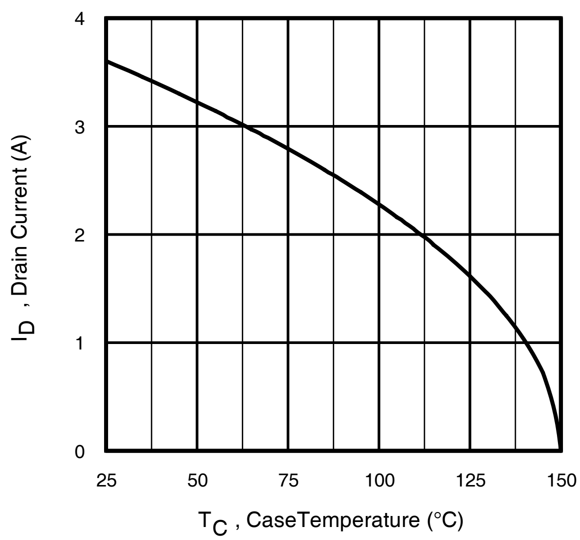


Fig 9. Maximum Drain Current Vs. Case Temperature

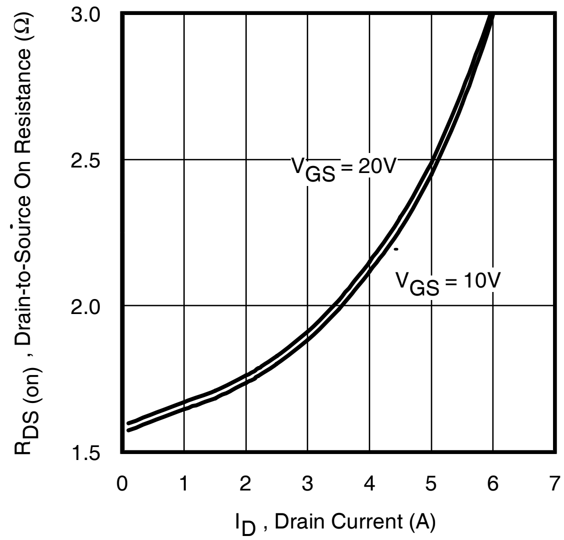


Fig 9. Typical Rdson Vs. Drain Current

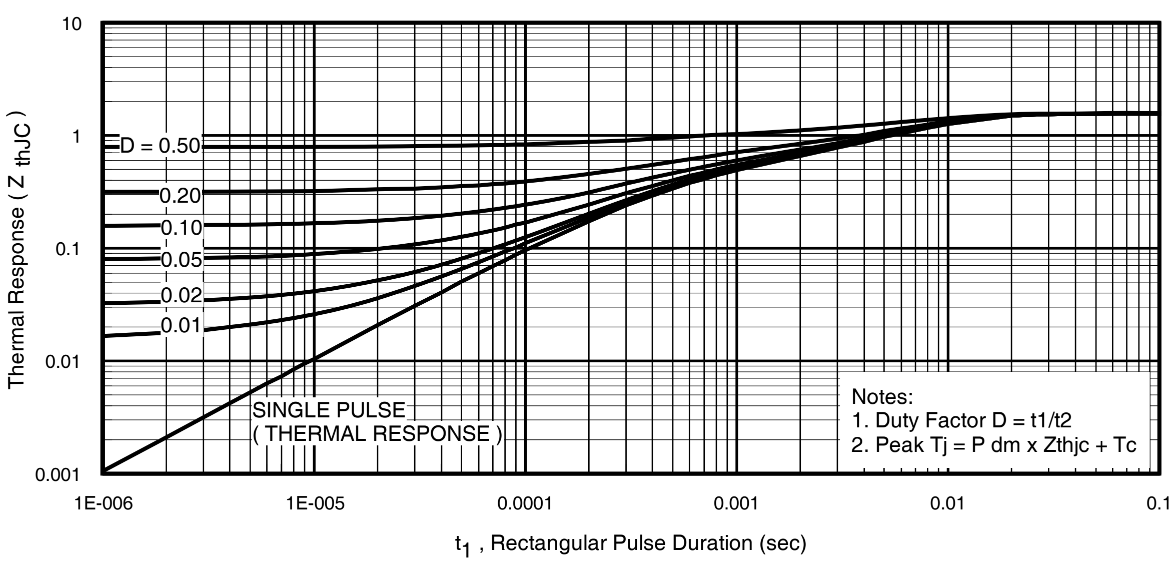


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

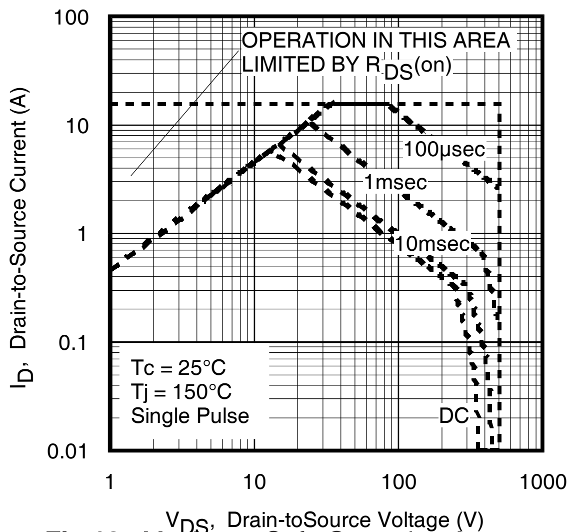


Fig 12. Maximum Safe Operating Area

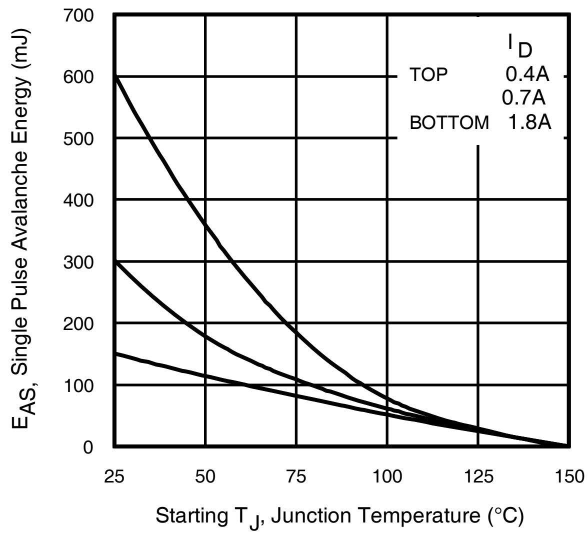


Fig 13. Maximum Avalanche Energy vs. Drain Current

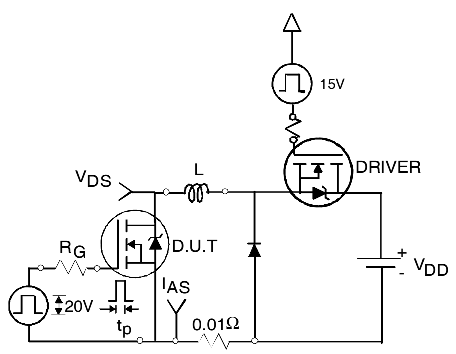


Fig 13a. Unclamped Inductive Test Circuit

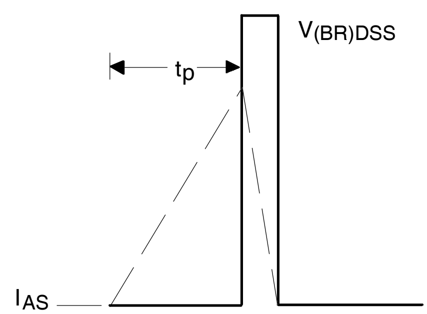


Fig 13b. Unclamped Inductive Waveforms

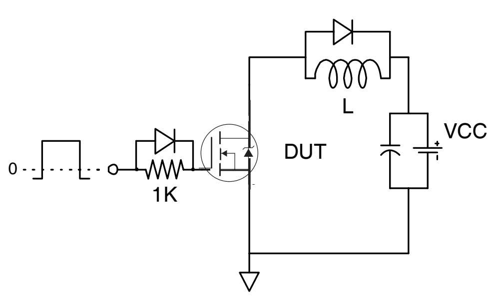


Fig 14a. Gate Charge Test Circuit

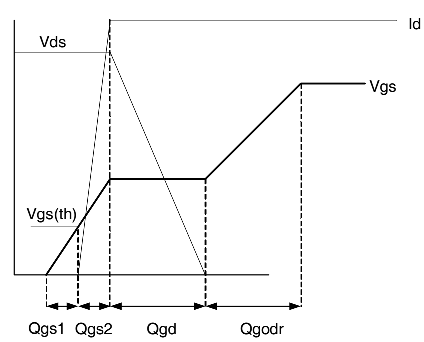


Fig 14b. Gate Charge Waveform

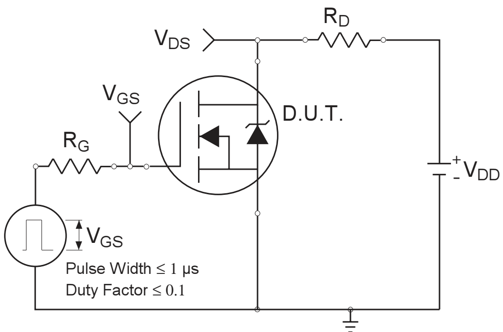


Fig 15a. Switching Time Test Circuit

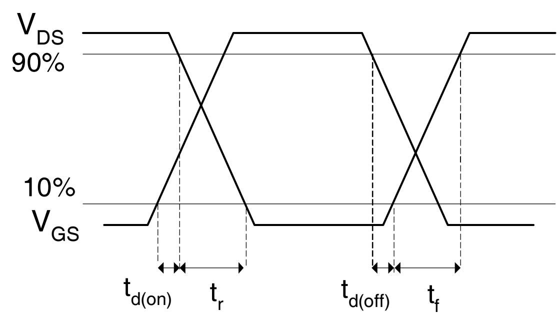
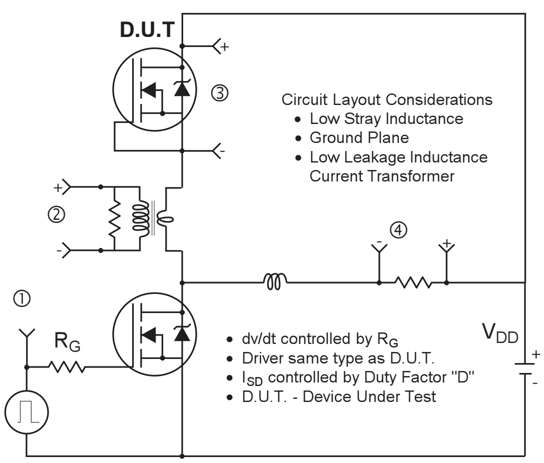
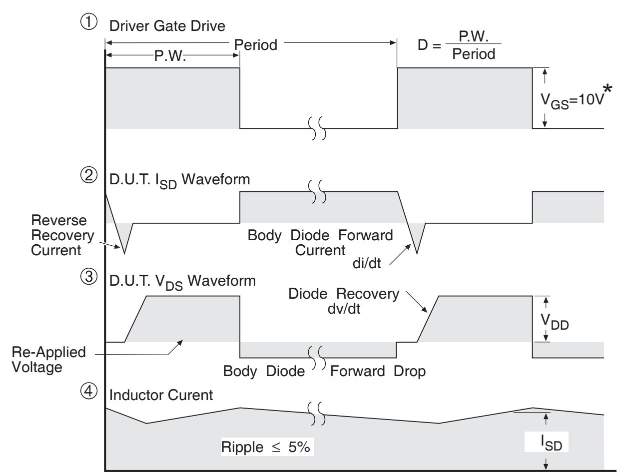


Fig 15b. Switching Time Waveforms



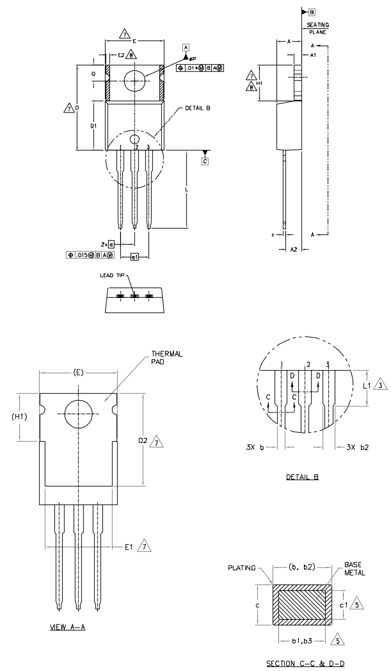


* V_{GS} = 5V for Logic Level Devices

Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.- CONTROLLING DIMENSION : INCHES.
7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

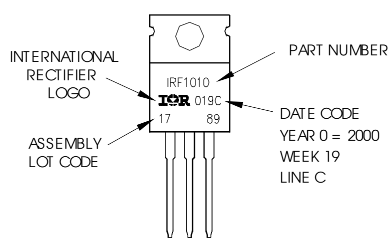
DIODES

1.- ANODE
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note:For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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