BLF7G22L-130; Power LDMOS transistor Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

Product profile

1.1 General description

130 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Typical performance Table 1.

Typical RF performance at $T_{case} = 25$ °C in a common source class-AB production test circuit.

Mode of operation	f	I _{Dq}	V _{DS}	$P_{L(AV)}$	Gp	η_{D}	ACPR
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2110 to 2170	950	28	30	18.5	32	-32 ^[1]
1-carrier W-CDMA	2110 to 2170	950	28	33	18.5	33	-39 <mark>[2]</mark>

^[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2000 MHz to 2200 MHz frequency range

^[2] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF7G22	L-130 (SOT502A)			
1	drain			
2	gate		$\begin{array}{cccccccccccccccccccccccccccccccccccc$	ئے.
3	source	<u>[1]</u>		2
				3 sym112
BLF7G22	LS-130 (SOT502B)			•
1	drain			,
2	gate		3	اً ا
3	source	<u>[1]</u>	2	2
				3 3
				sym112

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	ge	
	Name	Description	Version
BLF7G22L-130	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF7G22LS-130	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_{D}	drain current		-	28	Α
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T_{case} = 80 °C; P_{L} = 30 W	0.35	K/W

6. Characteristics

Table 6. Characteristics

 $T_i = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_{D} = 1.5 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 150 mA	1.3	1.8	2.3	V
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	5	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	25	29.5	-	Α
I _{GSS}	gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	450	nA
g _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_{D} = 7.5 \text{ A}$	-	10	11	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 5.25 \text{ A}$	-	0.1	0.16	Ω

7. Test information

Table 7. Functional test information

Mode of operation: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 950 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$P_{L(AV)}$	average output power		-	30	-	W
Gp	power gain	$P_{L(AV)} = 30 \text{ W}$	17	18.5	-	dB
RLin	input return loss	$P_{L(AV)} = 30 \text{ W}$	-	-15	-9	dB
η_{D}	drain efficiency	$P_{L(AV)} = 30 \text{ W}$	29	32	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 30 \text{ W}$	-	-31	-28	dBc

7.1 Ruggedness in class-AB operation

The BLF7G22L-130 and BLF7G22LS-130 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28 \text{ V}$; $I_{Dq} = 950 \text{ mA}$; $P_L = 130 \text{ W}$ (CW); f = 2110 MHz.

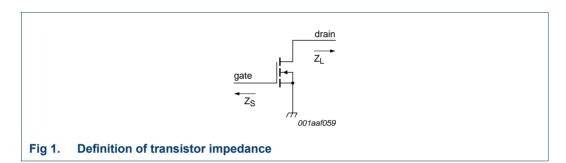
7.2 Impedance information

Table 8. Typical impedance information

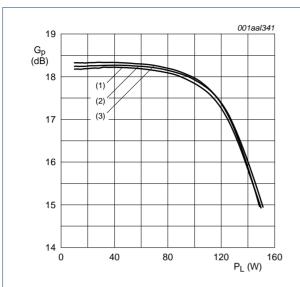
 $I_{Dq} = 950 \text{ mA}$; main transistor $V_{DS} = 28 \text{ V}$.

 Z_S and Z_L defined in Figure 1.

f (MHz)	Z _S (Ω)	Z _L (Ω)
2050	1.3 – j3.6	2.2 – j2.6
2140	1.9 – j4.2	2.0 – j2.6
2230	3.1 – j4.7	1.9 – j2.8



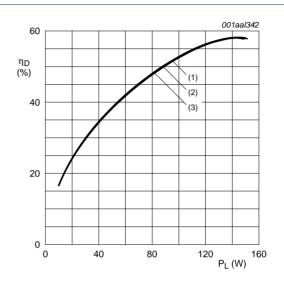
7.3 1 Tone CW



 V_{DS} = 28 V; I_{Dq} = 950 mA.

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

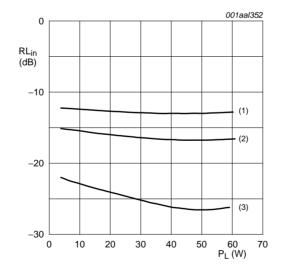
Fig 2. Power gain as a function of load power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 950 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 3. Drain efficiency as a function of load power; typical values



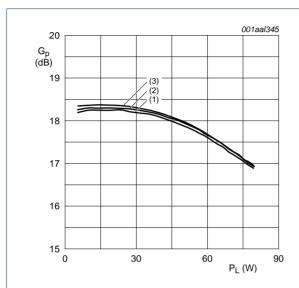
 $V_{DS} = 28 \text{ V}; I_{Dq} = 950 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 4. Input return loss as a function of load power; typical values

7.4 1-carrier W-CDMA

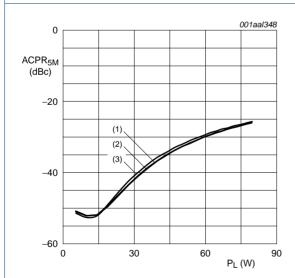
Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.



 $V_{DS} = 28 \text{ V}; I_{Dq} = 950 \text{ mA}.$

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

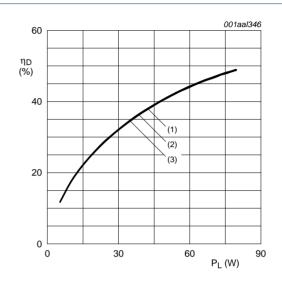
Fig 5. Power gain as a function of load power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 950 \text{ mA}.$

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

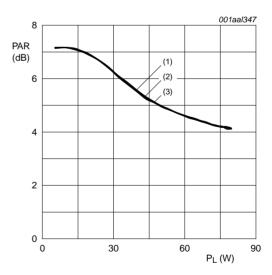
Fig 7. Adjacent channel power ratio (5MHz) as a function of load power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 950 \text{ mA}.$

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

Fig 6. Drain efficiency as a function of load power; typical values



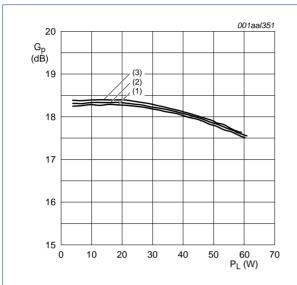
 $V_{DS} = 28 \text{ V}; I_{Dq} = 950 \text{ mA}.$

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

Fig 8. Peak-to-average power ratio as a function of load power; typical values

7.5 2-carrier W-CDMA (5 MHz carrier spacing)

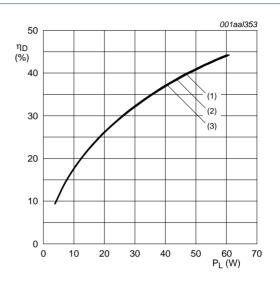
Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF.



 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 5 MHz.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

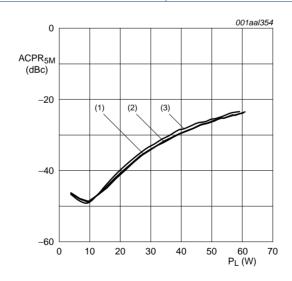
Fig 9. Power gain as a function of load power; typical values



 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 5 MHz.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

Fig 10. drain efficiency as a function of load power; typical values



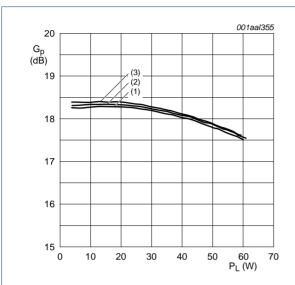
 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 5 MHz.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

Fig 11. Adjacent channel power ratio (5 MHz) as a function of load power; typical values

7.6 2-carrier W-CDMA (10 MHz carrier spacing)

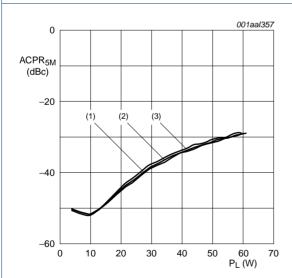
Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF.



 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 10 MHz.

- (1) f = 2117.5 MHz
- (2) f = 2140 MHz
- (3) f = 2162.5 MHz

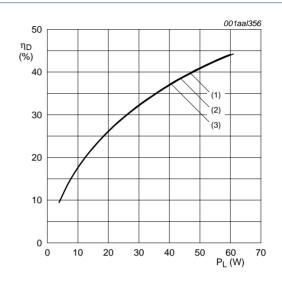
Fig 12. Power gain as a function of load power; typical values



 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 10 MHz.

- (1) f = 2117.5 MHz
- (2) f = 2140 MHz
- (3) f = 2162.5 MHz

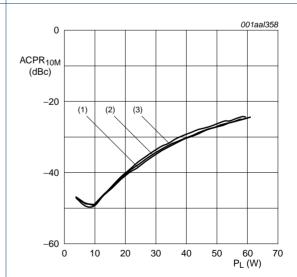
Fig 14. Adjacent channel power ratio (5 MHz) as a function of load power; typical values



 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 10 MHz.

- (1) f = 2117.5 MHz
- (2) f = 2140 MHz
- (3) f = 2162.5 MHz

Fig 13. Drain efficiency as a function of load power; typical values



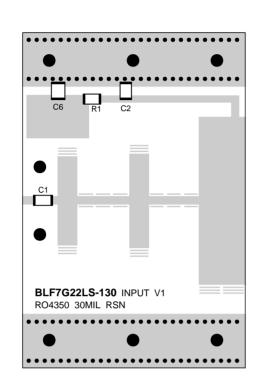
 V_{DS} = 28 V; I_{Dq} = 950 mA; carrier spacing 10 MHz.

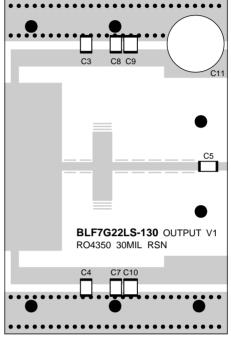
- (1) f = 2117.5 MHz
- (2) f = 2140 MHz
- (3) f = 2162.5 MHz

Fig 15. Adjacent channel power ratio (10 MHz) as a function of load power; typical values

BLF7G22L-130_7G22LS-130#5

7.7 Test circuit





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See Table 9 for list of components. The drawing is not to scale.

Fig 16. Component layout

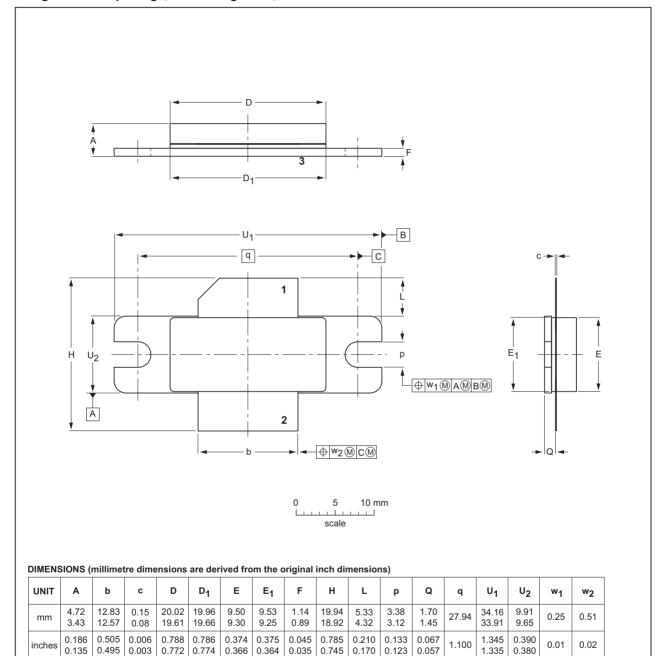
Table 9. List of components
See Figure 16 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5	multilayer ceramic chip capacitor	9.1 pF	ATC100B
C6, C7	multilayer ceramic chip capacitor	220 nF	AVX1206
C8, C9, C10	multilayer ceramic chip capacitor	4.7 μF; 50 V	Kemet
C11	electrolytic capacitor	220 μF; 63 V	ВС
R1	SMD resistor	6.2 Ω	Philips 1206

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

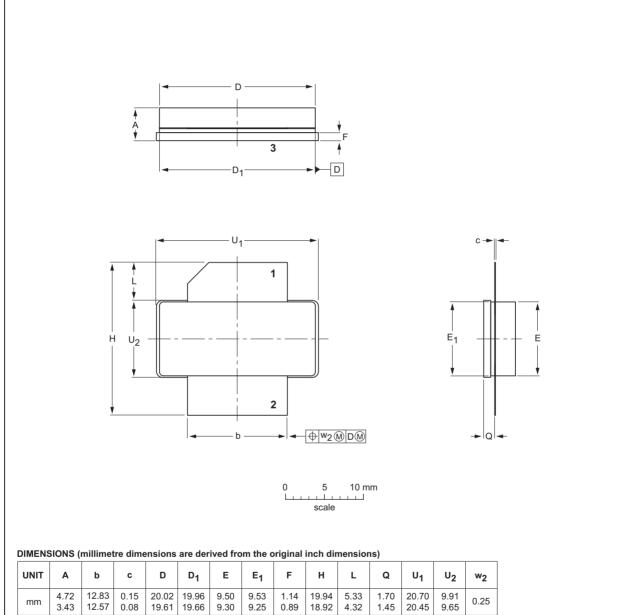


OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT502A						-03-01-10 - 12-05-02

Fig 17. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B



UNIT	Α	b	С	D	D ₁	E	E ₁	F	н	L	Q	U ₁	U ₂	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61		9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches		0.505 0.495									0.067 0.057		0.390 0.380	0.010

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	1330E DATE
SOT502B					07-05-09 12-05-02

Fig 18. Package outline SOT502B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLF7G22L-130_7G22LS-130#5	20150901	Product data sheet	-	BLF7G22L-130_7G22 LS-130 v.4	
Modifications:	The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.				
	Legal texts have been adapted to the new company name where appropriate.				
BLF7G22L-130_7G22LS-130 v.4	20110120	Product data sheet	-	BLF7G22LS-130 v.3	
BLF7G22L-130_7G22LS-130 v.3	20101118	Product data sheet	-	BLF7G22LS-130 v.2	
BLF7G22L-130_7G22LS-130 v.2	20101004	Product data sheet	-	BLF7G22LS-130 v.1	
BLF7G22LS-130 v.1	20100202	Product data sheet	-	-	

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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BLF7G22L-130; BLF7G22LS-130

Power LDMOS transistor

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BLF7G22L-130; BLF7G22LS-130

AMPLEON

Power LDMOS transistor

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