UNRF2A3

Silicon NPN epitaxial planar type

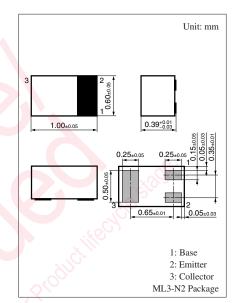
For digital circuits

Features

- Reduction of assembly cost and package size with 1006 type mold leadless package is possible
- Maximum package height (0.4 mm) contributes to develop thinner equipments

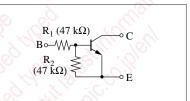
Absolute Maximum Ratings $T_a = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V _{CBO}	50	V	
Collector-emitter voltage (Base open)	V _{CEO}	50	V	
Collector current	I _C	80	mA	
Total power dissipation	P _T	100	mW	
Junction temperature	Tj	125	°C	
Storage temperature	T _{stg}	-55 to +125	°C	



Marking Symbol: 1W

Internal Connection



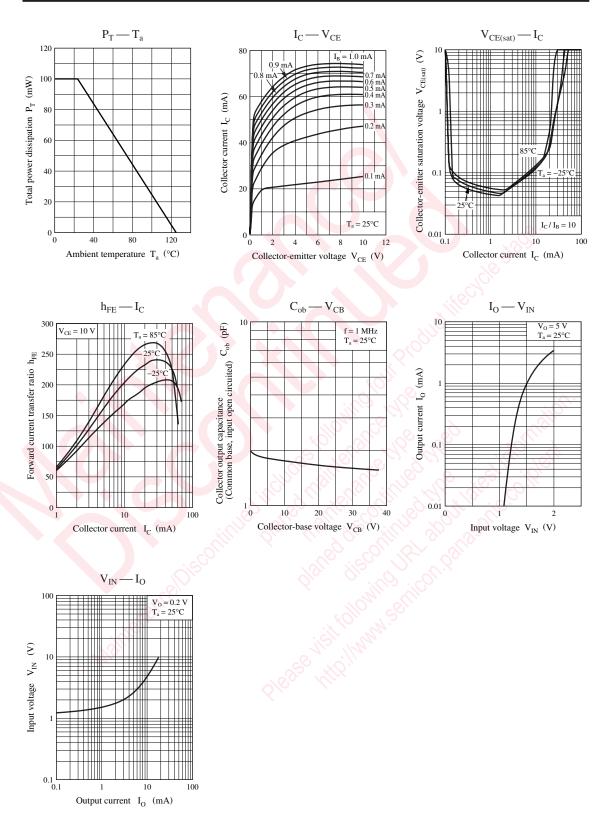
Electrical Characteristics $T_a = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V _{CBO}	$I_{\rm C} = 10 \ \mu A, I_{\rm E} = 0$	50			V
Collector-emitter voltage (Base open)	V _{CEO}	$I_{\rm C} = 2 \text{ mA}, I_{\rm B} = 0$	50			V
Collector-base cutoff current (Emitter open)	I _{CBO}	$V_{CB} = 50 \text{ V}, I_E = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	I _{CEO}	$V_{CE} = 50 \text{ V}, I_B = 0$			0.5	μΑ
Emitter-base cutoff current (Collector open)	I _{EBO}	$V_{EB} = 6 V, I_C = 0$			0.1	mA
Forward current transfer ratio	h _{FE}	$V_{CE} = 10 \text{ V}, \text{ I}_{C} = 5 \text{ mA}$	80			
Collector-emitter saturation voltage	V _{CE(sat)}	$I_{\rm C} = 10 \text{ mA}, I_{\rm B} = 0.3 \text{ mA}$			0.25	V
Output voltage high-level	V _{OH}	$V_{CC} = 5 \text{ V}, \text{ V}_{B} = 0.5 \text{ V}, \text{ R}_{L} = 1 \text{ k}\Omega$	4.9			V
Output voltage low-level	V _{OL}	$V_{CC} = 5 \text{ V}, \text{V}_{B} = 3.5 \text{V}, \text{R}_{L} = 1 \text{k}\Omega$			0.2	V
Input resistance	R ₁		-30%	47	+30%	kΩ
Resistance ratio	R ₁ / R ₂		0.8	1.0	1.2	_
Transition frequency	f _T	$V_{CB} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 200 \text{ MHz}$		150		MHz

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

UNRF2A3





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