Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Panasonic

AN41908A

Lens Driver IC for camcorder and security-camera incorporating Iris control

FEATURES

- Voltage drive system 256-step microstep drivers (2 systems)
  (Super low noise Zoom and Focus drive)
- Built-in Iris controller
- Motor control by 4-line serial data communication
- 2 systems of open-drain for driving LED
- PCB space saving.
- Low power consumption of Iris drive by PWM
- 44 pin Plastic Quad Flat Non-leaded Package (QFN Type)

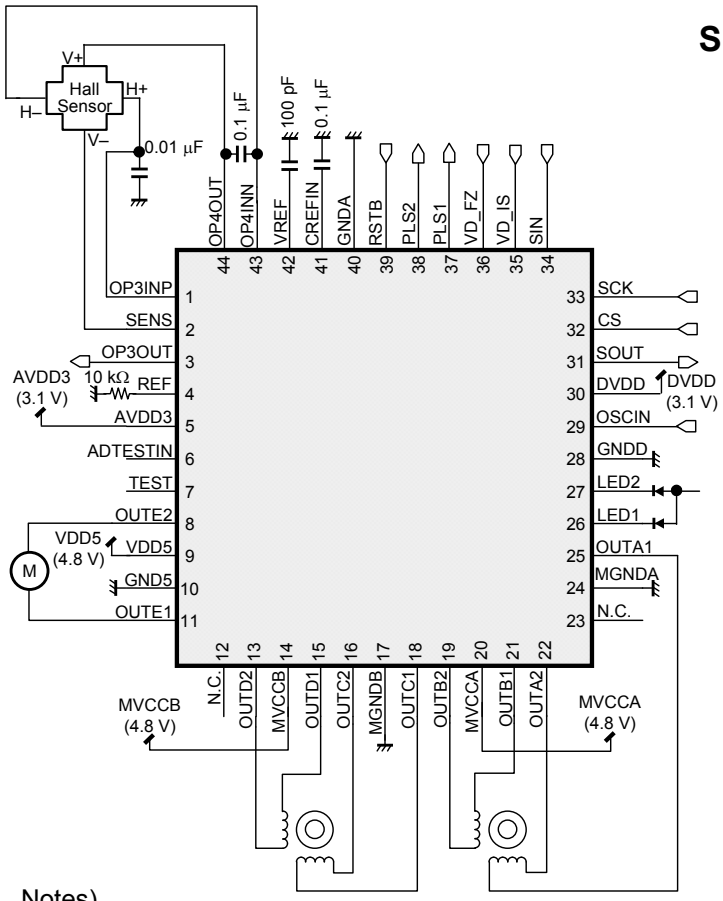
DESCRIPTION

AN41908A is a lens motor driver IC for camcorder and security-camera featuring the functions of Iris control. Voltage drive system and several torque ripple correction techniques enable super- low noise microstep drive.

APPLICATIONS

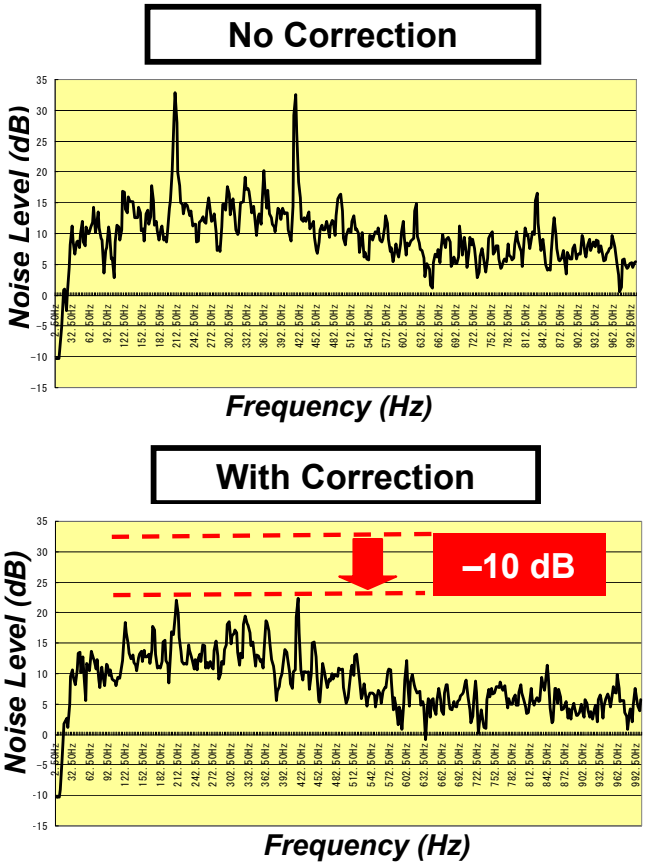
- Camcorder, Security-camera

SIMPLIFIED APPLICATION



Notes)
This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

Super low noise Zoom and Focus drive.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Controller supply voltage	AVDD3	–0.3 to + 4.0	V	*1
	DVDD	–0.3 to + 4.0		
Supply voltage for motor controller 1	MVCCA, MVCCB	–0.3 to + 6.0	V	*1
Supply voltage for motor controller 2	VDD5	–0.3 to + 6.0	V	*1
Operating ambient temperature	T_{opr}	–20 to + 85	°C	*2, *4
Operating junction temperature	T_j	–20 to + 125	°C	*2
Storage temperature	T_{stg}	–55 to + 125	°C	*2
Motor driver 1 (focus, zoom) H bridge drive current (DC current)	OUTA1, OUTA2, OUTB1, OUTB2, OUTC1, OUTC2, OUTD1, OUTD2	±0.25	A/ch	—
Motor driver 2 (iris) H bridge drive current (DC current)	OUTE1, OUTE2	±0.15	A/ch	—
Instantaneous H bridge drive current	$I_{M(pulse)}$	±0.4	A/ch	—
Input Voltage Range	OP3INP, OP4INN, ADTESTIN, REF, CREFIN	–0.3 to (AVDD3 + 0.3)	V	*3
	TEST, OSCIN, CS, SCK, SIN, VD_IS, VD_FZ, RSTB	–0.3 to (DVDD + 0.3)	V	*3
Output Voltage Range	OP3OUT, OP4OUT, SENS,VREF	–0.3 to (AVDD3 + 0.3)	V	*3
	PLS1, PLS2, SOUT	–0.3 to (DVDD + 0.3)	V	*3
Output Current Range	LED1, LED2	30	mA	—
ESD	HBM (Human Body Model)	±2	kV	—
	CDM (Charge Device Model)	±1	kV	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.

*3: (DVDD + 0.3) V must not be exceeded 4.0 V and (AVDD + 0.3) V must not be exceeded 4.0 V.

*4:The power dissipation shown is the value at Ta = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the PD-Ta diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

POWER DISSIPATION RATING

Condition	θ_{JA}	PD (Ta=25 °C)	PD (Ta=70 °C)
Mount on PWB *1	71.8°C/W	1.392W	0.765W
Without PWB	282.9°C/W	0.353W	0.194W

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy: 50×50×0.8 (mm) , heat dissipation fin: Dai-pad , the state where it does not mount.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	AVDD3,DVDD	2.7	3.1	3.6	V	*1
	MVCCA, MVCCB, VDD5	3.0	4.8	5.5	V	*1
Input Voltage Range	OP3INP, OP4INN, ADTESTIN, REF, CREFIN	–0.3	—	AVDD3 + 0.3	V	*2
	TEST, OSCIN, CS, SCK, SIN, VD_IS, VD_FZ, RSTB	–0.3	—	DVDD + 0.3	V	*2
Output Voltage Range	OP3OUT, OP4OUT, SENS,VREF	–0.3	—	AVDD3 + 0.3	V	*2
	PLS1, PLS2, SOUT	–0.3	—	DVDD + 0.3	V	*2
Output Current Range	OUTA1, OUTA2, OUTB1, OUTB2, OUTC1, OUTC2, OUTD1, OUTD2	−0.25	—	0.25	A	*1
	OUTE1, OUTE2	−0.15	—	0.15	A	*1
	LED1, LED2	—	—	30	mA	*1
External Constants	C_{VREF}		100		pF	—
	C_{REFIN}		0.1		µF	—
	R_{REF}		10		kΩ	—
	C_{OP3INP}		0.01		µF	—
	C_{OP4OUT}		0.1		µF	—
Operating ambient temperature	Ta^{opr}	-20		85	°C	—

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : (DVDD + 0.3) V must not be exceeded 4.0 V and (AVDD + 0.3) V must not be exceeded 4.0 V.

ELECRTRICAL CHARACTERISTICS

VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V T_a = 25°C±2°C

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current circuit, Common circuit							
MVCC supply current on Reset	$I_{Omdisable}$	No load, no 27 MHz input	—	0	3.0	μA	
MVCC supply current on Enable	$I_{menable}$	Output open	—	0.5	15	mA	
3 V supply current on Reset	$Icc3_{reset}$	No 27 MHz input	—	0	10.0	μA	
3 V supply current on Enable	$Icc3_{enable}$	Output open	—	7.0	20.0	mA	
VDD5 supply current on Reset	$Icc5_{reset}$	No 27 MHz input	—	0	3.0	μA	
VDD5 supply current on Enable	$Icc5_{enable}$	Output open	—	0.3	1.0	mA	
Supply current on Standby	$Icc_{standby}$	RSTB = High, output open, 27 MHz input, Total current	—	5.0	10.0	mA	
Supply current when FZ is Enable and Iris is in power save mode	Icc_{ps}	RSTB = High, output open, 27 MHz input, FZ = Enable, Total current	—	6.0	12.0	mA	
Digital input / output							
High-level input	$V_{in(H)}$	RSTB	0.54 × DVDD	—	DVDD + 0.3	V	
Low-level input	$V_{in(L)}$	RSTB	–0.3	—	0.2 × DVDD	V	
SOUT High-level output	$V_{out(H)}$: SDATA	[SOUT] 1 mA Source	DVDD – 0.5	—	—	V	
SOUT Low-level output	$V_{out(L)}$: SDATA	[SOUT] 1 mA Sink	—	—	0.5	V	
PLS1 to 2 High-level output	$V_{out(H)}$: MUX	—	0.9 × DVDD	—	—	V	
PLS1 to 2 Low-level output	$V_{out(L)}$: MUX	—	—	—	0.1 × DVDD	V	
Input pull-down resistance	$R_{pullret}$	RSTB	50	100	200	kΩ	
Motor driver 1 (focus, zoom)							
H bridge ON resistance	R_{onFZ}	IM = 100 mA	—	—	2.5	Ω	
H bridge leak current	I_{leakFZ}	—	—	—	0.8	μA	
Motor driver 2 (iris)							
H bridge ON resistance	R_{onIR}	IM = 50 mA	—	—	5	Ω	
H bridge leak current	I_{leakIR}	—	—	—	0.8	μA	
LED driver							
Output ON resistance	R_{onLED}	I = 20 mA, 5 V cell	—	—	8	Ω	
Output leak current	$I_{leakLED}$	—	—	—	0.8	μA	

ELECRTRICAL CHARACTERISTICS (continued)

VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V T_a = 25°C±2°C

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
OPAMP3 (HALL Sensor Amp. for output amplifier)							
Input voltage range	V_{IN}	—	½ AVDD3 – 0.5	½ AVDD3	½ AVDD3 + 0.5	V	
Input offset voltage	V_{OF}	—	–15	—	15	mV	
Output voltage (Low)	V_{OL}	ILOAD = –100 μA	—	0.1	0.2	V	
Output voltage (High)	V_{OH}	ILOAD = 100 μA	AVDD3 – 0.2	AVDD3 – 0.1	—	V	
Gain	V_{OG}	Gain setting value : 0h	19.7	21.9	24.1	V/V	
OPAMP4 (HALL Sensor Amp. for eliminating common-mode voltage)							
Input voltage range	V_{IN}	—	½ AVDD3 – 0.1	—	½ AVDD3 + 0.1	V	
Input offset voltage	V_{OF}	—	–10	—	10	mV	
Output voltage (Low)	V_{OL}	ILOAD = –10 μA	—	0.1	0.2	V	
Output voltage (High)	V_{OH}	ILOAD = 3 mA	AVDD3 – 0.5	AVDD3 – 0.2	—	V	
Reference voltage output block							
Output voltage 1	VREF	ILOAD = 0 A, CVREF = 100 pF	½ AVDD3 – 0.1	½ AVDD3	½ AVDD3 + 0.1	V	
Output voltage 2	VREFL	ILOAD = ±100 μA, CVREF = 100 pF	VREF – 0.1	VREF	VREF + 0.1	V	
Hall bias controller (SENS pin output)							
Min. output current	IBL	REF = 10 kΩ, SENS = 0.7 V Setting value : 00 h	—	0	0.1	mA	
Output current accuracy 1	IB40H	REF = 10 kΩ, SENS = 0.7 V Setting value : 40 h	0.9	1.02	1.14	mA	
Output current accuracy 2	IBBFH	REF = 10 kΩ, SENS = 0.7 V Setting value : BE h	2.66	3.02	3.38	mA	

ELECRTRICAL CHARACTERISTICS (continued)

VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V T_a = 25°C±2°C

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Serial port input							
Serial clock	Sclock	—	1	—	5	MHz	*1
SCK low time	T1	—	100	—	—	ns	*1
SCK high time	T2	—	100	—	—	ns	*1
CS setup time	T3	—	60	—	—	ns	*1
CS hold time	T4	—	60	—	—	ns	*1
CS disable high time	T5	—	100	—	—	ns	*1
SIN setup time	T6	—	50	—	—	ns	*1
SIN hold time	T7	—	50	—	—	ns	*1
SOUT delay time	T8	—	—	—	60	ns	*1
SOUT hold time	T9	—	60	—	—	ns	*1
SOUT Enable-Hi-Z time	T10	—	—	—	60	ns	*1
SOUT Hi-Z-Enable time	T11	—	—	—	60	ns	*1
SOUT C load	T_{SC}	—	—	—	40	pF	*1
Digital input / output							
High-level input threshold voltage	$V_{in(H)}$	SCK, SIN, CS, OSCIN, VD_IS, VD_FZ, TEST	—	1.36	—	V	*1
Low-level input threshold voltage	$V_{in(L)}$	SCK, SIN, CS, OSCIN, VD_IS, VD_FZ, TEST	—	1.02	—	V	*1
RSTB signal pulse width	Trst	—	100	—	—	µs	*1
Input hysteresis width	V_{hysin}	SCK, SIN, CS, OSCIN, VD_IS, VD_FZ, TEST	—	0.34	—	V	*1
Video sync. signal width	VD_W	—	80	—	—	µs	*1
CS signal wait time 1	$T_{(VD-CS)}$	—	400	—	—	ns	*1
CS signal wait time 2	$T_{(CS-DT1)}$	—	5	—	—	µs	*1

Note) *1 : Typical Value checked by design.

ELECRTRICAL CHARACTERISTICS (continued)

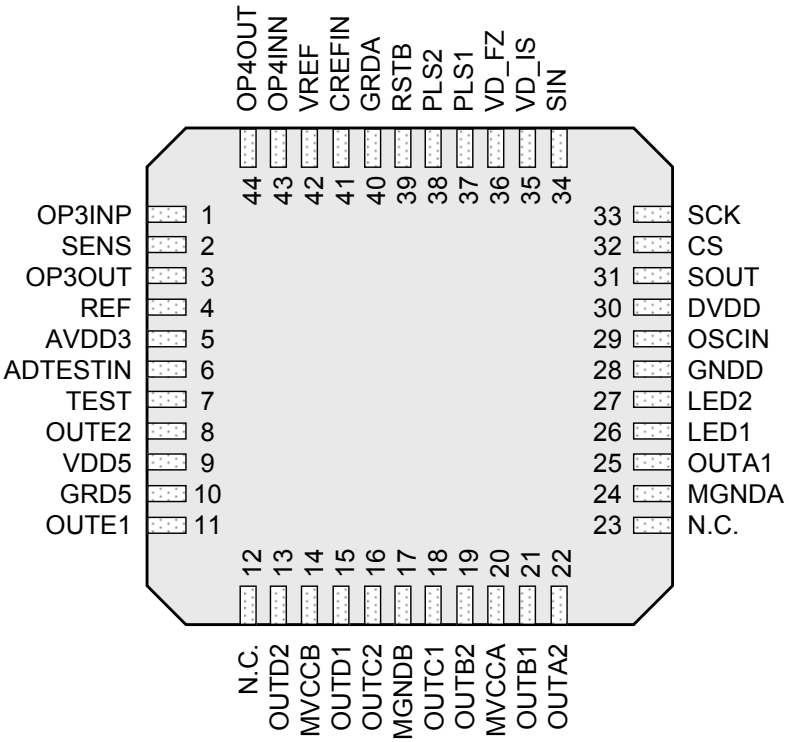
VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V T_a = 25°C±2°C

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Pulse generator							
Pulse start resolution for pulse 1	PL1wait	OSCIN = 27 MHz	—	20.1	—	µs	*1
Pulse resolution for pulse 1	PL1width	OSCIN = 27 MHz	—	1.2	—	µs	*1
Pulse start resolution for pulse 2	PL2wait	OSCIN = 27 MHz	—	20.1	—	µs	*1
Iris control							
AD sampling frequency	$IRIS_{Sample}$	OSCIN = 27 MHz	—	500	—	kHz	*1
Iris control							
Thermal shutdown operation temperature	Ttsd	—	—	150	—	°C	*1
Thermal shutdown hysteresis width	Δ Ttsd	—	—	40	—	°C	*1
Supply voltage monitor circuit							
3.3 V Reset operation	Vrston	—	—	2.27	—	V	*1
3.3 V Reset hysteresis width	Vrsthys	—	—	0.2	—	V	*1
MVCCx Reset operation	$V_{rstFZon}$	—	—	2.2	—	V	*1
MVCCx Reset hysteresis width	$V_{rstFZhys}$	—	—	0.2	—	V	*1
VDD5 Reset operation	$V_{rstlSon}$	—	—	2.2	—	V	*1
VDD5 Reset hysteresis width	$V_{rstlShys}$	—	—	0.2	—	V	*1
8 bit DAC for Hall Offset adjustment							
Adjustment range (High)	DAOTHof	—	—	AVDD 3	—	V	*1
Adjustment range (Low)	DAOTLof	—	—	0	—	V	*1
10 bit ADC							
Input Range (High)	$V_{in(H)}$	—	—	—	AVDD 3 – 0.2	V	*1
Input Range (Low)	$V_{in(L)}$	—	0.2	—	—	V	*1
DNLE (Differential linearity error)	DNL10A	—	—	1.0	—	LSB	*1
INLE (Integral linearity error)	INL10A	—	—	2.0	—	LSB	*1

Note) *1 : Typical Value checked by design.

PIN CONFIGURATION

Top View



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	OP3INP	Input	Hall signal amplifier non-inverting input
2	SENS	Output	Hall current bias output
3	OP3OUT	Output	Hall signal amplifier output
4	REF	—	Resistor connection for Hall current bias setting
5	AVDD3	Power supply	3 V analog power supply
6	ADTESTIN	Input	ADC test input
7	TEST	Input	Test mode input
8	OUTE2	Output	Motor output E2
9	VDD5	Power supply	Power supply for Iris
10	GND5	Ground	GND for Iris
11	OUTE1	Output	Motor output E1
12, 23	N. C.	—	N. C.
13	OUTD2	Output	Motor output D2
14	MVCCB	Power supply	Power supply for motor B
15	OUTD1	Output	Motor output D1
16	OUTC2	Output	Motor output C2
17	MGNDB	Ground	GND for motor B
18	OUTC1	Output	Motor output C1
19	OUTB2	Output	Motor output B2
20	MVCCA	Power supply	Power supply for motor A
21	OUTB1	Output	Motor output B1
22	OUTA2	Output	Motor output A2
24	MGNDA	Ground	GND for motor A
25	OUTA1	Output	Motor output A1
26	LED1	Input	Open-drain 1 for driving LED
27	LED2	Input	Open-drain 2 for driving LED
28	GNDD	Ground	Digital GND
29	OSCIN	Input	OSCIN input
30	DVDD	Power supply	3 V digital power supply
31	SOUT	Output	Serial data output
32	CS	Input	Chip select signal input
33	SCK	Input	Serial clock input

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

PIN FUNCTIONS (Continued)

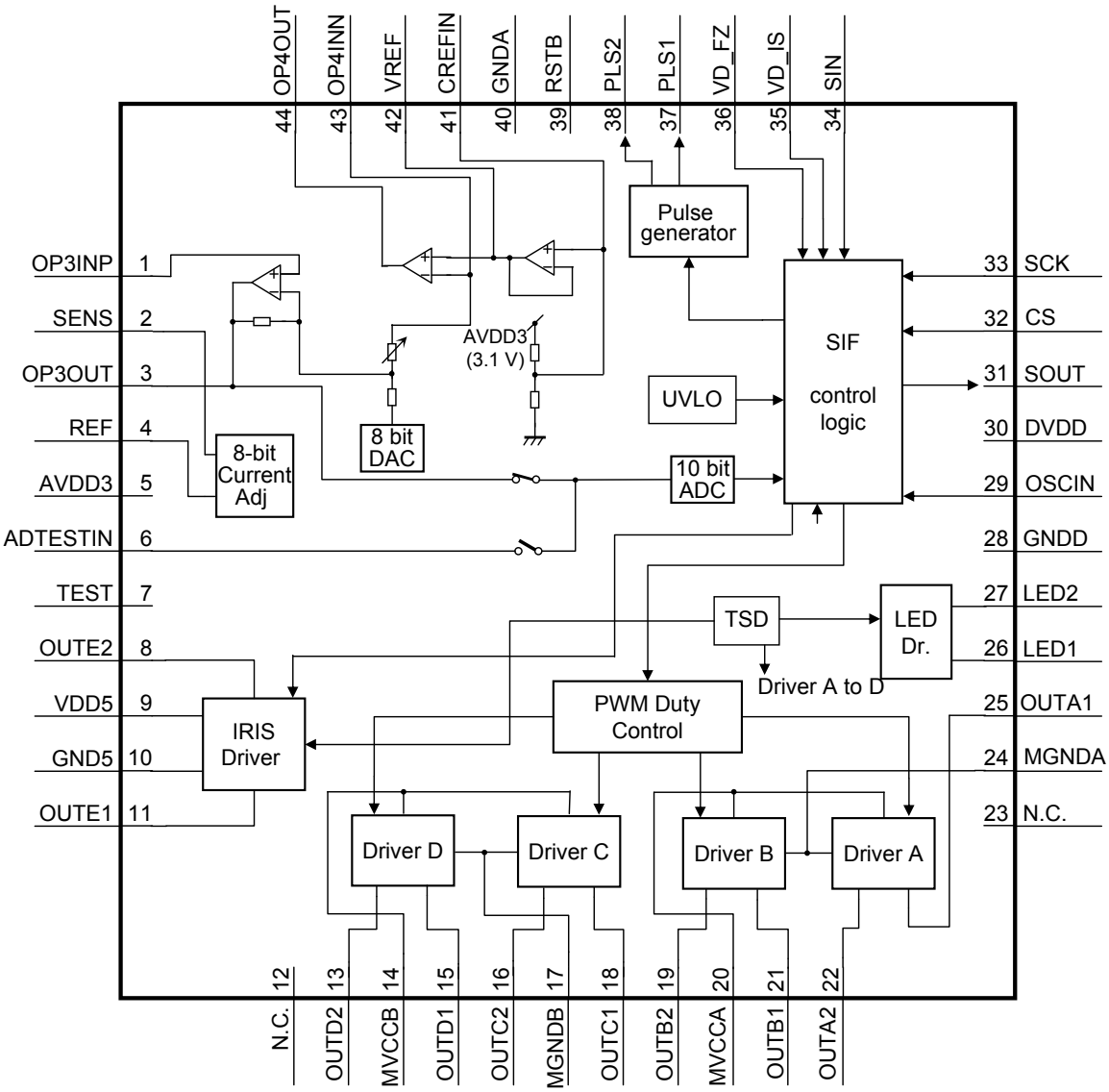
Pin No.	Pin name	Type	Description
34	SIN	Input	Serial data input
35	VD_IS	Input	Iris video sync. signal input
36	VD_FZ	Input	Focus zoom sync. signal input
37	PLS1	Output	Pulse 1 output
38	PLS2	Output	Pulse 2 output
39	RSTB	Input	Reset signal input
40	GNDA	Ground	3 V analog GND
41	CREFIN	—	(AVDD3)/2 capacitor connection pin
42	VREF	Output	Reference voltage for Hall sensor
43	OP4INN	Input	Midpoint bias amplifier inverting input
44	OP4OUT	Output	Midpoint bias amplifier output

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

Panasonic

AN41908A

FUNCTIONAL BLOCK DIAGRAM



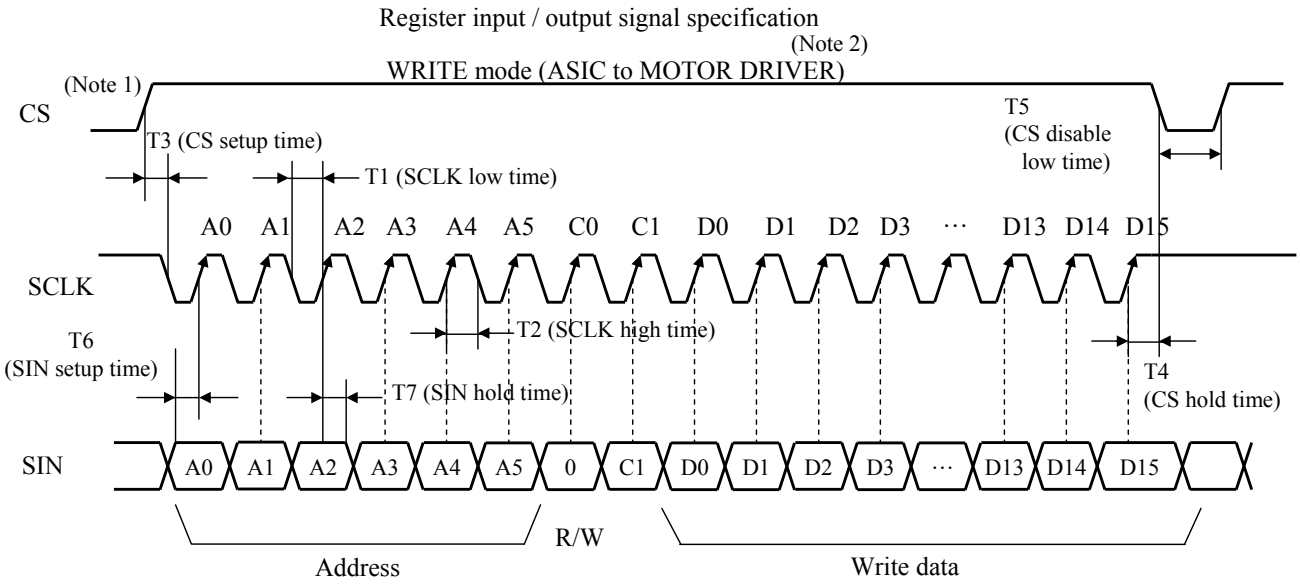
Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

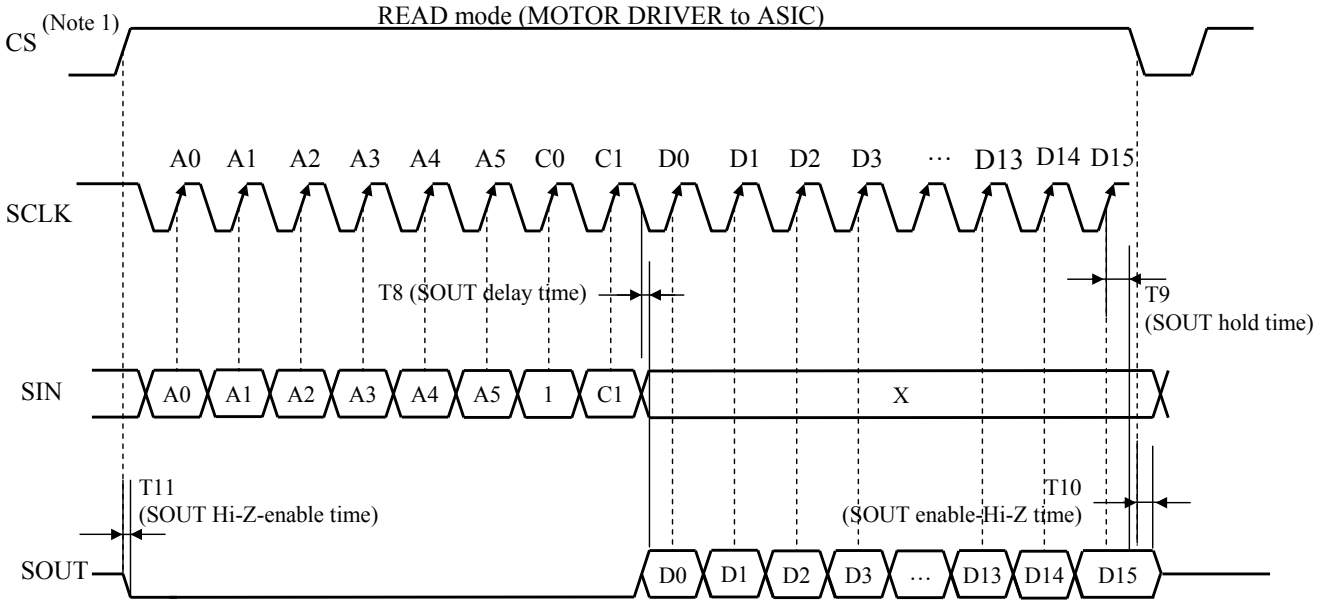
APPLICATIONS INFORMATION

1. Serial Interface

■ Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.





Note 1) CS default value of each cycle (Write / Read mode) starts from Low-level.
Note 2) It is necessary to input the system clock OSCIN at write mode.

APPLICATIONS INFORMATION (Continued)

■ Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H							IRS_TGT[9:0]									
01H	DGAIN[6:0]							ASOUND_LPF_FC[2:0]			AS_FLT_OFF	DEC_AVE	OVER_LPF_FC_2ND[1:0]		OVER_LPF_FC_1ST[1:0]	
02H	PID_POLE[3:0]				PID_ZERO[3:0]				IRIS_ROUND[3:0]				IRIS_CALC_NR[3:0]			
03H			DT_ADJ_IRIS[1:0]		PWM_IRIS[2:0]			PWM_LPF_FC[2:0]			PWM_FLT_OFF	LMT_ENB	ARW[3:0]			
04H	HALL_OFFSET_DAC[7:0]								HALL_BIAS_DAC[7:0]							
05H				AAF_FC	HALL_GAIN[3:0]						PID_INV	TGT_FLT_OFF	TGT_LPF_FC[3:0]			
06H							START1[9:0]									
07H	P1EN				WIDTH1[11:0]											
08H							START2[9:0]									
09H	P2EN										WIDTH2[5:0]					
0AH						DUTY_TEST	TGT_IN_TEST[9:0]									
0BH	PID_CLIP[3:0]				ADC_TEST	PDWNB	MODESEL_FZ	MODESEL_IRIS	TESTEN1			ASWMODE[1:0]				
0CH							IRSAD[9:0] (Read Only)									
0DH																
0EH				AVE_SPEED[4:0]					TGT_UPDATE[7:0]							
0FH						Reserved	Reserved									
10H																
20H		PWMRES[1:0]		PWMMODE[4:0]					DT1[7:0]							
21H									TESTEN2			FZTEST[4:0]				
22H			PHMODAB[5:0]						DT2A[7:0]							
23H	PPWB[7:0]								PPWA[7:0]							
24H			MICROAB[1:0]		LEDB	ENDISAB	BRAKEAB	CCWCWAB	PSUMAB[7:0]							
25H	INTCTAB[15:0]															
26H																
27H			PHMODCD[5:0]						DT2B[7:0]							
28H	PPWD[7:0]								PPWC[7:0]							
29H			MICROCD[1:0]		LEDA	ENDISCD	BRAKECD	CCWCWCD	PSUMCD[7:0]							
2AH	INTCTCD[15:0]															
2BH																
2CH														Reserved	Reserved	Reserved

APPLICATIONS INFORMATION (Continued)

■ Register List

Address	Register name / Bit wide	Function
00h	IRS_TGT[9:0]	Iris target
01h	OVER_LPF_FC_1ST[1:0]	ADC feedback filter (1) cut-off frequency
	OVER_LPF_FC_2ND[1:0]	ADC feedback filter (2) cut-off frequency
	DEC_AVE	Moving average of Iris target
	AS_FLT_OFF	Filter before PID controller enable / disable
	ASOUND_LPF_FC[2:0]	Filter cut-off frequency before PID controller
	DGAIN[6:0]	PID controller digital gain
02h	IRIS_CALC_NR[3:0]	PID controller integral error cumulative prevention level
	IRIS_ROUND[3:0]	PID controller differential error cumulative prevention level
	PID_ZERO[3:0]	PID controller zero point
	PID_POLE[3:0]	PID controller pole
03h	ARW[3:0]	Number of bits in PID controller integrator
	LMT_ENB	PID controller integral stop
	PWM_FLT_OFF	LPF after PID controller enable / disable
	PWM_LPF_FC[2:0]	LPF cut-off frequency after PID controller
	PWM_IRIS[2:0]	PWM frequency of Iris block output
	DT_ADJ_IRIS[1:0]	Dead time correction of Iris block output
04h	HALL_BIAS_DAC[7:0]	Drive current value for hall element
	HALL_OFFSET_DAC[7:0]	Offset adjustment for hall element output amplifier
05h	TGT_LPF_FC[3:0]	Iris target value LPF cut-off frequency
	TGT_FLT_OFF	Iris target value LPF function enable / disable
	PID_INV	PID controller polarity
	HALL_GAIN[3:0]	Hall element output amplifier gain
	AAF_FC	Cut-off frequency of hall element output amplifier
06h	START1[9:0]	Pulse 1 start time
07h	WIDTH1[11:0]	Pulse 1 width
	P1EN	Pulse 1 output enable
08h	START2[9:0]	Pulse 2 start time
09h	WIDTH2[5:0]	Pulse 2 width
	P2EN	Pulse 2 output enable

APPLICATIONS INFORMATION (Continued)

■ Register List (continued)

Address	Register name / Bit wide	Function
0Ah	TGT_IN_TEST[9:0]	Iris output duty direct specified value
	DUTY_TEST	Iris output duty direct specification enable
0Bh	ASWMODE[1:0]	ADTESTIN pin connection selection
	TESTEN1	Test mode enable 1
	MODESEL_IRIS	VD_IS polarity selection
	MODESEL_FZ	VD_FZ polarity selection
	PDWNB	Power down of Iris block
	ADC_TEST	ADC read value updated timing
	PID_CLIP[3:0]	Iris output PWM maximum duty
0Ch	IRSAD[9:0]	ADC output for Iris (read only)
0Eh	TGT_UPDATE[7:0]	IRS_TGT (iris target) update delay time
	AVE_SPEED[4:0]	Iris target moving average speed

APPLICATIONS INFORMATION (Continued)

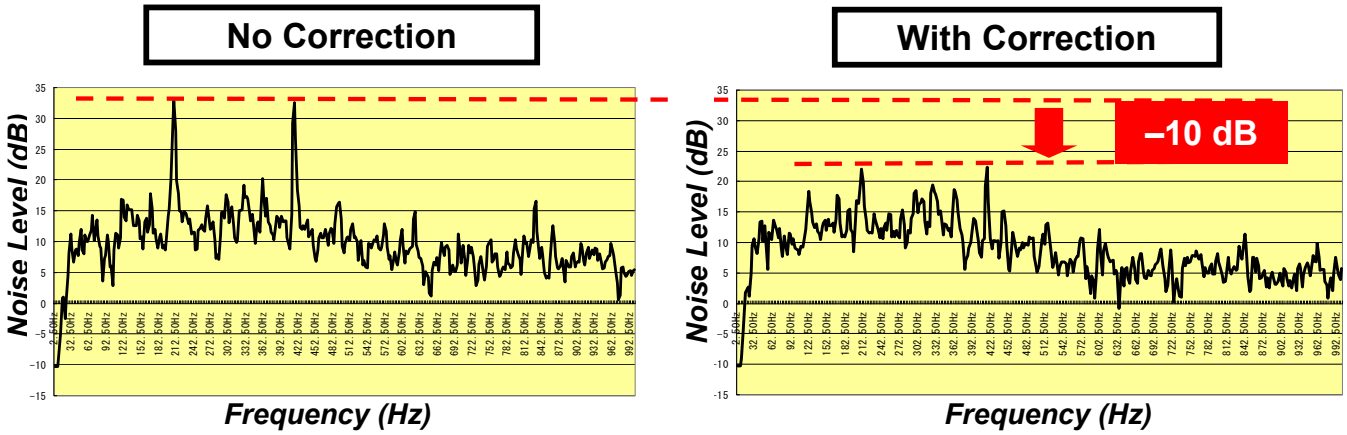
■ Register List (continued)

Address	Register name / Bit wide	Function
20h	DT1[7:0]	Start point wait time
	PWMMODE[4:0]	Micro step output PWM frequency
	PWMRES[1:0]	Micro step output PWM resolution
21h	FZTEST[4:0]	PLS1/2 pin output signal selection
	TESTEN2	Test mode enable 2
22h	DT2A[7:0]	α motor start point excitation wait time
	PHMODAB[5:0]	α motor phase correction
23h	PPWA[7:0]	Driver A peak pulse width
	PPWB[7:0]	Driver B peak pulse width
24h	PSUMAB[7:0]	α motor step count number
	CCWCWAB	α motor rotation direction
	BRAKEAB	α motor brake
	ENDISAB	α motor enable/disable control
	LEDB	LED B output control
	MICROAB[1:0]	α motor sine wave division number
25h	INTCTAB[15:0]	α motor step cycle
27h	DT2B[7:0]	β motor start point excitation wait time
	PHMODCD[5:0]	β motor phase correction
28h	PPWC[7:0]	Driver C peak pulse width
	PPWD[7:0]	Driver D peak pulse width
29h	PSUMCD[7:0]	β motor step count number
	CCWCWCD	β motor rotation direction
	BRAKECD	β motor brake
	ENDISCD	β motor enable/disable control
	LEDA	LED A output control
	MICROCD[1:0]	β motor sine wave division number
2Ah	INTCTCD[15:0]	β motor step cycle

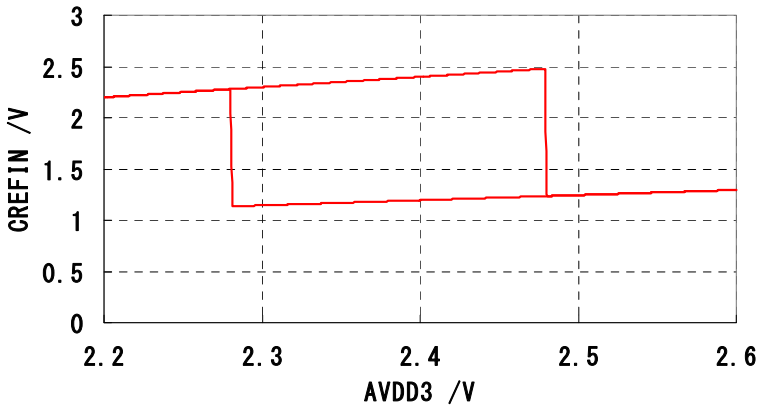
Please refer to a application note for details.

TYPICAL CHARACTERISTICS CURVES

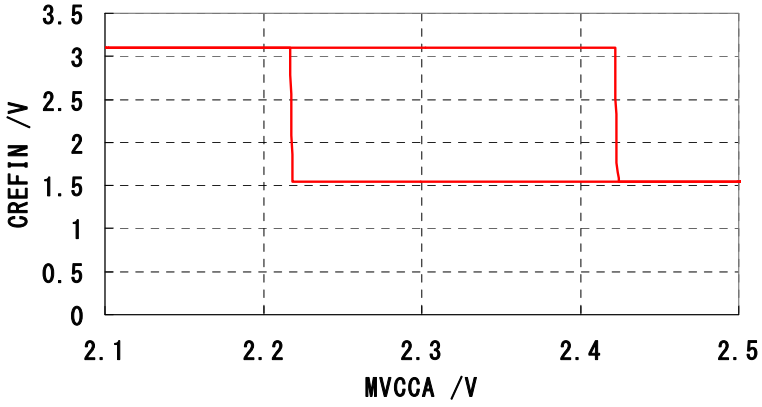
1,Super low noise Zoom and Focus drive.



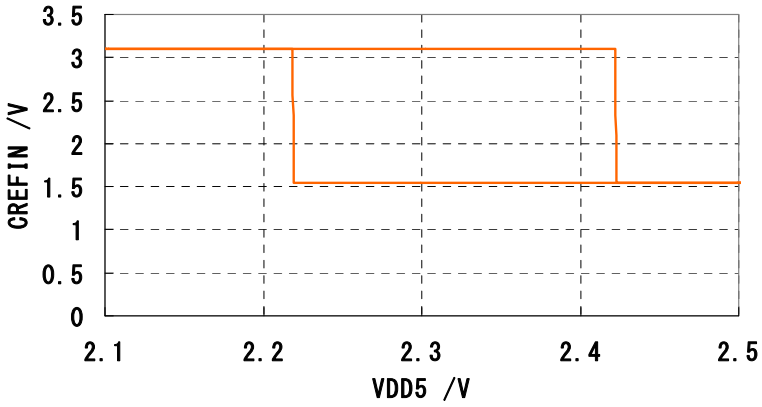
2,Characteristic of supply voltage monitor.



(1) AVDD3
Operation voltage : 2.28V
Return voltage : 2.48V



(2) MVCC
Operation voltage : 2.22V
Return voltage : 2.42V

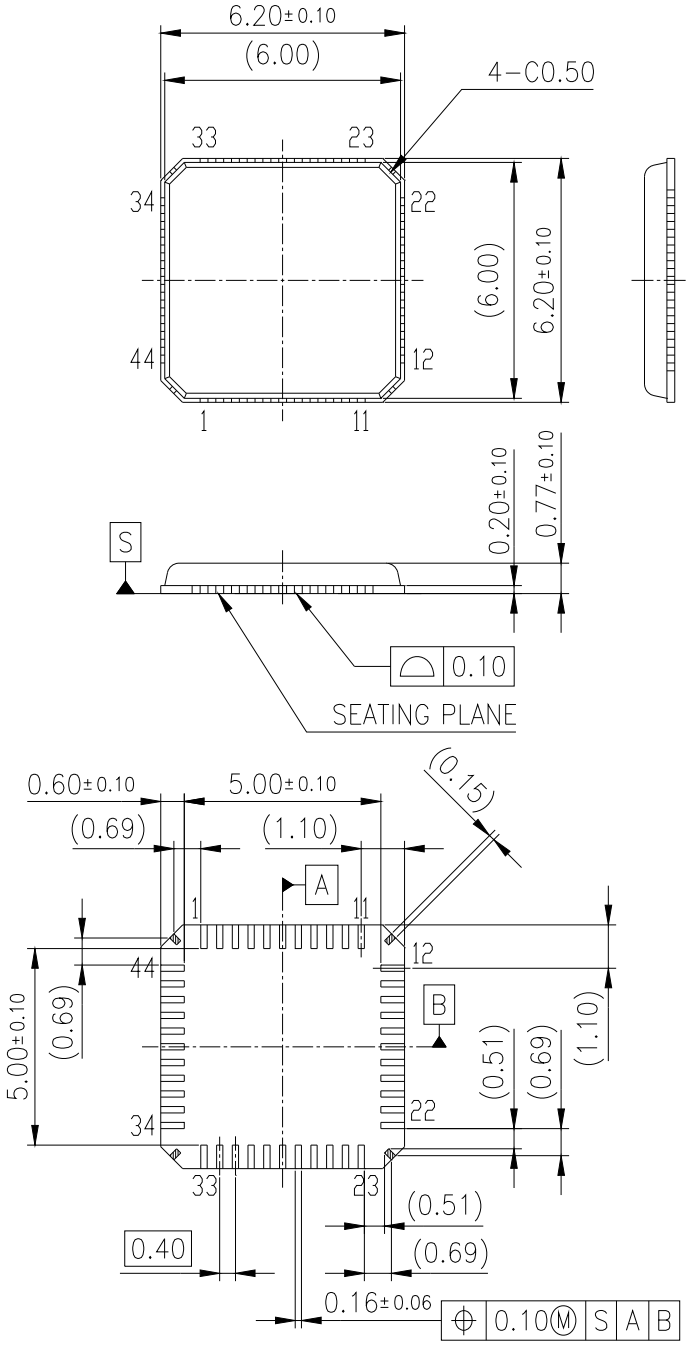


(3) VDD5
Operation voltage : 2.22V
Return voltage : 2.42V

PACKAGE INFORMATION (Reference Data)

Package Code: *QFN044-P-0606D

unit:mm



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

Panasonic

AN41908A

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(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
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3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Take time to check the characteristics on use. When changing an external circuit constant for use, consider not only static characteristics, but also transient characteristics and external parts with respect to the characteristics difference among ICs so that you can get enough margin. Moreover, consider the influence of electric charge remaining in an external capacitor on rising/falling of power supply.

12. Apply voltage from a low-impedance to power supply pins and connect a bypass capacitor to the LSI as near as possible.

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