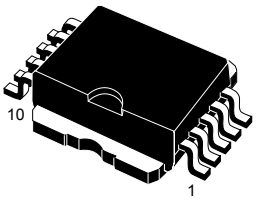
VN5T006ASP-E

Datasheet

Single channel high-side driver with analog current sense for 24 V automotive applications



PowerSO-10

Product status link
VN5T006ASP-E

Product summary	
Order code	**VN5T006ASP-E**
Package	PowerSSO-24
Packing	Tube
Order code	**VN5T006ASPTR-E**
Package	PowerSSO-24
Packing	Tape and reel

Features

Description	Parameter	Value
Max. transient supply voltage	V_{CC}	58 V
Operating voltage range	V_{CC}	8 to 36 V
Typ. on-state resistance (per channel)	R_{ON}	6 mΩ
Current limitation (typ.)	I_{LIM}	115 A
Off-state supply current	I_S	2 µA(1)

1. *Typical value with all loads connected.*

- AEC-Q100 qualified
- General
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Fault reset standby pin (FR_Stby)
- Diagnostic functions
  - Proportional load current sense
  - Current sense precision for wide range currents
  - Off-state openload detection
  - Output short to V_{CC} detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protected with self switch of the Power MOSFET
  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads

Description

The VN5T006ASP-E is a device made using STMicroelectronics VIPower technology, intended for driving resistive or inductive loads with one side connected to the ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense, which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature, or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the device in overload conditions. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and on the fault reset standby pin disables all outputs and sets the device in standby mode.

1 Block diagram and pin description

Figure 1. Block diagram

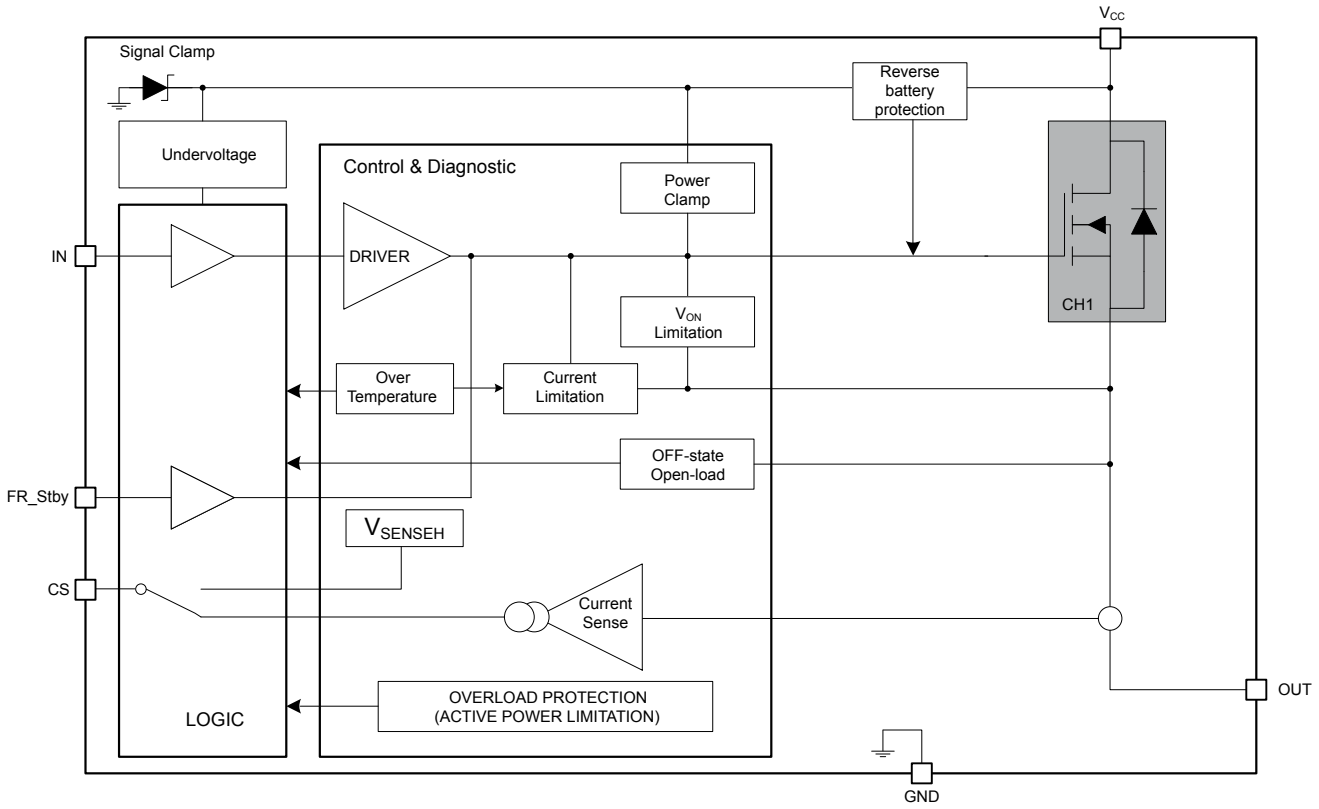


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
OUT	Power output.
GND	Ground connection.
IN	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state.
CS	Analog current sense pin, it delivers a current proportional to the load current.
FR_Stby	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram PowerSO-10 (top view)

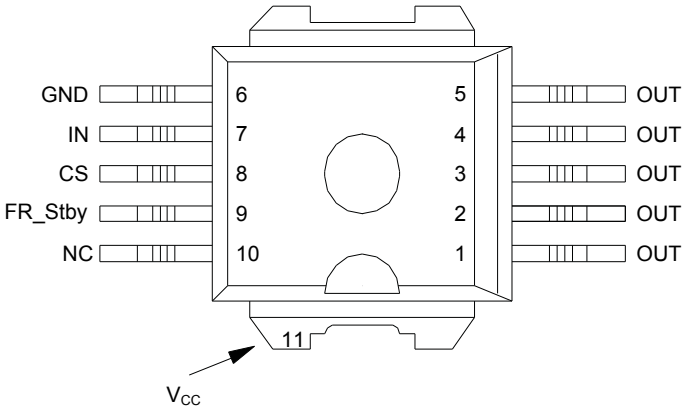


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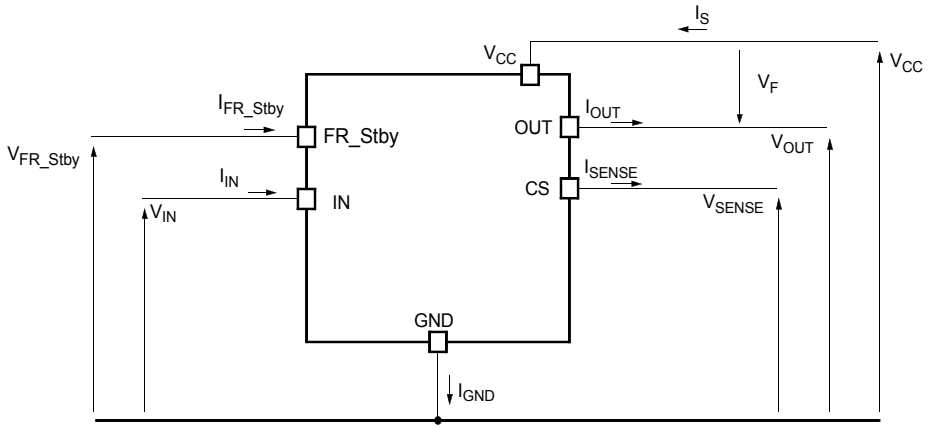
Table 2. Suggested connections for unused and not connected pins

Connection/pin	CurrentSense	NC	Output	Input	FR_Stby
Floating	Not allowed	X(1)	X	X	X
To ground	Through 10 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor

1. *X: do not care.*

2 Electrical specification

Figure 3. **Current and voltage conventions**



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. **Absolute maximum ratings**

Symbol	Parameter		Value	Unit
V_{CC}	DC supply voltage		58	V
$-V_{CC}$	Reverse DC supply voltage		-32	V
I_{OUT}	DC output current		Internally limited	A
$-I_{OUT}$	Reverse DC output current		90	A
I_{IN}	DC input current		-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current		-1 to 1.5	mA
V_{CSENSE}	Current sense maximum voltage		(V_{CC} - 58) to V_{CC}	V
E_{MAX}	Maximum switching energy (L = 10 mH; V_{BAT} = 32 V; T_{Jstart} = 150 °C; I_{OUT} = 8.9 A)		880	mJ
L_{smax}	Maximum stray inductance in short circuit condition R_L = 300 mΩ, V_{BAT} = 32 V, T_{Jstart} = 150 °C, I_{OUT} = $I_{limH\ (max.)}$		40	µH
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF)	IN	4000	V
		CS	2000	
		FR_Stby	4000	
		OUT	5000	
		V_{CC}	5000	
V_{ESD}	Charge device model (CDM-AEC-Q100-011)		750	V
T_J	Junction operating temperature		-40 to 150	°C
T_{stg}	Storage temperature		-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case (with one channel ON)	0.8	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	See Figure 27	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 36 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 10 A, T_J = 25 °C 8 V < V_{CC} < 36 V		6		mΩ
		I_{OUT} = 10 A, T_J = 150 °C 8 V < V_{CC} < 36 V			12	
$R_{ON\ REV}$	Reverse battery on-state resistance	V_{CC} = -24 V, I_{OUT} = -10 A, T_J = 25 °C			6	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	58	64	70	V
I_S	Supply current	Off-state, V_{CC} = 24 V, T_J = 25 °C, V_{IN} = V_{OUT} = V_{SENSE} = 0 V, V_{FR_Stby} = 0 V		2(1)	5(1)	µA
		On-state, V_{CC} = 24 V, V_{IN} = 5 V, I_{OUT} = 0 A		3	6	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V, V_{CC} = 24 V, T_J = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V, V_{CC} = 24 V, T_J = 125 °C	0		5	

1. *Power MOSFET leakage included.*

Table 6. Switching (V_{CC} = 24 V, T_J = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.4 Ω		32		µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.4 Ω		67		µs
$(dV_{OUT}/dt)_{(on)}$	Turn-on voltage slope	R_L = 2.4 Ω		0.7		V/µs
$(dV_{OUT}/dt)_{(off)}$	Turn-off voltage slope	R_L = 2.4 Ω		0.46		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 2.4 Ω		4.15		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 2.4 Ω		2.7		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
$V_{FR\_Stby\_L}$	Fault_reset_standby low level voltage				0.9	V
$I_{FR\_Stby\_L}$	Low level fault_reset_standby current	V_{FR_Stby} = 0.9 V	1			µA
$V_{FR\_Stby\_H}$	Fault_reset_standby high level voltage		2.1			V
$I_{FR\_Stby\_H}$	High level fault_reset_standby current	V_{FR_Stby} = 2.1 V			10	µA
$V_{FR\_Stby(hyst)}$	Fault_reset_standby hysteresis voltage		0.25			V
$V_{FR\_Stby\_CL}$	Fault_reset_standby clamp voltage	I_{FR_Stby} = 15 mA (t < 10 ms)	11		15	V
		I_{FR_Stby} = -1 mA		-0.7		V
t_{reset}	Overload latch-off reset time	See Figure 4	2		24	µs
t_{stby}	Standby delay	See Figure 5	120		1200	µs

Figure 4. t_{reset} definition

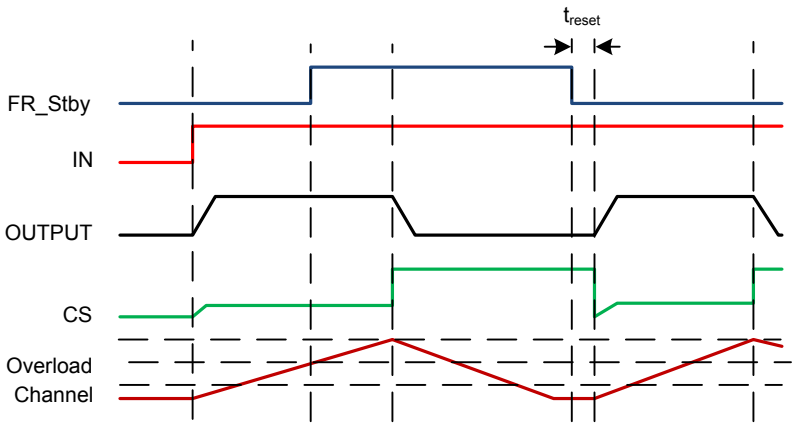


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Figure 5. t_{stby} definition

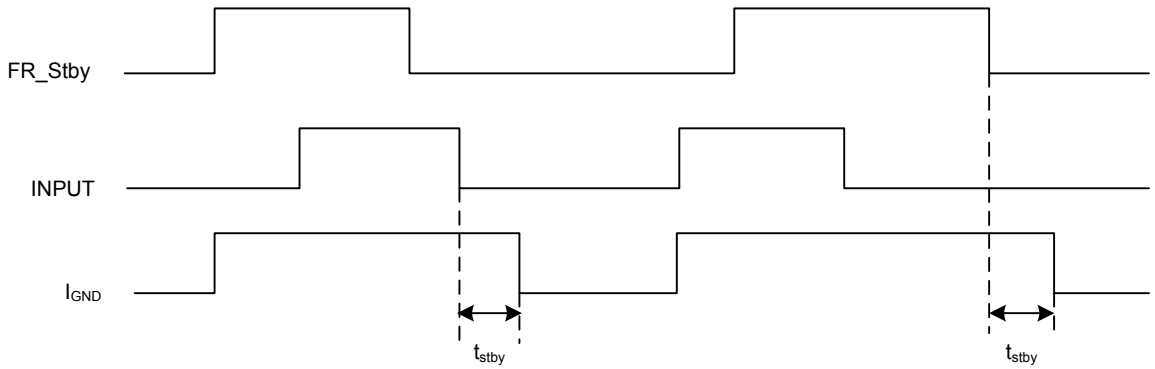

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Table 8. **Protections and diagnostics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 24 V	81	115	162	A
		5 V < V_{CC} < 36 V			162	
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 24 V, T_R < T_J < T_{TSD}		29		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 10 A, V_{IN} = 0 V, L = 6 mH	V_{CC} - 58	V_{CC} - 64	V_{CC} - 70	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1 A, T_J = -40 °C to 150 °C		25		mV

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.6 A, V_{SENSE} = 0.5 V, T_J = -40 °C to 150 °C	3930	11250	19850	
		I_{OUT} = 0.6 A, V_{SENSE} = 0.5 V, T_J = 25 °C to 150 °C	5035		17055	
dK_0/K_0 (1)	Current sense ratio drift	I_{OUT} = 0.6 A, V_{SENSE} = 0.5 V, T_J = -40 °C to 150 °C	-30		30	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1.6 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	5600	10750	16940	
		I_{OUT} = 1.6 A, V_{SENSE} = 1 V, T_J = 25 °C to 150 °C	6215		14660	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 1.6 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	-28		25	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 2.4 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	6030	10370	15865	
		I_{OUT} = 2.4 A, V_{SENSE} = 1 V, T_J = 25 °C to 150 °C	6200		13635	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 2.4 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	-26		23	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	6040	10070	15285	
		I_{OUT} = 3 A, V_{SENSE} = 2 V, T_J = 25 °C to 150 °C	6040		13090	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 3 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	-25		22	%
K_4	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	5845	8670	13630	
		I_{OUT} = 6 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	6000		10895	
dK_4/K_4 (1)	Current sense ratio drift	I_{OUT} = 6 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-20		20	%
K_5	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	5920	8400	11520	
		I_{OUT} = 10 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	6730		9765	
dK_5/K_5 (1)	Current sense ratio drift	I_{OUT} = 10 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-15		15	%
K_6	I_{OUT}/I_{SENSE}	I_{OUT} = 20 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	6960	8330	10090	
dK_6/K_6 (1)	Current sense ratio drift	I_{OUT} = 20 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-8		8	%
dK/K_{BULB1} (1)	Current sense ratio drift	I_{OUT} = 0.6 A to 6 A, I_{OUTCAL} = 3 A, V_{SENSE} = 0.5 V, T_J = -40 °C to 150 °C	-30		50	%
dK/K_{BULB2} (1)	Current sense ratio drift	I_{OUT} = 1.6 A to 4.2 A, I_{OUTCAL} = 3 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	-30		26	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dK/K_{BULB3} (1)	Current sense ratio drift	I_{OUT} = 0.6 A to 2.4 A, I_{OUTCAL} = 1.6 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	-27		25	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 0 V, T_J = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 5 V, T_J = -40 °C to 150 °C	0		2	
V_{SENSE}	Max. analog sense output voltage	I_{OUT} = 40 A, R_{SENSE} = 3.9 kΩ	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} = 24 V, R_{SENSE} = 3.9 kΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition(2)	V_{CC} = 24 V, V_{SENSE} = 5 V		9	12	mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 1 A < I_{OUT} < 40 A, I_{SENSE} = 90% of $I_{SENSEMAX}$ (see Figure 6)		300	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX}, I_{OUTMAX} = 10 A (see Figure 10)			450	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 1 A < I_{OUT} < 40 A, I_{SENSE} = 10% of $I_{SENSEMAX}$ (see Figure 6)		5	20	µs

1. *Specified by design, not tested in production.*
2. *Fault condition includes: power limitation, overtemperature and openload in off-state condition.*

Table 10. Openload detection (V_{FR_Stby} = 5 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Openload off-state voltage detection threshold	V_{IN} = 0 V, 8 V < V_{CC} < 36 V	2	-	4	V
t_{DSTKON}	Output short circuit to VCC detection delay at turn off	See Figure 7	180	-	1800	µs
$I_{L(off2)}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V, V_{SENSE} = 0 V, V_{OUT} rising from 0 V to 4 V	-120	-	0	µA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in openload	V_{OUT} = 4 V, V_{IN} = 0 V, V_{SENSE} = 90 % of V_{SENSEH}, R_{SENSE} = 3.9 kΩ		-	20	µs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FR_Stby activation	Input = low (see Figure 9)		-	50	µs

Figure 6. Current sense delay characteristics

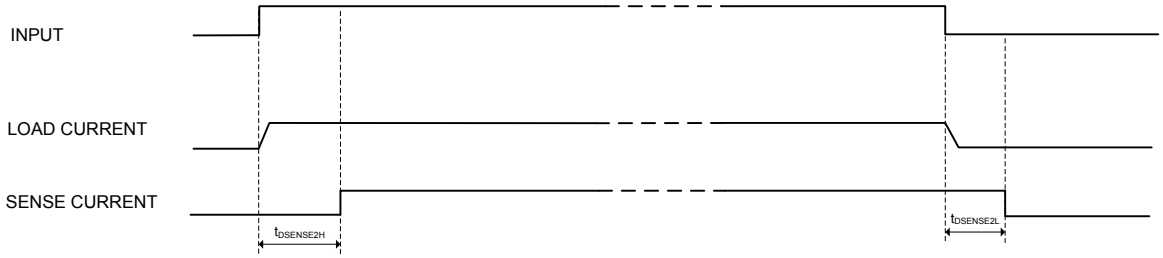

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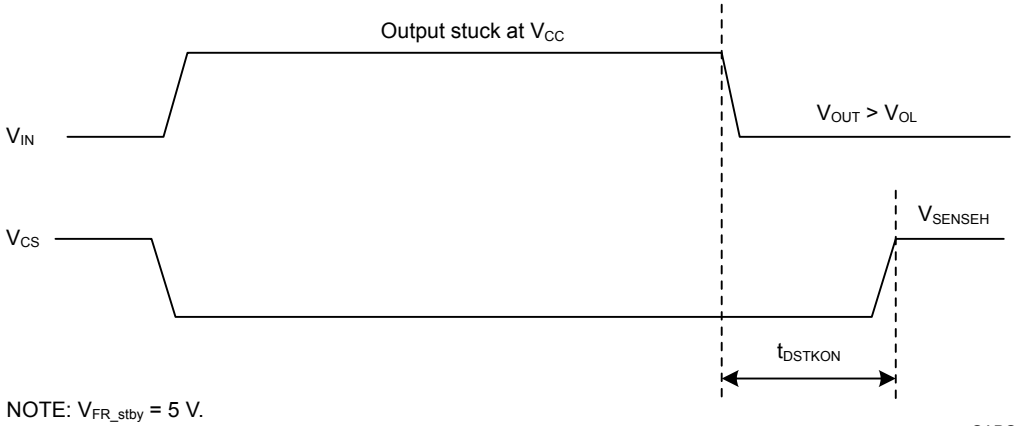
Figure 7. Openload off-state delay timing



NOTE: V_{FR_stby} = 5 V.

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Figure 8. **Switching characteristics**

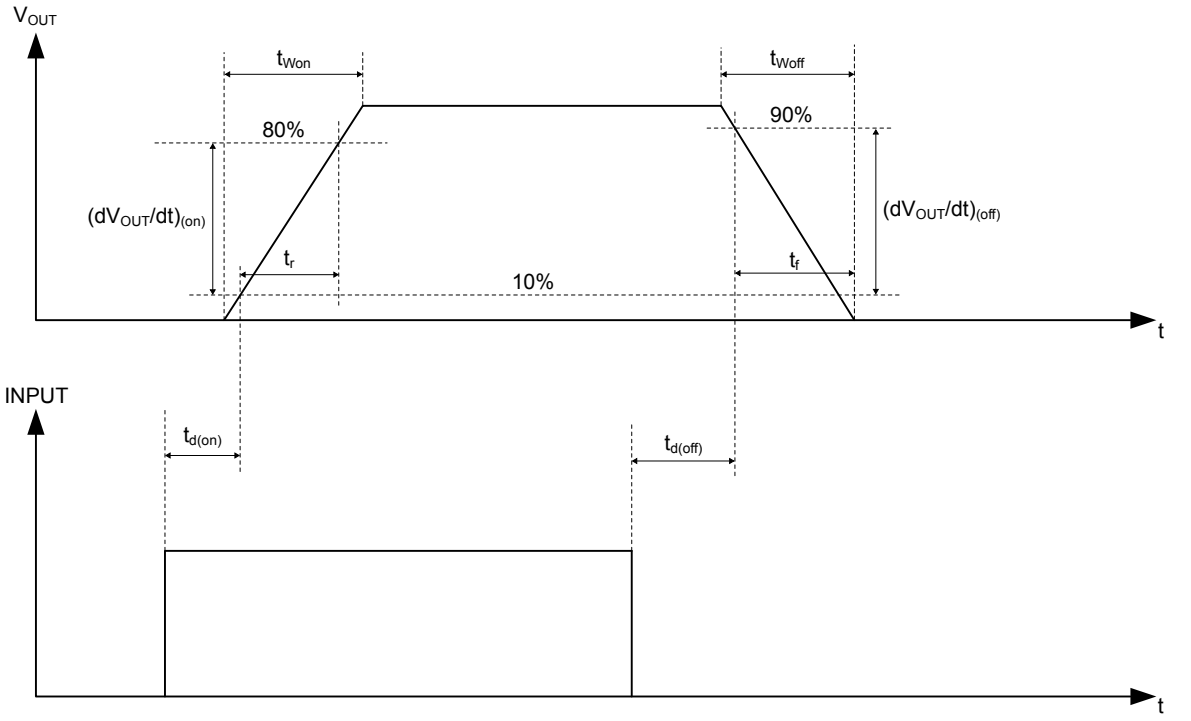

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Figure 9. **Output stuck to V_{CC} detection delay time at FR_Stby activation**

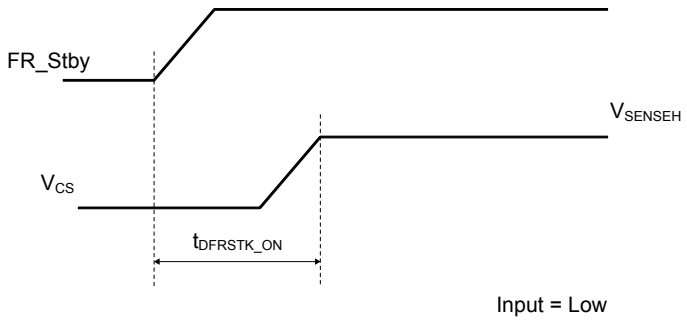

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Figure 10. Delay response time between rising edge of ouput current and rising edge of current sense

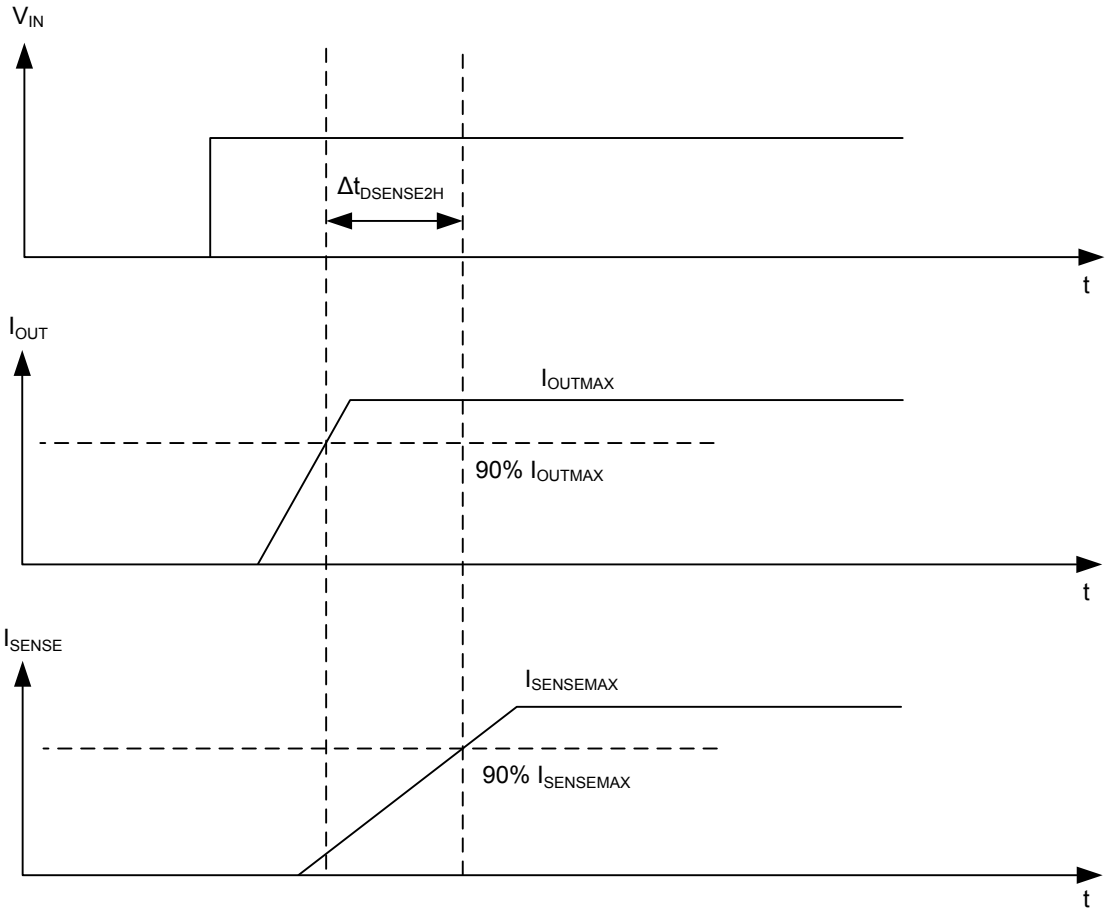


Figure 11. Output voltage drop limitation

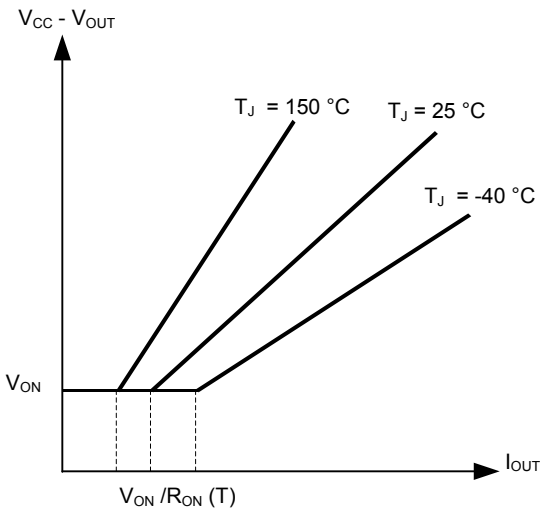
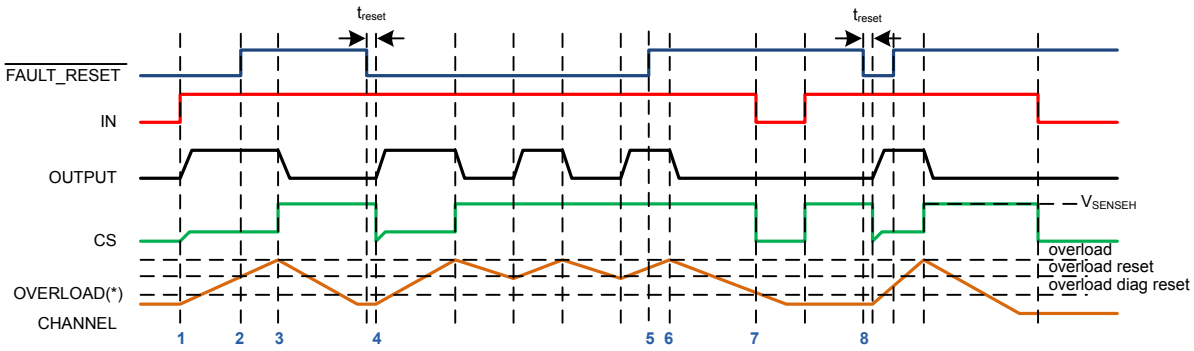


Figure 12. Device behavior in overload condition



1: OUTPUT and CS controlled by IN
2: FAULT_RESET from '0' to '1' → no action on CS pin
3: overload latch-off. IN high → CS high
4: FAULT_RESET low AND Temp channel < overload_reset → overload latch reset after t_{reset}
4 to 5: FAULT_RESET low AND IN high → thermal cycling, CS high
5: FAULT_RESET high → latch-off reset disabled
6 to 7: overload event and FAULT_RESET high → latch-off, no thermal cycling
7 to 8: overload diagnostic disabled/enabled by the input
8: overload latch-off reset by FAULT_RESET

(*) OVERLOAD = thermal shutdown OR power limitation

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Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature/short to ground	X	L	L	0
	L	H	Cycling	V_{SENSEH}
	H	H	Latched	V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	< Nominal
Openload off-state (with pull-up)	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	0
Negative output voltage clamp	X	L	Negative	0

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004 (E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedence
	III	IV				
1	-450 V	-600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	37 V	50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	- 150 V	- 200 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+ 150 V	+ 200 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4	- 12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+ 123 V	+ 174 V	1 pulse			350 ms, 1 Ω

1. *The above test levels must be considered referred to V_{CC} = 24.5 V except for pulse 5b.*
2. *Valid in case of external load dump clamp: 58 V maximum referred to ground.*

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004 (E) Test pulse	Test level results	
	III	IV
1	C	C(1)
2a	C	C
3a	C	C
3b(2)	E	E
3b(3)	C	C
4	C	C
5b(4)	C	C

1. *With R_{LOAD} < 24 Ω.*
2. *Without capacitor between V_{CC} and GND.*
3. *With 10 nF between V_{CC} and GND.*
4. *External load dump clamp, 58 V maximum, referred to ground.*

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics (curves)

Figure 13. Off-state output current

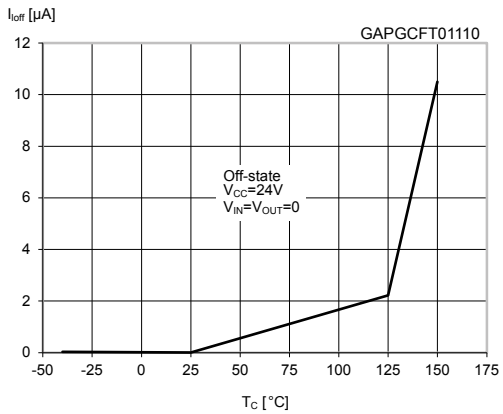


Figure 14. High level input current

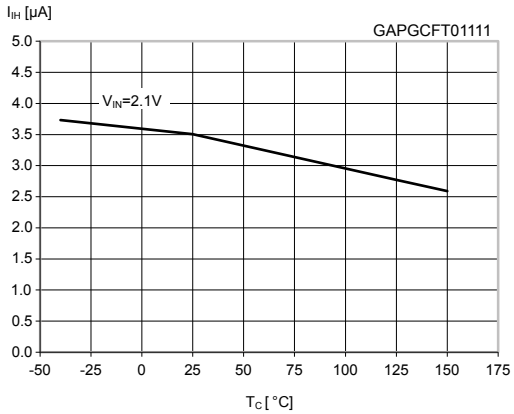


Figure 15. Input clamp voltage

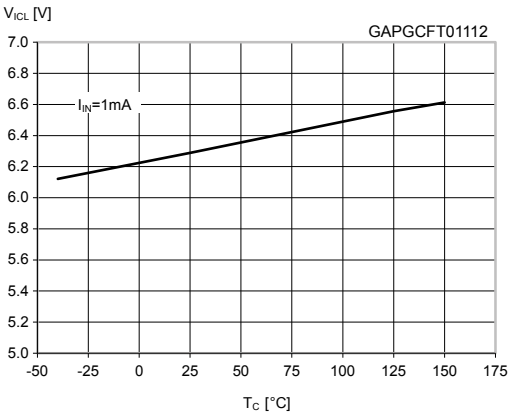


Figure 16. Low level input voltage

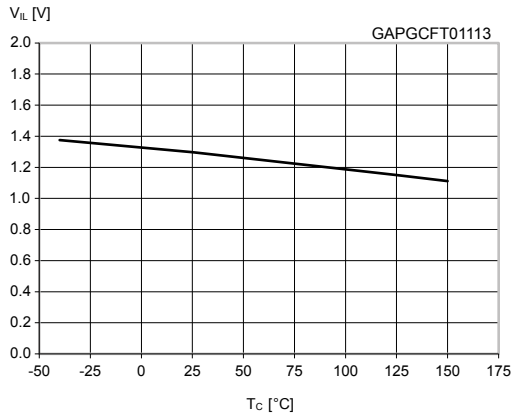


Figure 17. High level input voltage

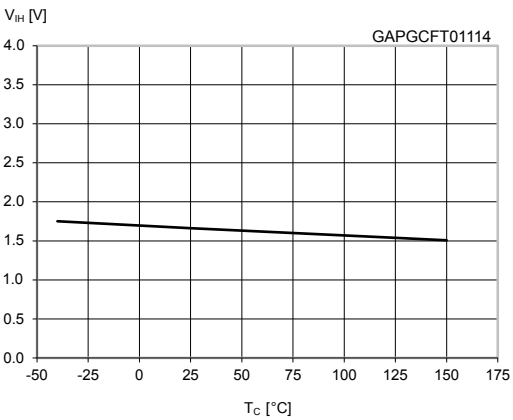


Figure 18. Input hysteresis voltage

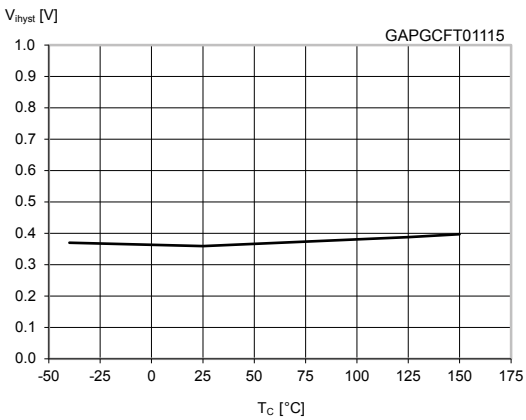


Figure 19. On-state resistance vs T_C

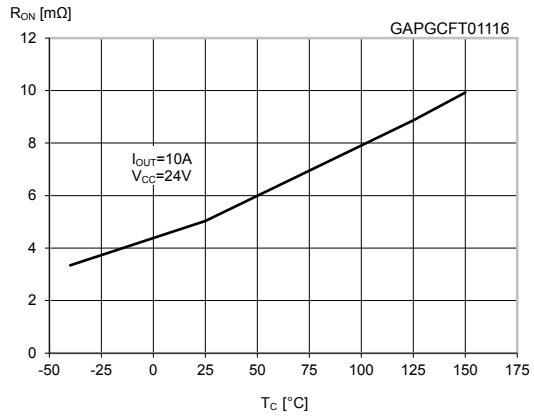


Figure 20. On-state resistance vs V_{CC}

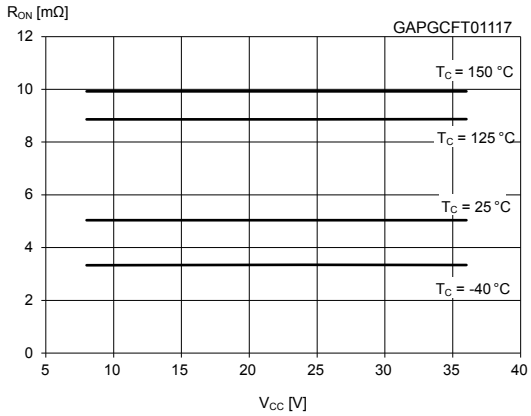


Figure 21. Turn-on voltage slope

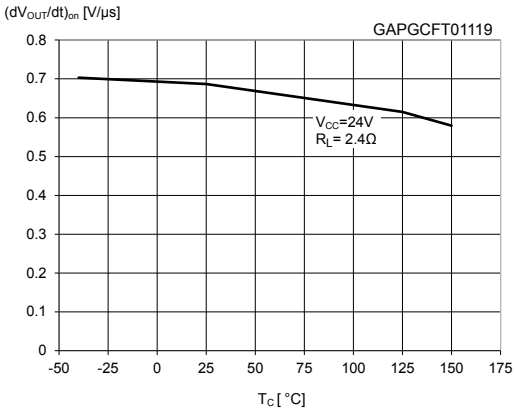


Figure 22. Turn-off voltage slope

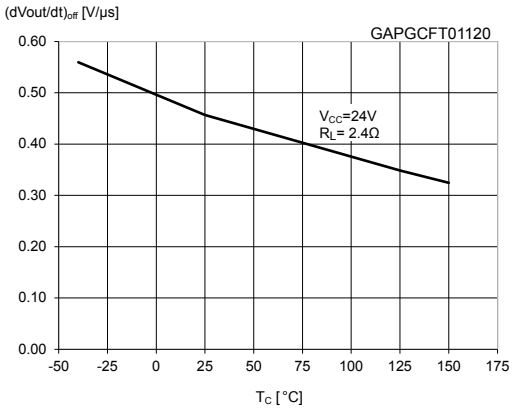
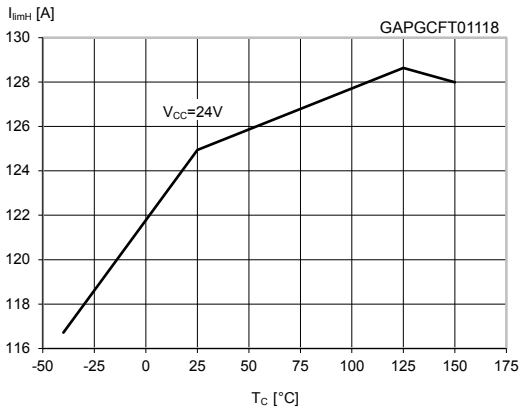
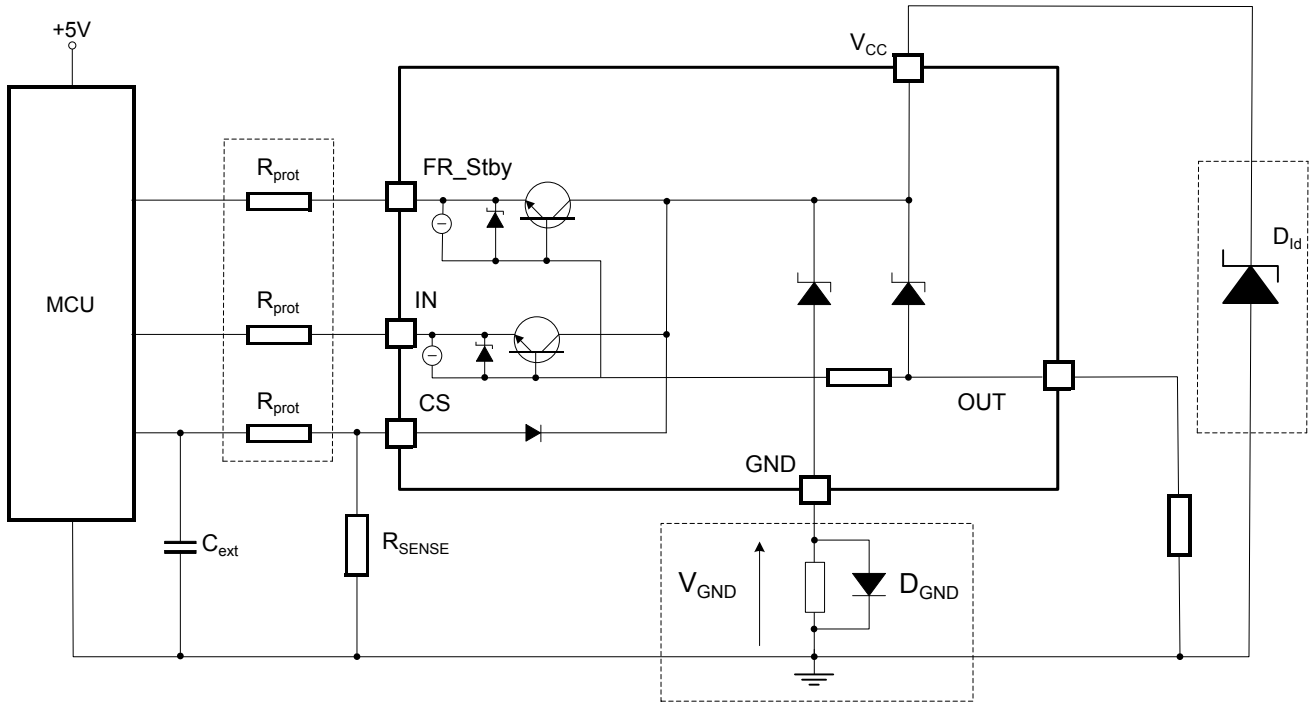


Figure 23. I_{LIMH} vs T_C



3 Application information

Figure 24. **Application schematic**



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3.1 Load dump protection

D_{Id} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2 2004 (E) Table 12, Table 13 and Table 14.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests that a resistor (R_{prot}) has to be inserted in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation: R_{prot} range calculation

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$

Calculation example:

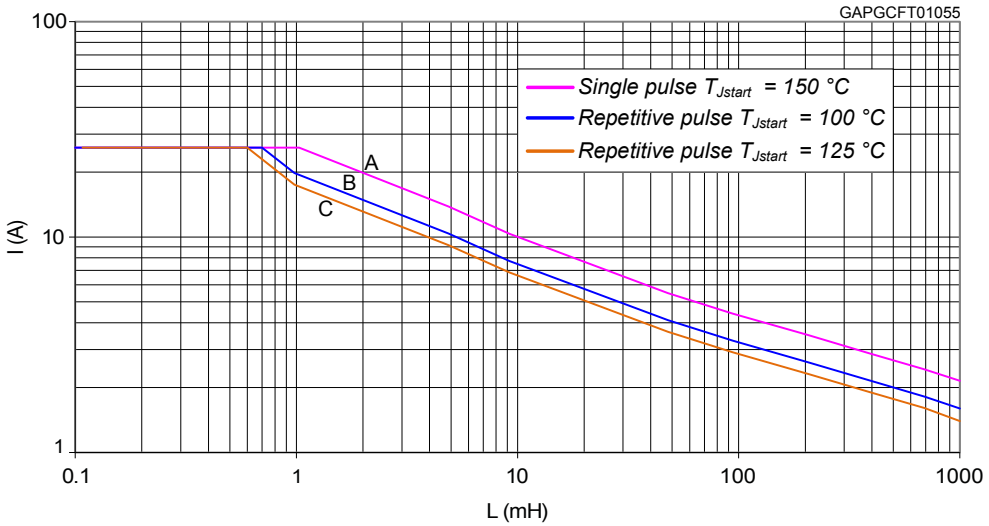
For V_{CCpeak} = -600 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

30 kΩ ≤ R_{prot} ≤ 190 kΩ.

Recommended value: R_{prot} = 56 kΩ.

4 Maximum demagnetization energy (V_{CC} = 24 V)

Figure 25. Maximum turn off current versus inductance

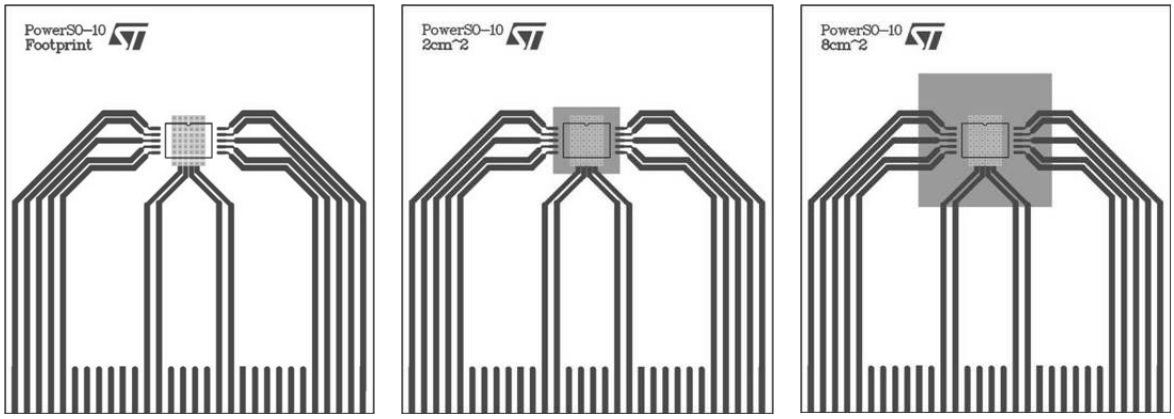


Note: Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{Jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

5.1 PowerSO-10 thermal data

Figure 26. **PowerSO-10 PCB**



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Layout condition of R_{th} and Z_{th} measurements: board finish thickness 1.6 mm ±10%; board double layer; board dimension 77 x 86; board material FR4; Cu thickness 0.070 mm (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm ±0.08 mm; Cu thickness on vias 0.025 mm.

Figure 27. **R_{thJA} vs PCB copper area in open box free air condition**

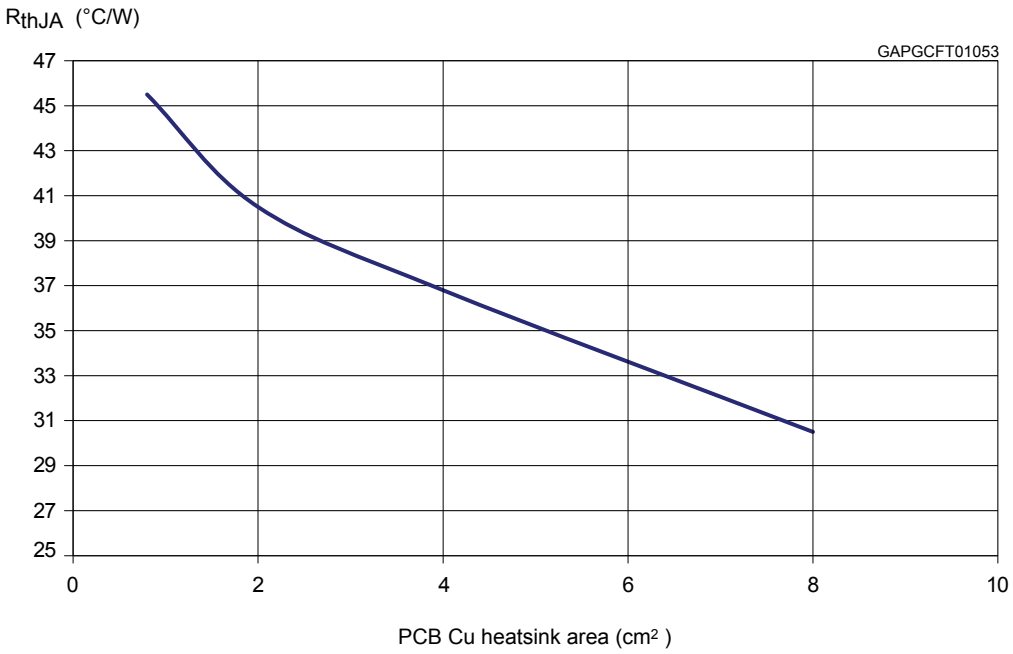


Figure 28. PowerSO-10 thermal impedance junction ambient single pulse

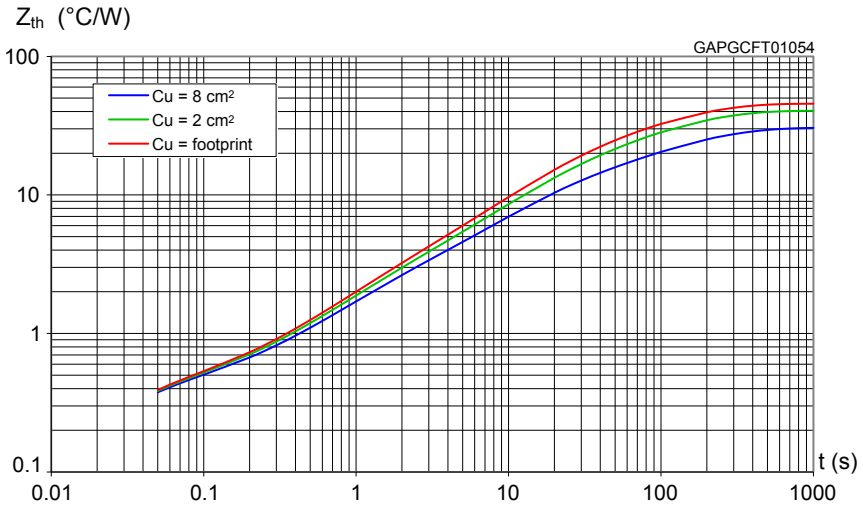
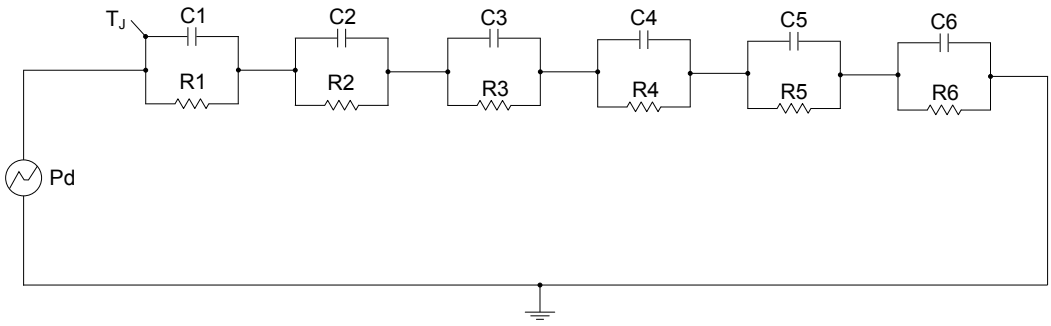


Figure 29. Thermal fitting model of a single channel HSD in PowerSO-10



The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered

Equation: pulse calculation formula

$Z_{th\delta} = R_{th} \cdot \delta + Z_{thtp} (1 - \delta)$

where $\delta = t_P/T$

Table 15. **Thermal parameters**

Area/island (cm^2)	Footprint	4	8
R1 (°C/W)	0.05		
R2 (°C/W)	0.3		
R3 (°C/W)	1.2		
R4 (°C/W)	7		
R5 (°C/W)	13	12	8
R6 (°C/W)	24	20	14
C1 (W.s/°C)	0.05		
C2 (W.s/°C)	0.1		
C3 (W.s/°C)	1		
C4 (W.s/°C)	2		
C5 (W.s/°C)	3	4	8
C6 (W.s/°C)	6	8	14

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 PowerSO-10 package information

Figure 30. PowerSO-10 package dimensions

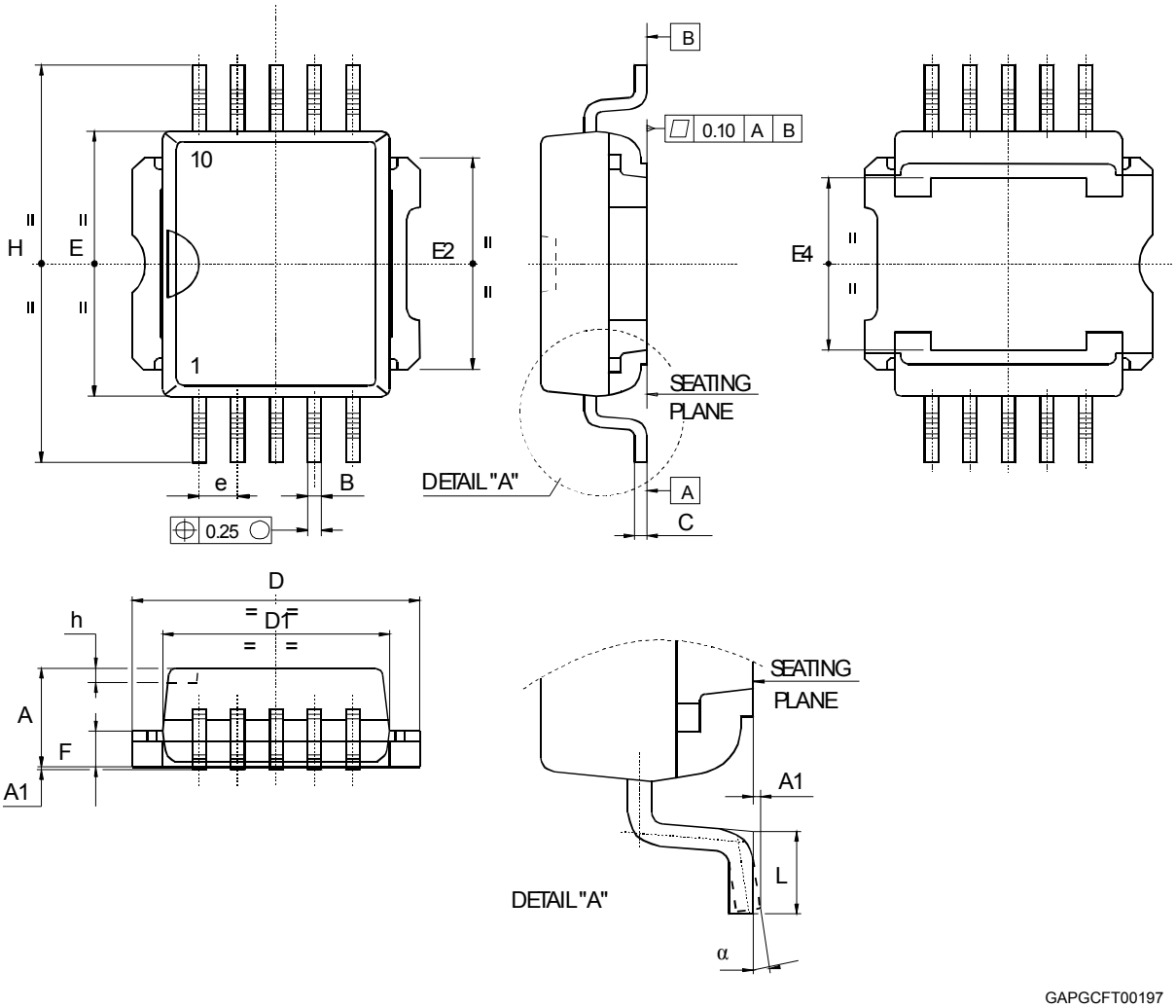


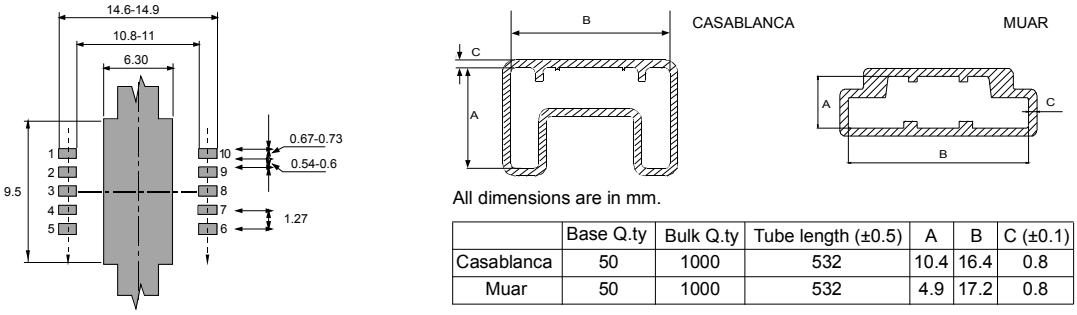
Table 16. PowerSO-10 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
a	0°		8°
α(1)	2°		8°

1. *Muar only POA P013P.*

6.2 PowerSO-10 packing information

Figure 31. **PowerSO-10 tube shipment (no suffix)**



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (±0.5)	A	B	C (±0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

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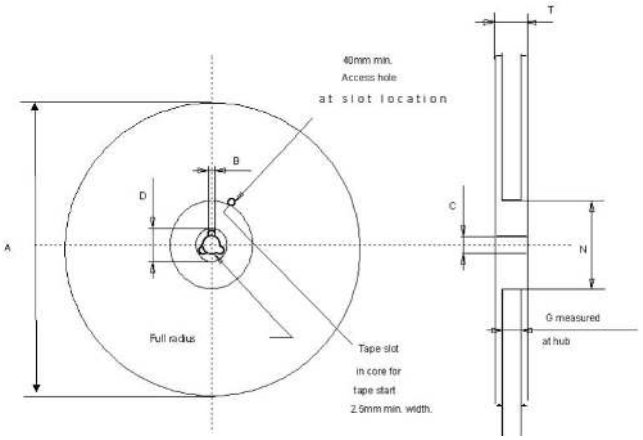
Figure 32. **PowerSO-10 tape and reel shipment (suffix “TR”)**



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

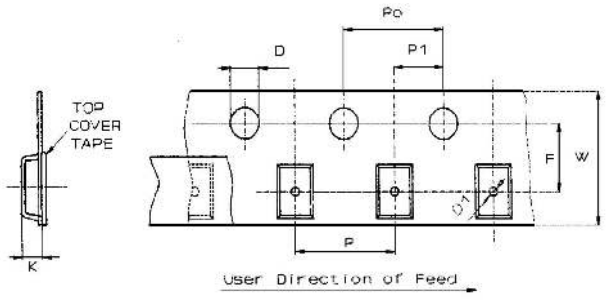
All dimensions are in mm.

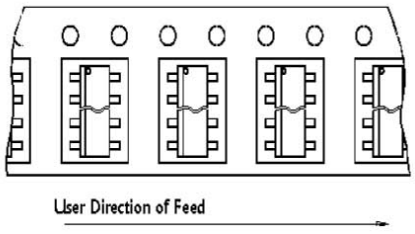
TAPE DIMENSIONS

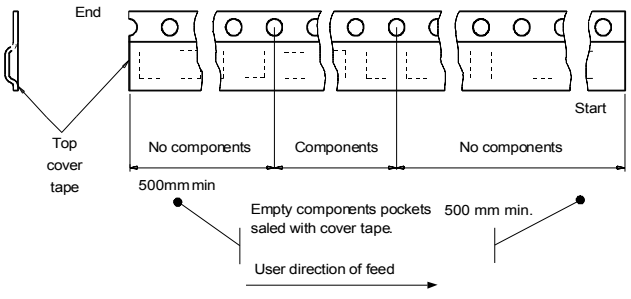
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







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Revision history

Table 17. **Document revision history**

Date	Revision	Changes
19-Dec-2012	1	Initial release.
16-Jan-2013	2	Updated *Figure 3: Current and voltage conventions* *Table 6: Switching (V_{CC} = 24 V; T_J = 25 °C)*: – $dV_{OUT}/dt_{(on)}$, $dV_{OUT}/dt_{(off)}$: updated values *Table 9: Current sense (8 V < VCC < 36 V)*: – I_{OL}: removed row – dK/K_{BULB2}, dK/K_{BULB3}: updated test conditions Updated *Table 22: Turn-On voltage slope* and *Table 23: Turn-Off voltage slope*.
16-Jun-2013	3	Changed document status from “preliminary data” to “production data”.
17-Sep-2013	4	Updated Disclaimer.
11-Apr-2016	5	Added AEC-Q101 qualified in *Features* section *Table 9: Current sense (8 V < V_{CC} < 36 V)*: – dK_6/K_6: updated test conditions
17-May-2022	6	Updated Figure 9 and Figure 12 Moved *Section 3.3: Maximum demagnetization energy (V_{CC} = 24 V)* to Section 4 Maximum demagnetization energy (VCC = 24 V). Updated title of Figure 28 and Figure 29 Minor text changes.

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