

## 74FR74 Dual D-Type Flip-Flop

### General Description

The 74FR74 is a dual D-type flip-flops with true and complement ( $\overline{Q}$ ) outputs. On the 74FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CP<sub>n</sub>). Both parts feature asynchronous clear (C<sub>Dn</sub>) and set (S<sub>Dn</sub>) inputs which are low level enabled.

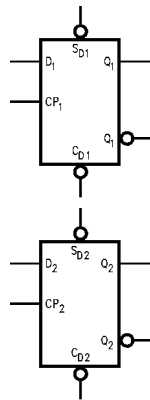
### Features

- 74FR74 is pin-for-pin compatible with the 74F74
- True 150 MHz f<sub>MAX</sub> capability on 74FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

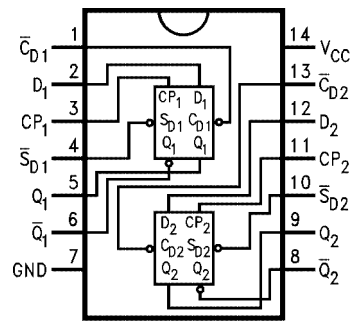
### Ordering Code:

Order Number	Package Number	Package Description
74FR74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74FR74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

### Logic Symbols



### Connection Diagram



### Pin Descriptions

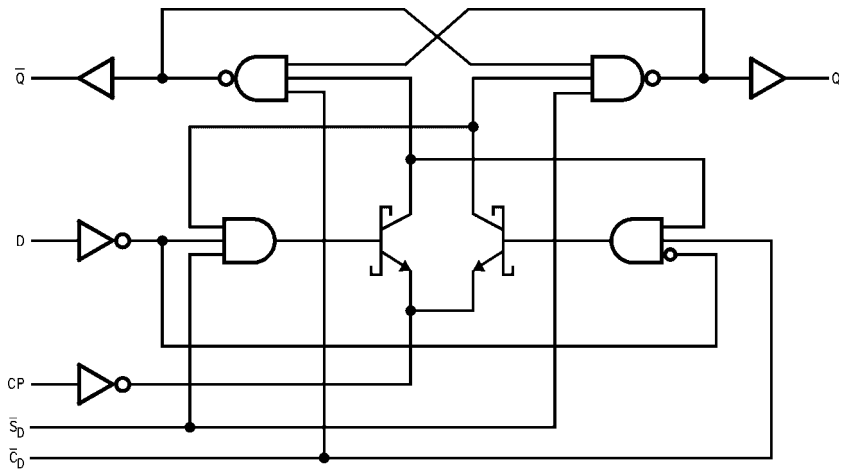
Pin Names	Description
D <sub>n</sub>	Data Inputs
CP <sub>n</sub>	Clock Inputs
S <sub>Dn</sub>	Asynchronous Set Inputs
C <sub>Dn</sub>	Asynchronous Clear Inputs
Q <sub>n</sub>	True Output
$\overline{Q}_n$	Complementary Output

### Truth Table

Inputs				Outputs	
$\overline{SD}$	$\overline{CD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	X	H	L
H	H	↗	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{Q}_0$

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance  
X = Immaterial  
↗ = Rising Edge  
Q<sub>0</sub> = Previous Q( $\overline{Q}$ ) before LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	2000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min	I <sub>OH</sub> = -1 mA
		2.4			V	Min	I <sub>OH</sub> = -3 mA
		2.0			V	Min	I <sub>OH</sub> = -24 mA
V <sub>OL</sub>	Output LOW Voltage			0.5	V	Min	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-150	μA	Max	V <sub>IN</sub> = 0.5V (D <sub>n</sub> , CP <sub>n</sub> )
				-1.8	mA	Max	V <sub>IN</sub> = 0.5V (C <sub>Dn</sub> , S <sub>Dn</sub> )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Test			3.75	V	0.0	V <sub>IOD</sub> = 150 mV, All Other Pins Grounded
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEx</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CC</sub>	Power Supply Current			24	mA	Max	

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	150	190		150		MHz
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	2.5	3.5	5.0	2.5	5.0	ns
t <sub>PHL</sub>	CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	2.5	4.5	6.0	2.5	6.0	
t <sub>PLH</sub>	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	1.5	3.5	5.5	1.5	5.5	ns
t <sub>PHL</sub>	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	2.0	5.5	7.0	2.0	7.0	
t <sub>OSHL</sub> (Note 3)	Pin to Pin Skew for HL Transitions					1.0	ns
t <sub>OSLH</sub> (Note 3)	Pin to Pin Skew for LH Transitions					1.0	ns
t <sub>OST</sub> (Note 3)	Pin to Pin Skew for HL/LH Transitions					3.0	ns
t <sub>O<math>\overline{Q}</math></sub> (Note 3)	True/Complement Output Skew					1.8	ns
t <sub>PS</sub> (Note 3)	Pin (Signal) Transition Variation					1.8	ns

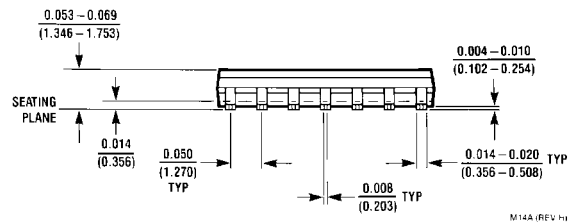
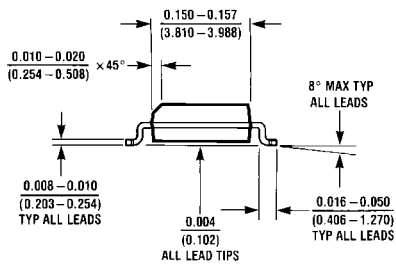
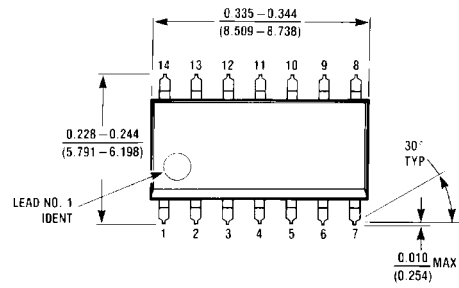
**Note 3:** Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>) or in opposite directions both HL and LH (t<sub>OST</sub>). t<sub>OST</sub> is guaranteed by design.

## AC Operating Requirements

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	2.5		2.5		ns
t <sub>S</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	2.5		2.5		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0		0		ns
t <sub>H</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	0		0		
t <sub>W</sub> (H)	CP <sub>n</sub> Pulse Width	3.3		3.3		ns
t <sub>W</sub> (L) (Note 4)	HIGH or LOW	3.3		3.3		
t <sub>W</sub> (L)	$\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ Pulse Width	4.0		4.0		ns
t <sub>REC</sub>	Recovery Time $\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ to CP <sub>n</sub>	2.0		2.0		ns

**Note 4:** This specification is guaranteed by design.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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