19-0670; Rev 0; 11/06

EVALUATION KIT AVAILABLE

Dual and Combinable Graphics Core Controller for Notebook Computers

General Description

The MAX8775 is a dual, step-down, interleaved, fixed-frequency, switch-mode power-supply (SMPS) controller with synchronous rectification. It is intended for GPU cores and I/O power generation in battery-powered systems. Flexible configuration allows the MAX8775 to operate as two independent single-phase regulators, or as one high-current two-phase regulator.

Configured in separate mode, the MAX8775 provides power to two dynamic voltage rails, one for the GPU core and the other for the I/O power rail. Configured in combined mode, the MAX8775 functions as a two-phase, high-current, single-output GPU core regulator, powering the high-performance GPU engines used in gaming machines and media center notebooks.

The REFIN voltage setting allows for multiple dynamic output voltages required by the different GPU operating and sleep states. Automatic fault blanking, forced-PWM operation, and transition control are achieved by detecting the voltage change at REFIN. Fixed-frequency operation with 180° out-of-phase interleaving minimizes input ripple current from the lowest input voltages up to the 26V maximum input. Current-mode control allows the use of low-ESR output capacitors. Internal integrators maintain high output accuracy over the full line-and-load range, in both forced-PWM mode and pulse-skipping mode. True differential current sensing provides accurate output current limit and current balance when operated in combined mode. Independent on/off and skip control allows flexible power sequencing and power management. Voltage-controlled soft-start reduces inrush current. Soft-stop gradually ramps the output voltage down, preventing negative voltage dips.

Applications

2 to 4 Li+ Cells Battery-Powered Devices

Media Center and Gaming Notebooks

GPU and I/O Power Supplies

Tracking Output Power Supplies

Features

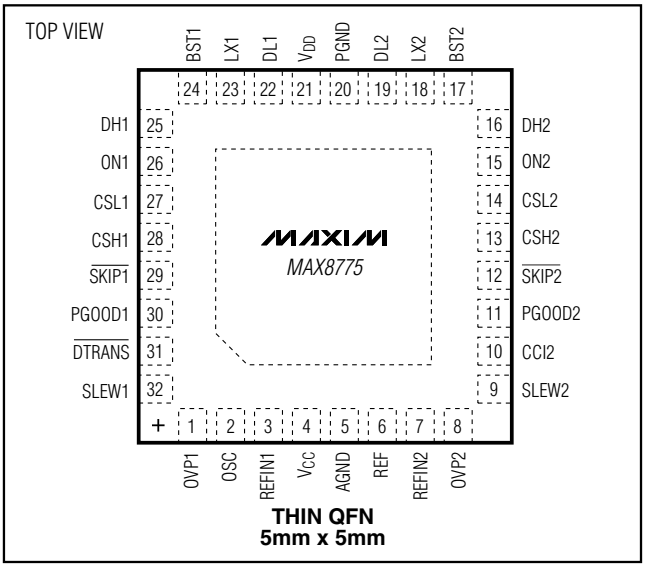
- **Dual-Output, Fixed-Frequency, Current-Mode Control**
- **Combinable Output for Higher Currents**
- **Dynamic Output Voltages with Automatic Fault Blanking and Transition Control**
- **True Out-of-Phase Operation**
- **True Differential Current Sense for Accurate Current Limit and Current Balance**
- **4V to 26V Input Range**
- **100kHz to 600kHz Switching Frequency**
- **0.5V to 2.5V Adjustable Outputs**
- **Internal Integrator for High Output Accuracy**
- **Stable with Low-ESR Output Capacitors**
- **Independent Selectable PWM and Skip-Mode Operation**
- **Independent Power-Good Outputs**
- **Soft-Start and Soft-Stop**
- **2.5V Precision Reference**
- **< 1µA Typical Shutdown Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8775ETJ+	-40°C to +85°C	32 Thin QFN 5mm x 5mm	T3255-5

+Denotes lead-free package.

Pin Configuration



THIN QFN 5mm x 5mm

Dual and Combinable Graphics Core Controller for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{CC}, CSH_, CSL_ to AGND .....-0.3V to +6V
ON_, $\overline{SKIP\_}$, PGOOD_ to AGND .....-0.3V to +6V
OVP_, REFIN_ to AGND .....-0.3V to +6V
$\overline{DTRANS}$ to AGND .....-0.3V to +6V
REF, OSC, SLEW_, CCI2 to AGND .....-0.3V to (V_{CC} + 0.3V)
BST1, BST2 to AGND .....-0.3V to +36V
LX1 to BST1 .....-6V to +0.3V
LX2 to BST2 .....-6V to +0.3V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
DL1, DL2 to PGND .....-0.3V to (V_{DD} + 0.3V)
AGND to PGND .....-0.3V to +0.3V
REF Short Circuit to AGND .....Continuous
REF Current .....+10mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin, 5mm x 5mm, Thin QFN
(derate 21.3mW/°C above +70°C) 1702mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP\_}$ = PGND = AGND, ON_ = V_{CC} = 5V, separate mode, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}		4		26	V
	V_{BIAS}	V_{CC}, V_{DD}	4.5		5.5	
V_{CC} Undervoltage Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis	4.1	4.25	4.5	V
Quiescent Supply Current (V_{CC})	I_{CC}	CSL_ forced above their regulation points		1.5	2.5	mA
Quiescent Supply Current (V_{DD})	I_{DD}	CSL_ forced above their regulation points, SKIP mode		< 1	5	µA
Shutdown Supply Current (V_{CC})	$I_{CC(SHDN)}$	ON1 = ON2 = GND		< 1	5	µA
Shutdown Supply Current (V_{DD})	$I_{DD(SHDN)}$	ON1 = ON2 = GND		< 1	5	µA
SMPS CONTROLLERS						
Output Voltage Accuracy	$V_{REFIN\_}$ - $V_{CSL\_}$	With respect to REFIN_, REFIN_ = 0.5V to 2.5V, $\overline{SKIP\_}$ = V_{CC} or GND (Note 1)	-5	0	+5	mV
Output Voltage-Adjust Range	$V_{CSL\_}$	Either SMPS (Note 2)	0.5		2.5	V
REFIN Operating Voltage-Adjust Range	$V_{REFIN\_}$	Either SMPS (Note 2)	0.5		2.5	V
REFINOK Threshold		Either SMPS		0.1		V
REFIN Transient Detection Threshold		5mV (typ) hysteresis		±25		mV
Combined-Mode Enabled Threshold	V_{REFIN2}		3	V_{CC} - 1	V_{CC} - 0.4	V
DC Load Regulation		Either SMPS, $\overline{SKIP\_}$ = V_{CC}, zero to full load		-0.1		%
Line Regulation Error		Either SMPS, 4V < V_{IN} < 26V		0.03		%/V
Switching-Frequency Accuracy (Note 3)	f_{OSC}	R_{OSC} = 143kΩ (f_{OSC} = 300kHz nominal)	-10		+10	%
		R_{OSC} = 71.5kΩ (f_{OSC} = 600kHz nominal) to 432kΩ (f_{OSC} = 99kHz nominal)	-15		+15	
Maximum Duty Factor	D_{MAX}		91	93		%
Minimum On-Time	t_{ONMIN}	(Note 4)			150	ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP\_}$ = PGND = AGND, ON_ = V_{CC} = 5V, separate mode, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SMPS1 to SMPS2 Phase Shift		SMPS2 starts after SMPS1			50		%
					180		Deg
Slew-Rate Current	$I_{SLEW\_}$	During transition		4.0	4.75	5.5	µA
	$I_{SLEWSS\_}$	Startup and shutdown		0.70	0.95	1.20	
CURRENT LIMIT							
Current-Limit Threshold	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$		26	30	34	mV
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP\_}$ = V_{CC}		-43	-36	-29	mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP\_}$ = GND			3		mV
Idle Mode™ Threshold	I_{MIN}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP\_}$ = GND		3.6	6	8.4	mV
REFERENCE (REF)							
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	T_A = +25°C to +85°C	2.482	2.50	2.518	V
			T_A = 0°C to +85°C	2.475	2.50	2.525	
Reference Source Load Regulation	ΔV_{REF}	I_{REF} = 0µA to 250µA			0.25	1.5	mV
Reference Sink Load Regulation		I_{REF} = -50µA				6	mV
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 100mV			2.3		V
CURRENT BALANCE							
Current-Balance Amplifier (GMI) Offset		[V(CSH1,CSL1) - V(CSH2,CSL2)] at I_{CCI} = 0		-2		+2	mV
Current-Balance Amplifier (GMI) Transconductance		$\Delta I_{CCI}/\Delta$[V(CSH1,CSL1) - V(CSH2,CSL2)], V_{CCI} = V_{OUT} = 0.5V to 2.5V, and V(CSH_,CSL_) = -60.0mV to +60.0mV			200		µS
FAULT DETECTION							
OVP_ Adjust Range	$V_{OVP\_}$			0.5		2.5	V
Output Overvoltage Trip Threshold		Rising edge measured at CSL_, with respect to OVP_ set voltage		180	200	220	mV
Output Overvoltage Fault Propagation Delay	t_{OVP}	50mV overdrive			10		µs
Output Undervoltage Protection Trip Threshold		Falling edge measured at CSL_, with respect to error comparator threshold		-325	300	-275	mV
Output Undevoltage Fault Propagation Delay	t_{UVP}	50mV overdrive			10		µs
Output Undervoltage Protection Blanking Time	t_{BLANK}	From rising edge of ON_			6144		$1/f_{SW}$
PGOOD_ Lower Trip Threshold		Falling edge measured at CSL_, with respect to error comparator threshold, hysteresis = 1%		-180	-150	-120	mV
PGOOD_ Propagation Delay	$t_{PGOOD\_}$	Falling edge, 50mV overdrive			10		µs

Idle Mode is a trademark of Maxim Integrated Products, Inc.

Dual and Combinable Graphics Core Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP\_}$ = PGND = AGND, ON_ = V_{CC} = 5V, separate mode, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD_ Output Low Voltage		I_{SINK} = 4mA				0.4	V
PGOOD_ Leakage Current	$I_{PGOOD\_}$	High state, PGOOD_ forced to 5.5V				1	µA
PGOOD_ Transition Blanking Time		Measured from the time CSL_ reaches the target voltage based on the slew rate set by $C_{SLEW\_}$			20		µs
Current-Balance Fault Comparator Thresholds		V(CCI2, REF), 0.5V ≤ V_{FB} ≤ 2.5V	Lower threshold, 0.84V_{REF}	2.0		2.2	V
			Upper threshold, 1.2V_{REF}	2.9		3.0	
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			+160		°C
GATE DRIVERS							
DH_ Gate Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V (Note 5)			1.5	5	Ω
DL_ Gate Driver On-Resistance (Note 5)	R_{DL}	DL_, high state			1.7	5	Ω
		DL_, low state			0.6	3	
DH_ Gate Driver Source/ Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2		A
DL_ Gate Driver Source Current	$I_{DL (SOURCE)}$	DL_ forced to 2.5V			1.7		A
DL_ Gate Driver Sink Current	$I_{DL (SINK)}$	DL_ forced to 2.5V			3.3		A
Dead Time	t_{DEAD}	DL_ to DH_		15	35		ns
		DH_ to DL_		10	26		
Internal Boost Diode Switch R_{ON}		Measure with 10mA of current			6.5	9	Ω
LX_, BST_ Leakage Current		$V_{BST\_}$ = $V_{LX\_}$ = 28V			< 2	20	µA
INPUTS AND OUTPUTS							
Logic Input Current		ON1, ON2, $\overline{DTRANS}$, $\overline{SKIP1}$, $\overline{SKIP2}$		-1		+1	µA
Logic Input-High Threshold		ON1, ON2, $\overline{DTRANS}$, $\overline{SKIP1}$, $\overline{SKIP2}$, hysteresis = 225mV		1.2	1.7	2.2	V
Input Leakage Current		CSH_, CSL_, 0V, or V_{DD}		-0.15		+0.15	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP\_}$ = 0, ON_ = V_{CC} = 5V, separate mode, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}		4		26	V
	V_{BIAS}	V_{CC}, V_{DD}	4.5		5.5	
V_{CC} Undervoltage Lockout	V_{UVLO}	Rising edge, 200mV typical hysteresis	4.1		4.5	V
Quiescent Supply Current (V_{CC})	I_{CC}	CSL_ forced above their regulation points			2.5	mA
Quiescent Supply Current (V_{DD})	I_{DD}	CSL_ forced above their regulation points			5	µA
Shutdown Supply Current (V_{CC})		ON1 = ON2 = GND			5	µA
Shutdown Supply Current (V_{DD})		ON1 = ON2 = GND			5	µA
MAIN SMPS CONTROLLERS						
PWM_ Output Voltage	$V_{REFIN\_}$ - $V_{CSL\_}$	With respect to REFIN_, REFIN_ = 0.5V to 2.5V, $\overline{SKIP\_}$ = V_{CC} or GND (Note 1)	-7.5		+7.5	mV
Output Voltage Adjust Range	$V_{CSL\_}$	Either SMPS (Note 2)	0.5		2.5	V
REFIN Operating Voltage Adjust Range	$V_{REFIN\_}$	Either SMPS (Note 2)	0.5		2.5	V
Combined Mode Enabled	V_{REFIN2}		3			V
Switching Frequency Accuracy (Note 2)	f_{OSC}	R_{OSC} = 143kΩ (f_{OSC} = 300kHz nominal)	-15		+15	%
		R_{OSC} = 71.5kΩ (f_{OSC} = 600kHz nominal) to 432kΩ (f_{OSC} = 99kHz nominal)	-20		+20	
Maximum Duty Factor	D_{MAX}		90			%
Slew-Rate Current	$I_{SLEW\_}$	During transition	3.75		5.50	µA
	$I_{SLEWSS\_}$	Startup and shutdown	0.7		1.2	
CURRENT LIMIT						
Current-Limit Threshold	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	25		35	mV
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	2.462		2.538	V
Reference Source Load Regulation	ΔV_{REF}	I_{REF} = 0µA to 250µA			2	mV
Reference Sink Load Regulation		I_{REF} = -50µA			10	mV
CURRENT BALANCE						
Current-Balance Amplifier (GMI) Offset		[V(CSH1,CSL1) - V(CSH2,CSL2)] at I_{CCI} = 0	-3		+3	mV

Dual and Combinable Graphics Core Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP\_}$ = 0, ON_ = V_{CC} = 5V, separate mode, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT DETECTION							
OVP_ Adjust Range	$V_{OVP\_}$			0.5		2.5	V
Output Overvoltage Trip Threshold		Rising edge measured at CSL_, with respect to OVP_ set voltage		180		220	mV
Output Undervoltage Protection Trip Threshold		Falling edge measured at CSL_, with respect to error comparator threshold		275		325	mV
PGOOD_ Lower Trip Threshold		Falling edge measured at CSL_ with respect to error comparator threshold, hysteresis = 1%		-180		-120	mV
PGOOD_ Output Low Voltage		I_{SINK} = 4mA				0.4	V
Current-Balance Fault Comparator Thresholds		V(CCI2, REF), 0.5V ≤ V_{FB} ≤ 2.5V	Lower threshold, $0.84V_{REF}$	2.0		2.2	mV
			Upper threshold, $1.2V_{REF}$	2.9		3.1	
GATE DRIVERS							
DH_ Gate Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V (Note 4)				5	Ω
DL_ Gate Driver On-Resistance (Note 4)	R_{DL}	DL_, high state				5	Ω
		DL_, low state				3	
INPUTS AND OUTPUTS							
Logic Input-High Threshold		ON1, ON2, $\overline{DTRANS}$, $\overline{SKIP1}$, $\overline{SKIP2}$, hysteresis = 225mV		1.2		2.2	V

Note 1: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage has a DC regulation level higher than the error comparator threshold by 50% of the ripple.

Note 2: Operation below 0.5V but above the REFOK threshold is allowed, but the accuracy is not guaranteed.

Note 3: The MAX8775 cannot operate over all combinations of frequency, input voltage (V_{IN}), and output voltage. For large input-to-output differentials and high switching-frequency settings, the required on-time might be too short to maintain the regulation specifications. Under these conditions, a lower operating frequency must be selected. The minimum on-time must be greater than 150ns, regardless of the selected switching frequency. On-time and off-time specifications are measured from the 50% point to the 50% point at the DH_ pin with LX_ = GND, VBST_ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 4: Specifications are guaranteed by design, not production tested.

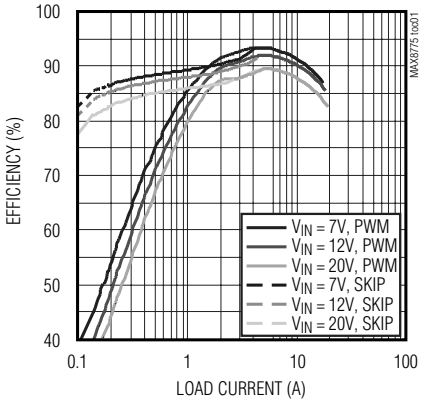
Note 5: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the thin QFN package.

Note 6: Specifications to T_A = -40°C to +85°C are guaranteed by design, not production tested.

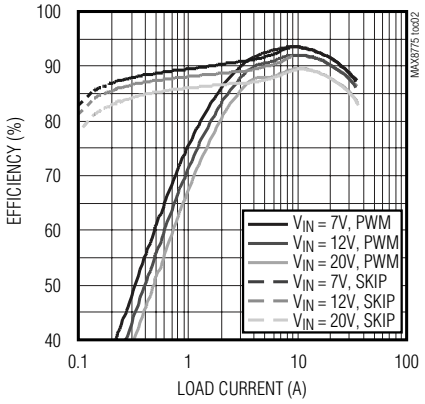
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP\_}$ = GND, T_A = +25°C, unless otherwise noted.)

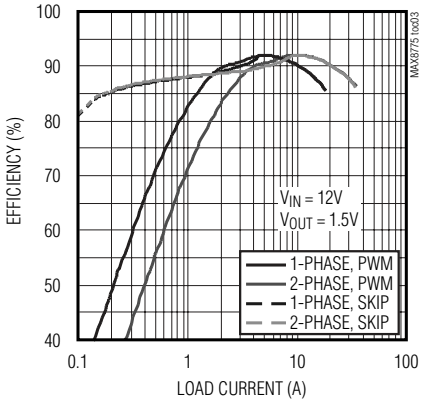
1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.5V)



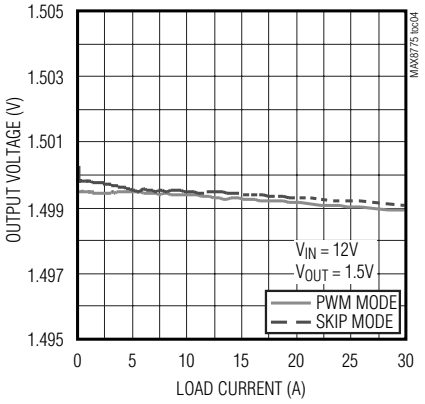
2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.5V)



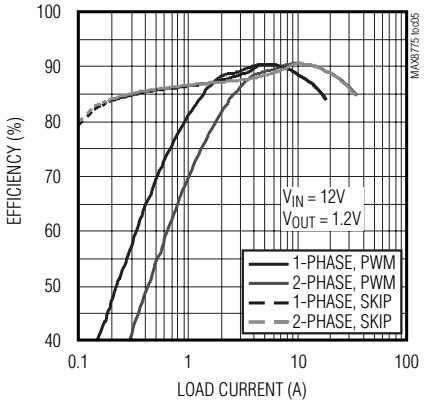
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.5V)



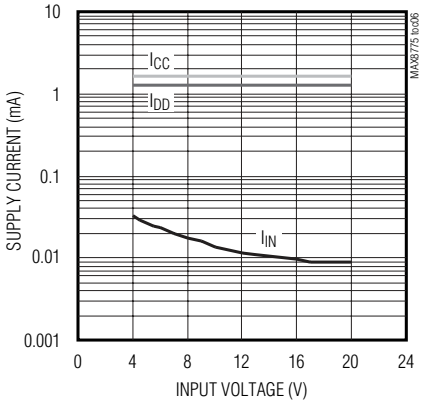
OUTPUT VOLTAGE vs. LOAD CURRENT



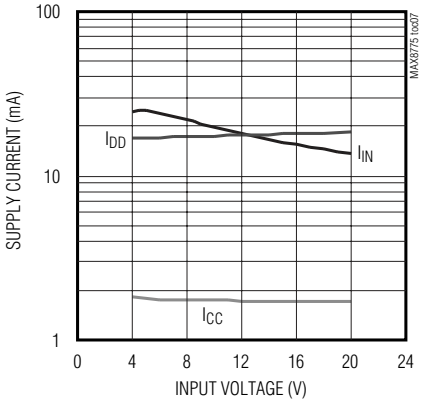
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



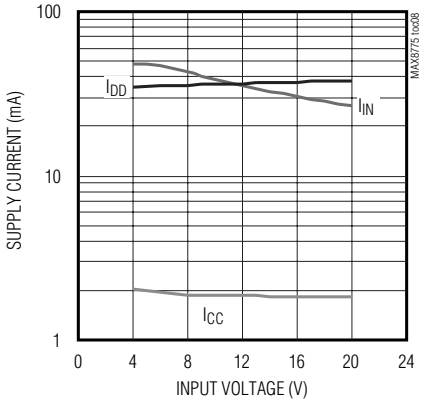
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



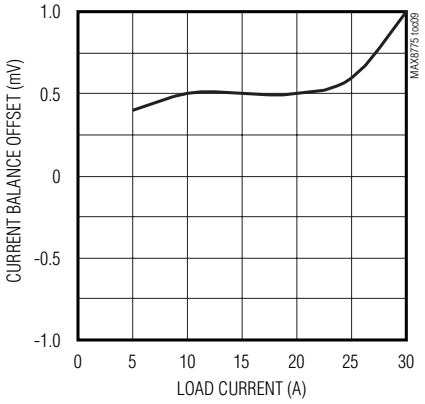
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (1-PHASE PWM MODE)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (2-PHASE PWM MODE)



CURRENT-SENSE OFFSET vs. LOAD CURRENT (2-PHASE PWM MODE)

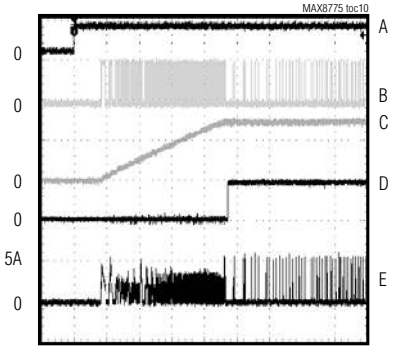


Dual and Combinable Graphics Core Controller for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP\_}$ = GND, T_A = +25°C, unless otherwise noted.)

STARTUP WAVEFORMS

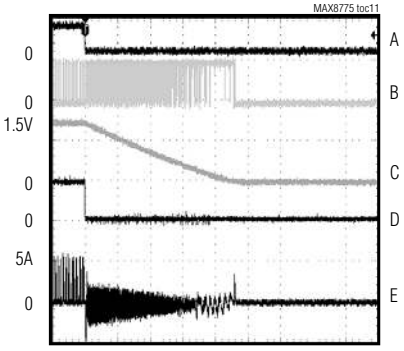


200µs/div

A: ON1, 5V/div
B: DL1, 5V/div
C: V_{OUT1}, 1V/div
D: PGOOD1, 5V/div
E: I_{LX1}, 5A/div

$\overline{SKIP1}$ = GND, R_{LOAD1} = 1Ω, V_{IN} = 12V

SHUTDOWN WAVEFORMS

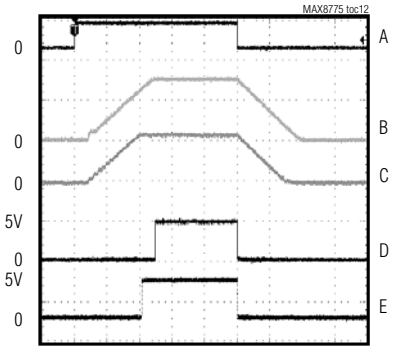


200µs/div

A: ON1, 5V/div
B: DL1, 5V/div
C: V_{OUT1}, 1V/div
D: PGOOD1, 5V/div
E: I_{LX1}, 5A/div

$\overline{SKIP1}$ = GND, R_{LOAD1} = 1Ω, V_{IN} = 12V

STARTUP/SHUTDOWN—SAME SLEW RATE

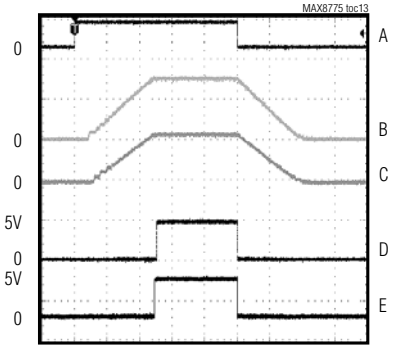


400µs/div

A: ON1, ON2, 5V/div
B: V_{OUT1}, 1V/div
C: V_{OUT2}, 1V/div
D: PGOOD1, 5V/div
E: PGOOD2, 5V/div

C_{SLEW1} = C_{SLEW2} = 470pF
R_{LOAD1} = R_{LOAD2} = 1Ω

STARTUP/SHUTDOWN—SAME START TIME

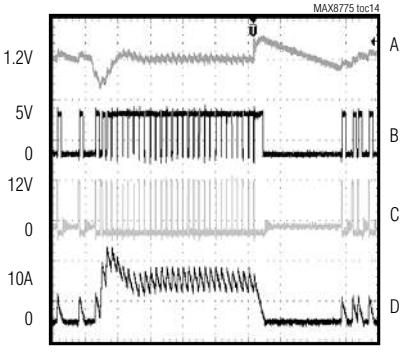


400µs/div

A: ON1, ON2, 5V/div
B: V_{OUT1}, 1V/div
C: V_{OUT2}, 1V/div
D: PGOOD1, 5V/div
E: PGOOD2, 5V/div

C_{SLEW1} = 470pF, C_{SLEW2} = 600pF
R_{LOAD1} = R_{LOAD2} = 1Ω

LOAD TRANSIENT (SEPARATE MODE)

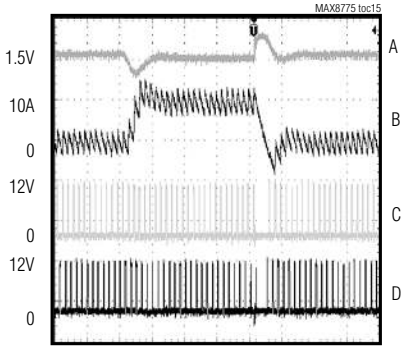


20µs/div

A: V_{OUT1}, 100mV/div
B: DL1, 5V/div
C: LX1, 10V/div
D: I_{LX1}, 10A/div

V_{IN} = 12V, V_{OUT1} = 1.2V
$\overline{SKIP1}$ = GND
I_{OUT1} = 1A TO 11A TO 1A

LOAD TRANSIENT (COMBINED MODE)



20µs/div

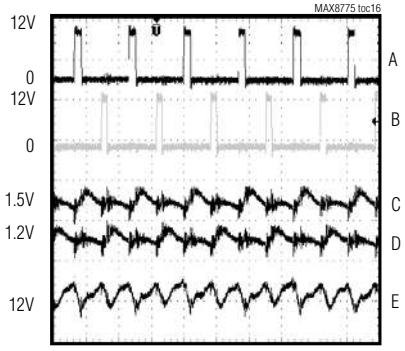
A: V_{OUT1}, 100mV/div
B: I_{LX1}, 10A/div
C: LX1, 10V/div
D: LX2, 10V/div

V_{IN} = 12V, V_{OUT} = 1.5V
I_{OUT1} = 5A TO 25A TO 5A

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP\_}$ = GND, T_A = +25°C, unless otherwise noted.)

SWITCHING WAVEFORMS

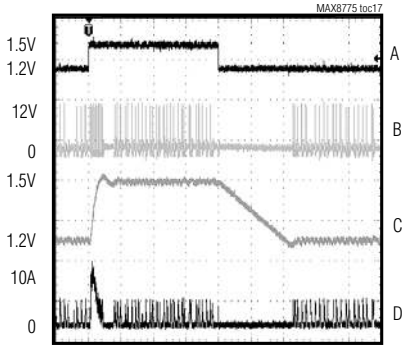


2µs/div

A: LX1, 10V/div
B: LX2, 10V/div
C: V_{OUT1}, 50mV/div
D: V_{OUT2}, 50mV/div
E: V_{IN}, 50mV/div

V_{IN} = 12V, V_{OUT1} = 1.5V, V_{OUT2} = 1.2V
I_{OUT1} = 5A, I_{OUT2} = 5A

REFIN TRANSITION WAVEFORMS ($\overline{DTRANS}$ = V_{CC})

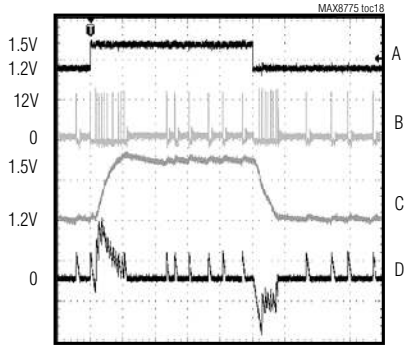


100µs/div

A: REFIN1, 500mV/div
B: LX1, 10A/div
C: V_{OUT1}, 200mV/div
D: I_{LX1}, 10A/div

V_{IN} = 12V, V_{REFIN1} = 1.2V TO 1.5V TO 1.2V
I_{OUT1} = 1A
$\overline{SKIP1}$ = GND

REFIN TRANSITION WAVEFORMS ($\overline{DTRANS}$ = GND)

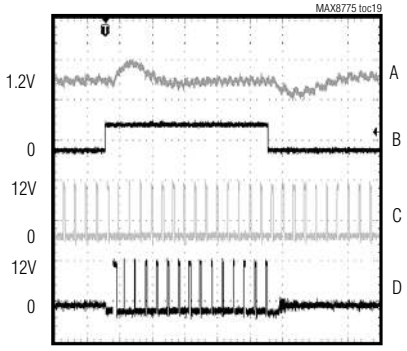


40µs/div

A: REFIN1, 500mV/div
B: LX1, 10A/div
C: V_{OUT1}, 200mV/div
D: I_{LX1}, 10A/div

V_{IN} = 12V, V_{REFIN1} = 1.2V TO 1.5V TO 1.2V
I_{OUT1} = 1A
$\overline{SKIP1}$ = GND

COMBINED-MODE PHASE TRANSITION

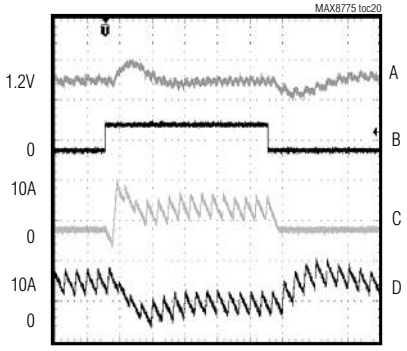


10µs/div

A: V_{OUT}, 50mV/div
B: ON2, 5V/div
C: LX1, 10V/div
D: LX2, 10V/div

V_{IN} = 12V, V_{OUT} = 1.2V
I_{OUT} = 10A

COMBINED-MODE PHASE TRANSITION



10µs/div

A: V_{OUT}, 50mV/div
B: ON2, 5V/div
C: I_{LX2}, 10A/div
D: I_{LX1}, 10A/div

V_{IN} = 12V, V_{OUT} = 1.2V
I_{OUT} = 10A

Dual and Combinable Graphics Core Controller for Notebook Computers

Pin Description

PIN	NAME	FUNCTION
1	OVP1	SMPS1 Overvoltage Adjust Input. The overvoltage trip threshold for SMPS1 is 200mV above the voltage at OVP1. Connect OVP1 to V_{CC} to disable OVP for SMPS1. OVP1 sets the overvoltage threshold for both phases in combined mode.
2	OSC	Oscillator Adjustment Input. Connect a resistor (R_{OSC}) between OSC and AGND to set the switching frequency (per phase): f_{OSC} = 300kHz x 143kΩ / R_{OSC} A 71.5kΩ to 432kΩ corresponds to switching frequencies of 600kHz to 100kHz, respectively. Ensure the minimum on-time requirement is met for the selected frequency.
3	REFIN1	SMPS1 External Reference Input. REFIN1 sets the output regulation voltage (V_{CSL1} = V_{REFIN1}). REFIN1 sets the output regulation voltage in combined mode (V_{CSL1} = V_{CSL2} = V_{REFIN1}).
4	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 10Ω resistor. Bypass V_{CC} to AGND with a 1µF or greater ceramic capacitor.
5	AGND	Analog Ground. Connect backside pad to AGND.
6	REF	2.5V Reference Voltage Output. Bypass REF to AGND with a 0.1µF or greater ceramic capacitor. The maximum value of this cap is 1µF. The reference can source up to 250µA. Loading REF degrades output-voltage accuracy according to the REF load-regulation error (see *Typical Operating Characteristics*). The reference shuts down when both ON1 and ON2 are low.
7	REFIN2	SMPS2 External Reference Input. REFIN2 sets the feedback regulation voltage (V_{CSL2} = V_{REFIN2}). Connect REFIN2 to V_{CC} to select combined mode. See OVP2 pin connection below.
8	OVP2	SMPS2 Overvoltage Adjust Input. The overvoltage trip threshold for SMPS2 is 200mV above the voltage at OVP2. Connect OVP2 to V_{CC} to disable OVP for SMPS2. Connect OVP2 to REF in combined mode when OVP is enabled. Connect OVP2 to V_{CC} in combined mode when OVP is disabled.
9	SLEW2	SMPS2 Slew-Rate Control. Connect a capacitor from SLEW2 to AGND to set the SMPS2 slew rate: Slew Rate (ΔV_{OUT2} / Δt) = I_{SLEW2} / C_{SLEW2} During startup and shutdown, SMPS2 ramps at 1/5 the programmed slew rate. Connect SLEW2 to SLEW1 in combined mode.
10	CCI2	Current-Balance Compensation for SMPS2. When combining SMPS1 and SMP2, connect a 47pF capacitor between CCI2 and AGND. Leave CCI2 open when operating SMPS1 and SMPS2 separately.
11	PGOOD2	SMPS2 Open-Drain Power-Good Output. PGOOD2 is low when SMPS2 is more than 150mV below its regulation threshold, when a 0V fault occurs, during soft-start, and in shutdown. PGOOD2 is the current-balance fault indicator when operating in combined mode.
12	$\overline{SKIP2}$	Low-Noise Mode Control for SMPS2. Connect $\overline{SKIP2}$ to GND for normal Idle Mode (pulse-skipping) operation or to V_{CC} for PWM mode (fixed frequency). $\overline{SKIP2}$ is ignored in combined mode.
13	CSH2	Positive Current-Sense Input for SMPS2. Connect to the positive terminal of the current-sense element. Figure 10 describes two different current-sensing options.
14	CSL2	Negative Current-Sense and Feedback Input for SMPS2. Connect to the negative terminal of the current-sense element. CSL2 regulates to REFIN2. Figure 10 describes two different current-sensing options. CSL2 regulates to REFIN1 in combined mode.
15	ON2	SMPS2 Enable Input. Drive ON2 high to enable SMPS2. Drive ON2 low to shut down SMPS2. When both outputs are combined, ON1 is the master control input to enable/disable the combined output, while ON2 enables/disables phase 2, allowing 1- or 2-phase operation.

Pin Description (continued)

PIN	NAME	FUNCTION
16	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2.
17	BST2	Boost Flying-Capacitor Connection for SMPS2. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST2 allows the DH2 turn-on current to be adjusted.
18	LX2	Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 is the lower supply rail for the DH2 high-side gate driver.
19	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from PGND to V_{DD}.
20	PGND	Power Ground
21	V_{DD}	Supply Voltage Input for the DL_ Gate Drivers. Connect to a 5V supply. Bypass V_{DD} to AGND with a 1µF or greater ceramic capacitor.
22	DL1	Low-Side Gate-Driver Output for SMPS1. DL1 swings from PGND to V_{DD}.
23	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 is the lower supply rail for the DH1 high-side gate driver.
24	BST1	Boost Flying-Capacitor Connection for SMPS1. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST1 allows the DH1 turn-on current to be adjusted.
25	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1.
26	ON1	SMPS1 Enable Input. Drive ON1 high to enable SMPS1. Drive ON1 low to shut down SMPS1. When both outputs are combined, ON1 is the master control signal to enable/disable the combined output, while ON2 enables/disables phase 2, allowing 1- or 2-phase operation.
27	CSL1	Negative Current-Sense and Feedback Input for SMPS1. Connect to the negative terminal of the current-sense element. CSL1 regulates to REFIN1. Figure 10 describes two different current-sensing options.
28	CSH1	Positive Current-Sense Input for SMPS1. Connect to the positive terminal of the current-sense element. Figure 10 describes two different current-sensing options.
29	$\overline{SKIP1}$	Low-Noise Mode Control for SMPS1. Connect $\overline{SKIP1}$ to GND for normal Idle Mode (pulse-skipping) operation or to V_{CC} for PWM mode (fixed frequency). When both outputs are combined, $\overline{SKIP2}$ is ignored and $\overline{SKIP1}$ sets the skip function for both SMPS1 and SMPS2.
30	PGOOD1	SMPS1 Open-Drain Power-Good Output. PGOOD1 is low when SMPS1 is more than 150mV below its regulation threshold, when a 0V fault occurs, during soft-start, and in shutdown. PGOOD1 is the voltage-regulation fault indicator when operating in combined mode.
31	$\overline{DTRANS}$	Forced-Downward Transient Disable Input. Connect $\overline{DTRANS}$ to V_{CC} to disable the forced-downward transition detection feature when operating in pulse-skipping mode, allowing the output to fall at a rate determined by the load current and total output capacitance. Connect $\overline{DTRANS}$ to AGND to enable the forced downward-transition detection feature.
32	SLEW1	SMPS1 Slew-Rate Control. Connect a capacitor from SLEW1 to AGND to set the SMPS1 slew rate: Slew Rate ($\Delta V_{OUT1} / \Delta t$) = I_{SLEW1} / C_{SLEW1} During startup and shutdown, SMPS1 ramps at 1/5 the programmed slew rate. In combined mode, the slew rate is set by both SLEW1 and SLEW2. Connect SLEW1 and SLEW2 together in combined mode: Combined Slew Rate ($\Delta V_{OUT} / \Delta t$) = ($I_{SLEW1} + I_{SLEW2}$) / ($C_{SLEW1} + C_{SLEW2}$)
—	EP	Exposed Backside Pad. Connect the exposed backside pad to AGND.

Dual and Combinable Graphics Core Controller for Notebook Computers

Detailed Description

The MAX8775 is a dual fixed-frequency step-down controller for low-voltage I/O and graphics core (GPU) supplies. It can be configured as two separate regulators generating two independent outputs. Alternatively, the MAX8775 can be configured in combined mode as a two-phase, single-output, high-current regulator, powering the high-performance graphics cores used in game machines and media center notebooks.

The standard applications circuit (Figure 1) generates dynamically adjustable output voltages on both outputs. REFIN voltage setting allows for multiple dynamic

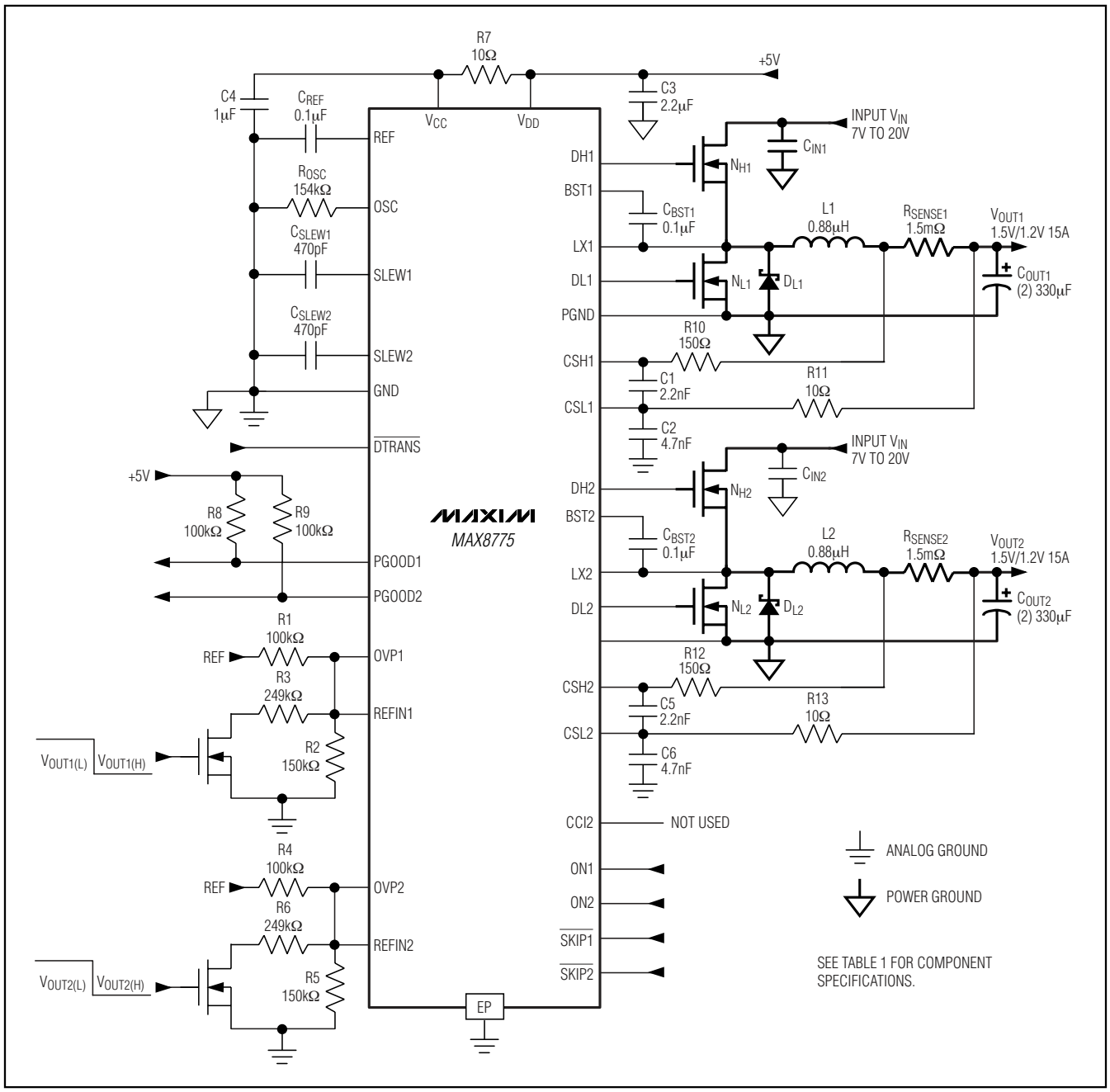


Figure 1. MAX8775 Separate Output Typical Operating Circuit

output voltages required by the different GPU operating and sleep states. Automatic fault blanking, forced-PWM operation, and transition control are achieved by detecting the voltage change at REFIN.

The interleaved, fixed-frequency architecture provides 180° out-of-phase operation to reduce the input capacitance required to meet the RMS input-current ratings. Each controller consists of a multi-input PWM comparator, high-side and low-side gate drivers, fault protection, power-good detection, soft-start, and shutdown logic. Current-mode control allows the use of low-ESR output capacitors.

In combined mode (Figure 2), phase 1 provides the main voltage-control loop while phase 2 maintains the

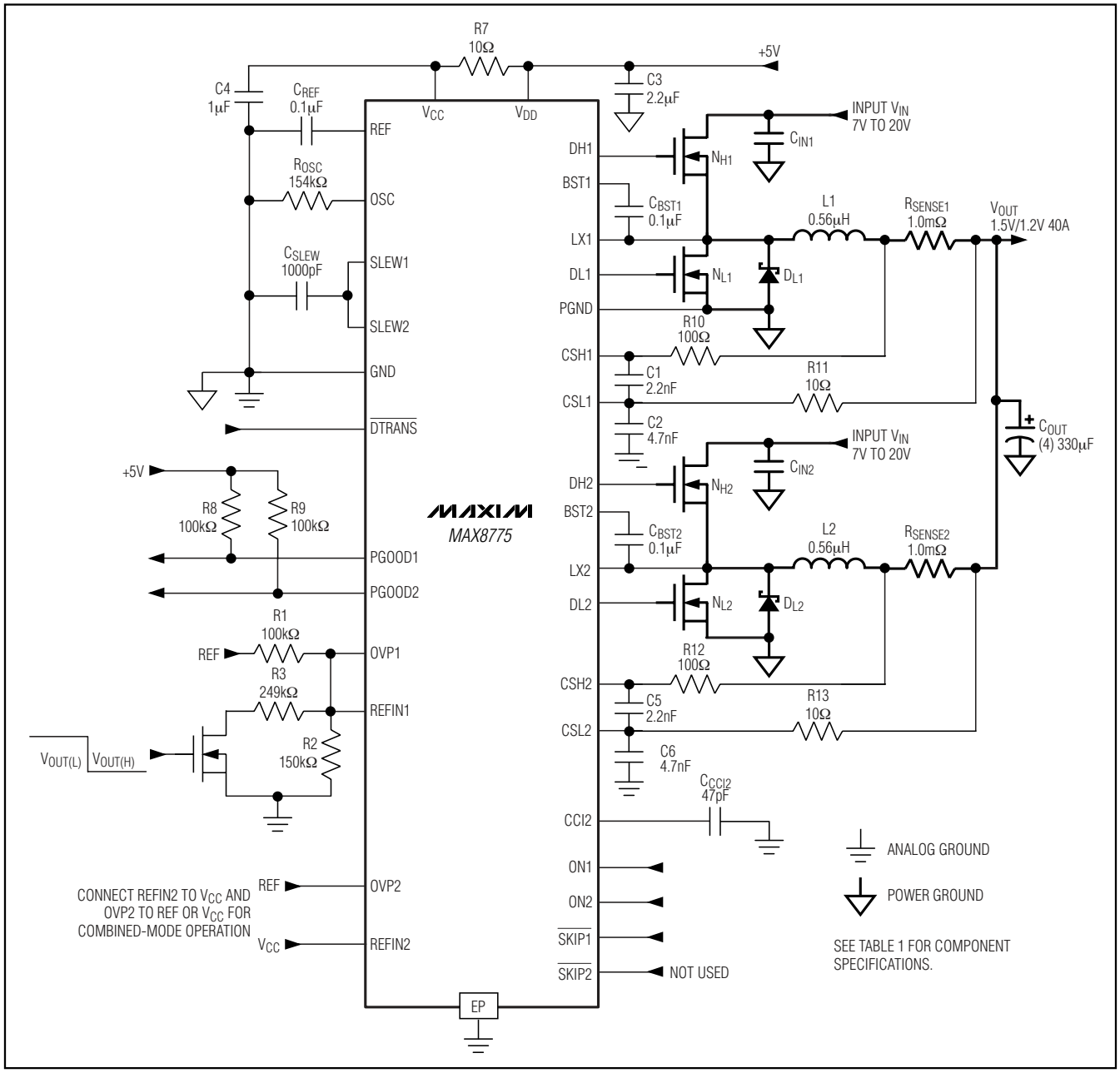


Figure 2. MAX8775 Combined-Output Typical Operating Circuit

Dual and Combinable Graphics Core Controller for Notebook Computers

current balance. PGOOD1 indicates when the combined output is in regulation, while PGOOD2 indicates the currents in both phases are balanced. Phase 2 can be enabled or disabled based on the load current required, maximizing efficiency over the full output current range.

Figure 3 is the MAX8775 functional block diagram.

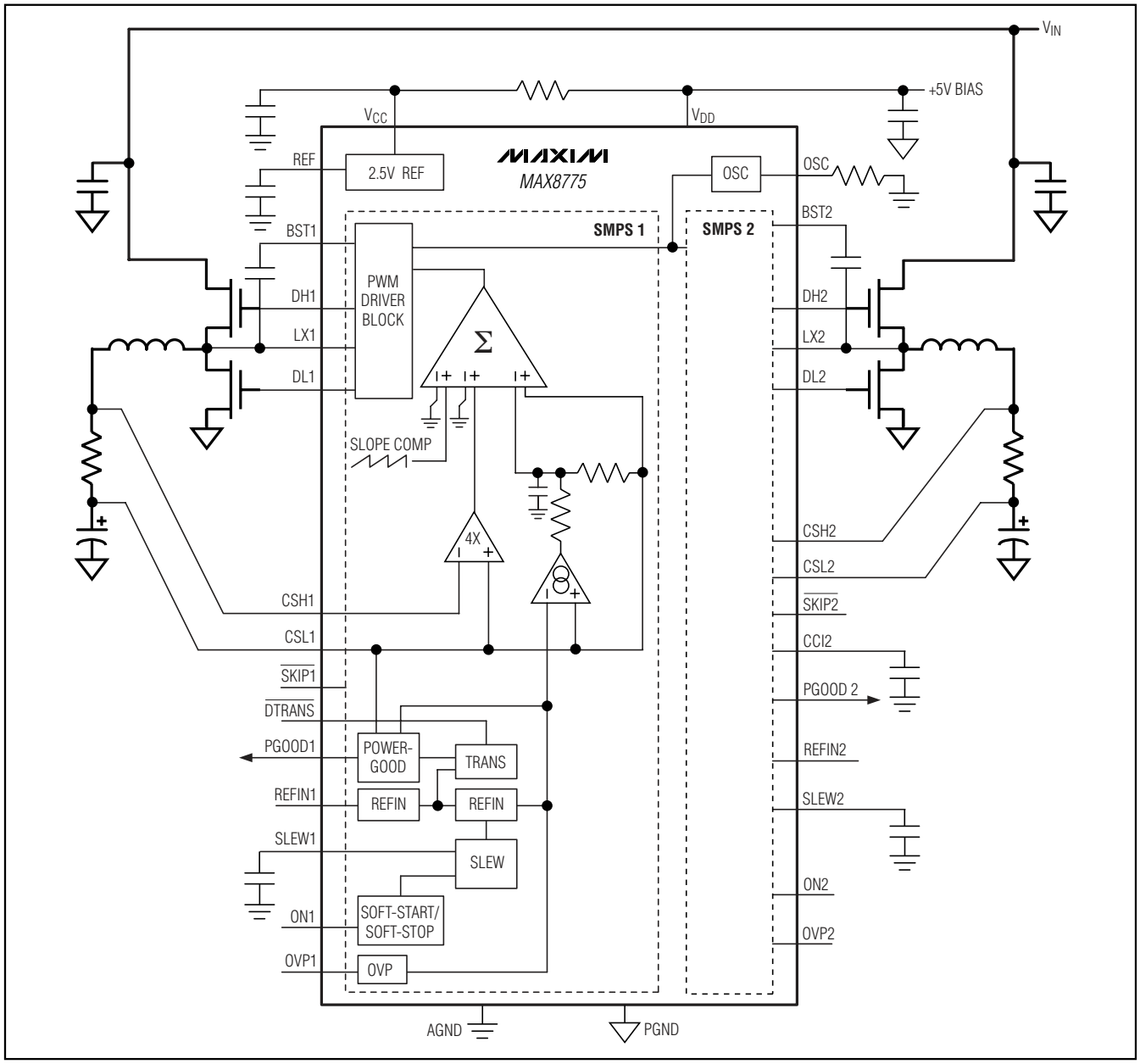


Figure 3. MAX8775 Functional Block Diagram

Table 1. Component Selection for Standard Applications

COMPONENT	V_{IN} = 7V TO 24V V_{OUT1} = 1.0V - 1.5V / 15A	V_{IN} = 7V TO 24V V_{OUT2} = 1.8V / 10A	V_{IN} = 7V TO 24V V_{OUT1} = 1.0V - 1.5V / 40A
MODE	**SEPARATE (FIGURE 1)**	**SEPARATE**	**COMBINED (FIGURE 2)**
Switching Frequency	280kHz	280kHz	280kHz
$C_{IN\_}$, Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(1) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(4) 10µF, 25V Taiyo Yuden TMK432BJ106KM
$C_{OUT\_}$, Output Capacitor	(2) 330µF, 6.3V, 7mΩ, low-ESR capacitor Panasonic EEFSD0D331XR	(1) 330µF, 6.3V, 7mΩ, low-ESR capacitor Panasonic EEFSD0D331XR	(4) 330µF, 6.3V, 7mΩ, low-ESR capacitor Panasonic EEFSD0D331XR
$N_{H\_}$ High-Side MOSFET	(1) Vishay/Siliconix SI7634DP	(1) International Rectifier IRF7811W	(1) Vishay/Siliconix SI7634DP
$N_{L\_}$ Low-Side MOSFET	(1) Vishay/Siliconix SI7336ADP	(1) Vishay/Siliconix SI7336ADP	(2) Vishay/Siliconix SI7336ADP
$D_{L\_}$ Schottky Rectifier	3A, 40V Schottky diode Central Semiconductor CMSH3-40	3A, 40V Schottky diode Central Semiconductor CMSH3-40	3A, 40V Schottky diode Central Semiconductor CMSH3-40
L_ Inductor	0.88µH, 18A, 2.1mΩ NEC/Tokin MPC1040LR88	1.8µH, 13.8A, 6.2mΩ Sumida CDEP105(S)-1R8	0.56_H, 26A, 1.3mΩ NEC/Tokin MPC1040LR56 Panasonic ETQP4LR56WFC
Current-Sense $R_{SENSE\_}$	1.5mΩ, 1W, 2512 Panasonic ERJM1WTJ1M5U	2mΩ, 0.5W, 2010 Vishay WSL20102L000F	1.0mΩ, 1W, 2512 Panasonic ERJM1WTJ1M0U

Table 2. Component Suppliers

SUPPLIER	WEBSITE		SUPPLIER	WEBSITE
AVX	www.avx.com		Panasonic	www.panasonic.com/industrial
Central Semiconductor	www.centralsemi.com		Sanyo	www.secc.co.jp
Coilcraft	www.coilcraft.com		Sumida	www.sumida.com
Coiltronics	www.coiltronics.com		Taiyo Yuden	www.t-yuden.com
Fairchild Semiconductor	www.fairchildsemi.com		TDK	www.component.tdk.com
International Rectifier	www.irf.com		TOKO	www.tokoam.com
Kemet	www.kemet.com		Vishay (Dale, Siliconix)	www.vishay.com

See Table 1 for component selections and Table 2 for the component manufacturers.

SMPS 5V Bias Supply (V_{CC} and V_{DD})

The MAX8775 SMPSs require a 5V bias supply in addition to the high-power input supply (battery or AC adapter). V_{DD} is the power rail for the MOSFET gate drive, and V_{CC} is the power rail for the IC. Connect the external 4.5V to 5.5V supply directly to V_{DD} and connect V_{DD} to V_{CC} through an RC filter, as shown in Figure 1. The maximum supply current required is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(NL1)} + Q_{G1(NH1)} + Q_{G2(NL2)} + Q_{G2(NH2)}) = 1.8mA \text{ to } 40mA$$

where I_{CC} is 1.8mA, f_{SW} is the switching frequency, and $Q_{G\_}$ is the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

Reference (REF)

The 2.5V reference is accurate to ±1% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.1µF or greater ceramic capacitor. The reference sources up to 250µA and sinks 50µA to support external loads.

Dual and Combinable Graphics Core Controller for Notebook Computers

SMPS Detailed Description

SMPS Enable Controls (ON1, ON2)

ON1 and ON2 provide independent control of output soft-start and soft-shutdown. This allows flexible control of startup and shutdown sequencing. The outputs may be started simultaneously, sequentially, or independently. To provide sequential startup, connect ON_ of one regulator to PGOOD_ of the other. For example, with ON1 connected to PGOOD2, OUT1 soft-starts after OUT2 is in regulation. Additionally, tracking and ratiometric startup and shutdown can be achieved using the SLEW_ capacitors. See the *Startup Sequencing* section.

When configured in combined mode (REFIN2 = V_{CC}), ON1 is the master control input that enables/disables the combined output. ON2 enables/disables only the 2nd phase, allowing dynamic switching between one-phase and two-phase operation.

Toggle ON_ low to clear the overvoltage, undervoltage, and thermal-fault latches.

Soft-Start and Soft-Shutdown

Soft-start begins when ON_ is driven high and REF is in regulation. During soft-start, the output is ramped up from 0V to the final set voltage at 1/5 the slew rate programmed by the capacitor at the SLEW_ pin. This reduces inrush current and provides a predictable ramp-up time for power sequencing:

$$\text{Soft-Start/Stop Slew Rate } (\Delta V_{OUT\_} / \Delta t) = I_{SLEWSS\_} / C_{SLEW\_}$$

where $I_{SLEWSS\_}$ is 0.95µA (typ), and $C_{SLEW\_}$ is the capacitor across the SLEW_ pin and AGND. A 470pF capacitor programs a slew rate of approximately 10mV/µs, and a soft-start, soft-shutdown slew rate of approximately 2mV/µs.

Soft-shutdown begins after ON_ goes low, an output undervoltage fault, or a thermal fault. During soft-shutdown, the output is ramped down to 0V at 1/5 the programmed slew rate, reducing negative inductor currents that can cause negative voltages on the output. At the end of soft-shutdown, DL_ is driven high until startup is again triggered by a rising edge of ON_. The reference is turned off when both outputs have been shut down.

When configured in separate mode, the two outputs are independent. A fault at one output does not trigger shutdown of the other.

Startup Sequencing

Individually programmable slew-rate control, on/off control, and power-good outputs allow flexible configuration of the MAX8775 for different power-up sequencing. This is useful in applications where one power rail needs to come up after another, track another rail, or reach regulation at about the same time. Figures 4, 5, and 6 show three configurations for startup sequencing.

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums three signals: the output voltage-error signal with respect to the reference voltage, the current-sense signal, and the slope compensation ramp (Figure 3). The MAX8775 uses a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage

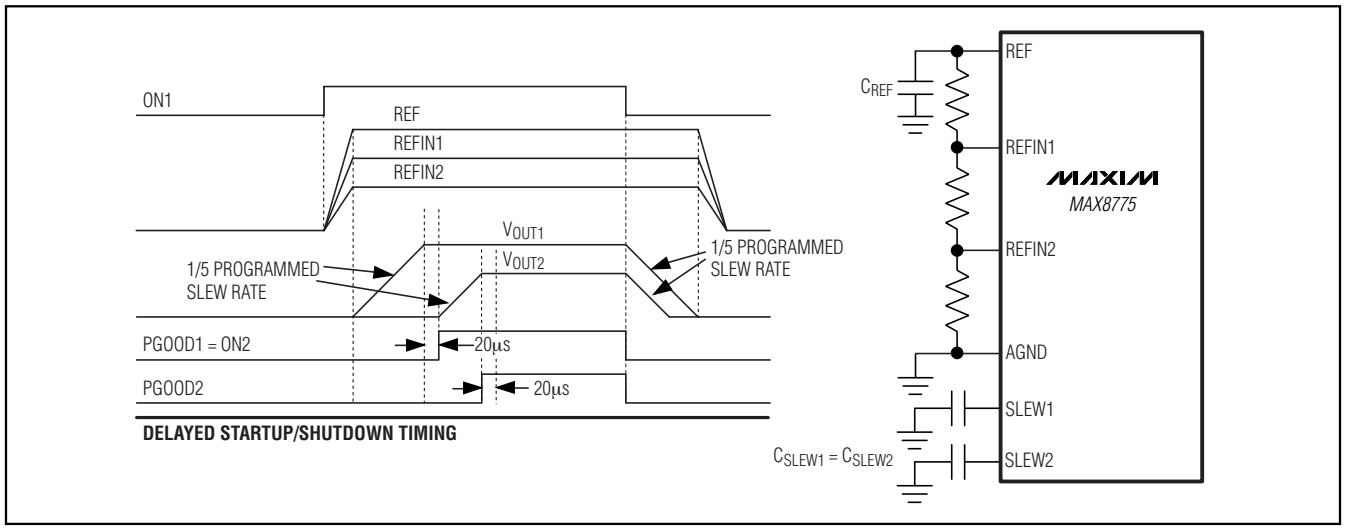


Figure 4. MAX8775 Delayed Startup/Shutdown Timing

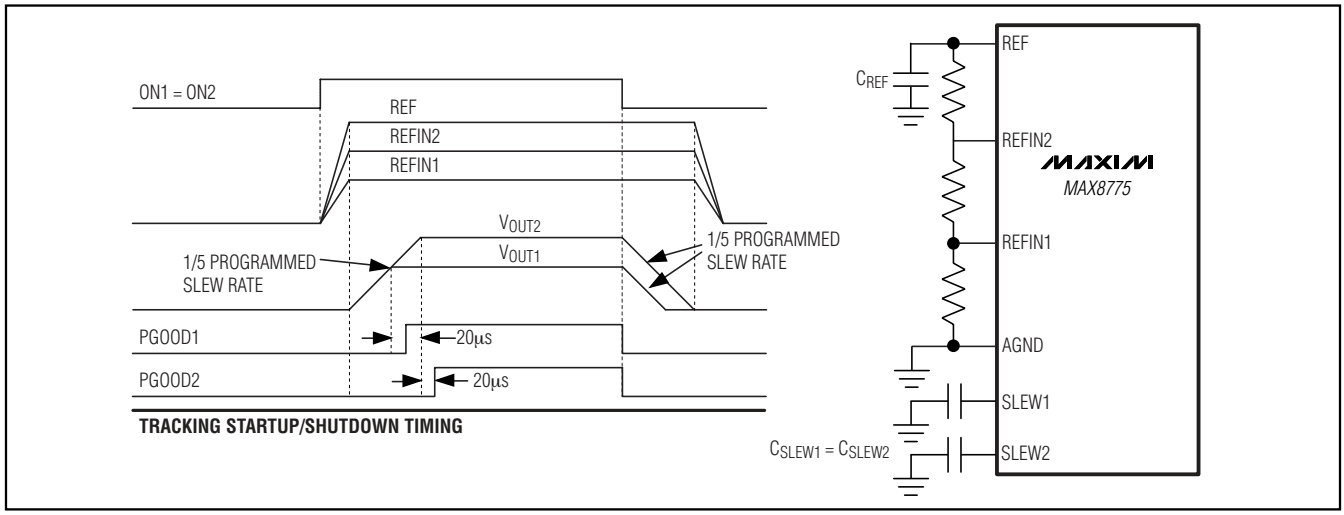


Figure 5. MAX8775 Tracking Startup/Shutdown Timing

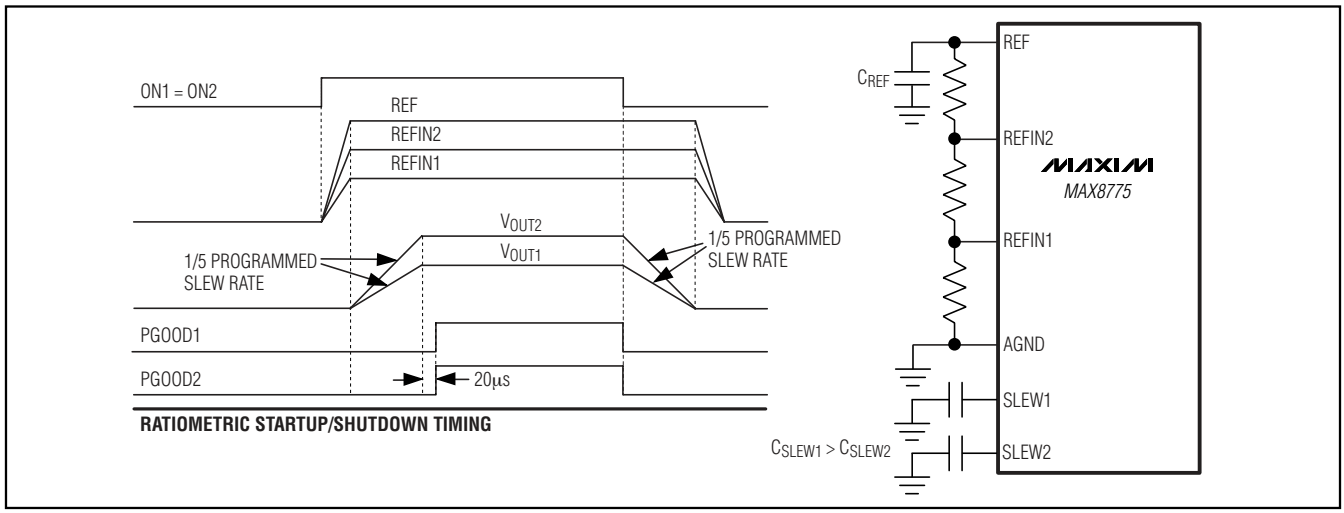


Figure 6. MAX8775 Ratiometric Startup/Shutdown Timing

without a traditional error amplifier and the phase shift associated with it.

The MAX8775 uses a relatively low loop gain, allowing the use of lower cost output capacitors. The relative gain of the voltage comparator to the current comparator is internally fixed at 4:1. The high current gain results in stable operation even with low-output ESR capacitors. An internal integrator corrects for any load-regulation error caused by the high current gain. The low value of loop gain helps reduce output filter capacitor size and cost by shifting the unity-gain crossover frequency to a lower level.

Frequency Selection (FSEL)

The OSC input programs the PWM mode switching frequency. Connect a resistor (R_{OSC}) between OSC and AGND to set the switching frequency (per phase):

$$f_{SW} = 300kHz \times 143k\Omega / R_{OSC}$$

R_{OSC} values between 71.5kΩ and 432kΩ correspond to switching frequencies of 600kHz to 100kHz, respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower. Low-frequency (100kHz) operation offers the best overall efficiency at the expense of component size and board space.

Dual and Combinable Graphics Core Controller for Notebook Computers

When selecting a switching frequency, the minimum on-time at the highest input voltage and lowest output voltage must be greater than the 150ns (max) minimum on-time specification in the *Electrical Characteristics* table:

$$V_{OUT(MIN)} / V_{IN(MAX)} \times T_{SW} > t_{ON(MIN)}$$

A good rule is to choose a minimum on-time of at least 200ns.

When in pulse-skipping operation $\overline{SKIP\_}$ = GND, the minimum on-time must take into consideration the time needed for proper skip-mode operation. The on-time for a skip pulse must be greater than the 150ns (max) minimum on-time specification in the *Electrical Characteristics* table:

$$\frac{L \times V_{IMIN}}{R_{SENSE} \times (V_{IN(MAX)} - V_{OUT(MIN)})} \geq t_{ON(MIN)}$$

Forced-PWM Mode

To maintain low-noise, fixed-frequency operation, drive $\overline{SKIP\_}$ high to put the output into forced-PWM mode. This disables the zero crossing comparator and allows negative inductor current. During forced-PWM mode, the switching frequency remains constant and the no-load supply current is typically between 20mA and 40mA per phase, depending on external MOSFETs and switching frequency.

Light-Load Operation Control ($\overline{SKIP\_}$)

The MAX8775 includes $\overline{SKIP\_}$ inputs, which enable the corresponding outputs to operate in discontinuous mode. Connect $\overline{SKIP\_}$ to GND to enable the zero-crossing comparators of either controller. When the zero-crossing comparator is enabled, the controller forces DL_ low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. During skip mode, the V_{DD} current consumption is reduced and efficiency is improved.

In combined mode, $\overline{SKIP2}$ is unused, and $\overline{SKIP1}$ sets the operating mode for both phases. At very light loads, one-phase and two-phase pulse-skipping operation have about the same efficiency (see the Efficiency vs. Load Current (V_{OUT}=1.5V) graph in *Typical Operating Characteristics*). Keeping the MAX8775 in two-phase skip allows it to dynamically respond to a full-load transient without requiring any system level-control signal to indicate the state of the GPU core.

Idle Mode Current-Sense Threshold

When pulse-skipping mode is enabled, the on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the Idle Mode current-sense threshold. Under light-load conditions, the on-time duration depends solely on the Idle Mode current-sense threshold, which is 20% ($\overline{SKIP\_}$ = GND) of the full load current-limit threshold. This forces the controller to source a minimum amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until the output voltage drops below the feedback threshold. Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses. Therefore, the controller regulates the valley of the output ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 7). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across CSH_ and CSL_. Once $V_{CSH\_}$ - $V_{CSL\_}$ drops below the 3mV zero-crossing, current-sense threshold, the comparator forces DL_ low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical-conduction" point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is determined by:

$$I_{LOAD(SKIP)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2LV_{IN}f_{OSC}}$$

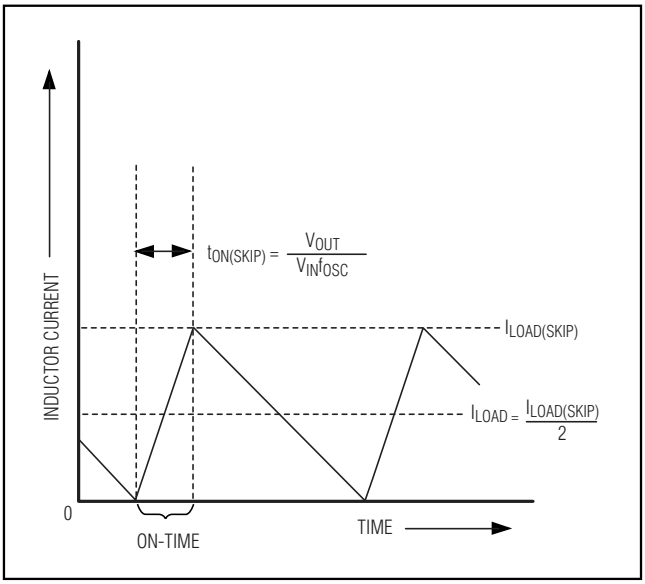


Figure 7. Pulse-Skipping/Discontinuous Crossover Point

In combined-mode operation, since the load is shared between two phases, the load current at which PFM/PWM crossover occurs is twice that of each phase's crossover current.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductance. Generally, low inductance produces a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Output Voltage

The MAX8775 regulates each output to the voltage set at REFIN_ by sensing the CSL_ pin. Changing the voltage at REFIN_ allows the MAX8775 to be used in applications that require dynamic output voltage changes between two or more set points. Figure 1 shows a dynamically adjustable resistive voltage-divider network at REFIN_. Using system control signals to drive the gate(s) of small-signal MOSFETs, resistors can be switched in and out of the REFIN_ resistor-divider, dynamically changing the voltage at REFIN_. The main output voltage is determined by the following equation:

$$V_{OUT(PWM)} = V_{REF}\left(\frac{R_{EQ}}{R_{EQ} + R_{TOP}}\right)$$

where R_{EQ} is the equivalent resistance between REFIN_ and ground, and R_{TOP} is the resistance between REFIN_ and REF (see Figures 1 and 2).

In combined mode (REFIN2 = V_{CC}), REFIN1 sets the voltage of the combined output.

Internal Integrator

The MAX8775 includes an internal transconductance amplifier that integrates the feedback voltage and provides fine adjustment to the regulation voltage, allowing accurate DC output-voltage regulation regardless of the output ripple voltage. When the inductor conducts continuously, the MAX8775 regulates the peak of the output ripple. The internal integrator corrects for errors due to ESR ripple voltage, slope compensation, and current-sense load regulation, maintaining high DC accuracy throughout the full load range, including light-load operation while in pulse-skipping mode.

Dynamic Output Voltages

The MAX8775 controller automatically detects upward transitions of 25mV at REFIN_, enters forced-PWM operation, and blanks the power-good thresholds until 20µs after the output reaches the new regulation target. The MAX8775 slews the output up at a rate set by the slew capacitor $C_{SLEW\_}$:

$$\text{Slew Rate } (\Delta V_{OUT\_} / \Delta t) = I_{SLEW\_} / C_{SLEW\_}$$

where $I_{SLEW\_}$ is 4.75µA (typ), and $C_{SLEW\_}$ is the capacitor across the SLEW_ pin and AGND. A 470pF capacitor programs a slew rate of approximately 10mV/µs.

Setting $\overline{DTRANS}$ low enables the automatic REFIN_ detection downward transitions (Figure 8). This feature is especially useful as it allows the MAX8775 to be set in the high-efficiency, pulse-skipping operation ($\overline{SKIP\_}$ = low), while voltage transitions are automatically taken care of by the MAX8775. Forced downward transitions return the energy from the output capacitors back to the input reservoir.

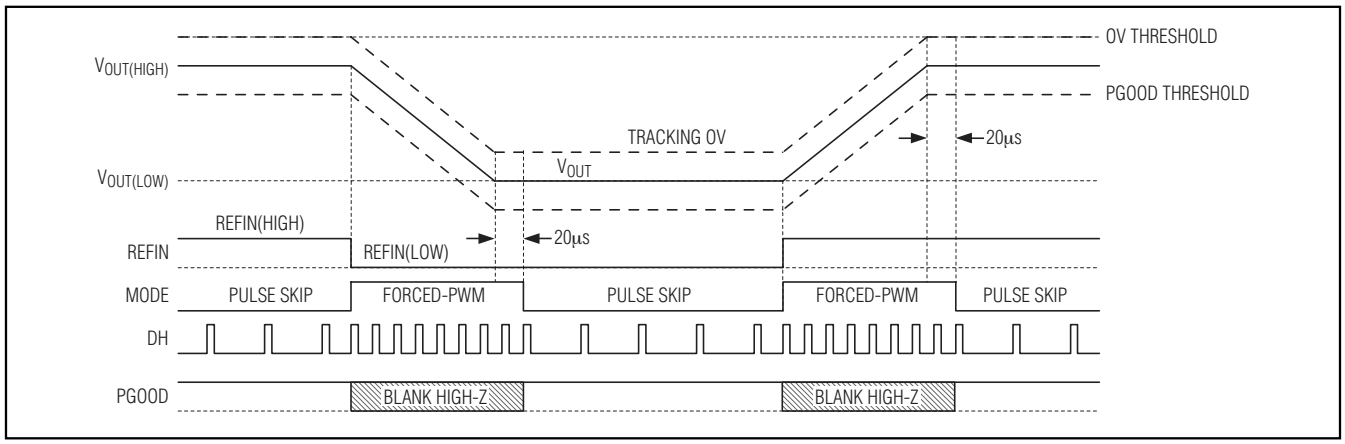


Figure 8. REFIN Transition (Skip Mode, Downward Transition Enabled)

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Setting $\overline{\text{DTRANS}}$ high disables the forced downward REFIN_ transition. This allows the output voltage to drift down at a rate determined by the load current and the total output capacitance (Figure 9). Downward transitions in some systems are less critical from a timing standpoint because the voltage is above the new lower target.

The power consumed in moving the output voltage to the new lower level in a forced manner where the energy is returned to the input with $\overline{\text{DTRANS}}$ low, needs to be weighed against the higher leakage power loss when the voltage drifts down with $\overline{\text{DTRANS}}$ high. Since the efficiency calculations require complex workload duty factors to be taken into consideration, a simple setting of the $\overline{\text{DTRANS}}$ pin allows testing and comparison in both modes to determine which mode offers best efficiency. Table 3 is the $\overline{\text{DTRANS}}$ operating modes truth table.

Combined-Mode Operation

Combined Mode (REFIN2 = V_{CC})

Combined-mode operation allows the MAX8775 to support even higher output currents by sharing the load current between two phases, distributing the power dissipation over several power components. The MAX8775 is configured in combined mode by connecting REFIN2 to V_{CC} and OVP2 to REF or V_{CC}. See Figure 2 for the combined-mode standard application schematic. See the OVP2 connection requirements in the *Pin Description* table.

Phase Transition (ON2)

While in combined mode, ON1 functions as the master control signal that enables/disables the combined output. ON2 enables/disables only phase 2. This allows for flexible power management where phase 2 can be disabled at lighter loads, operating at the most optimal point of the efficiency curve. The MAX8775 does not override the ON2 signal during startup and shutdown. If ON2 is low during startup and shutdown, the MAX8775 operates only in one phase. Since the startup and shutdown slew rates are slow and the load currents are typically low, one-phase operation during startup and shutdown might be possible. Actual system testing and characterization of system load is required to guarantee operation in this mode.

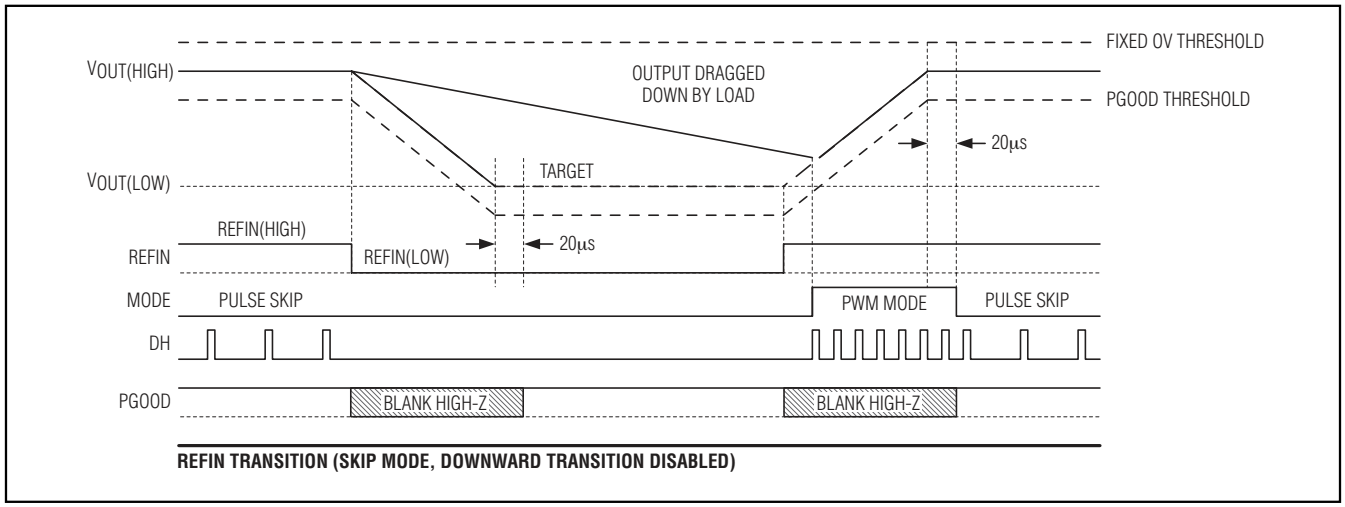

Figure 9. REFIN Transition (Skip Mode, Downward Transition Disabled)

Table 3. $\overline{\text{DTRANS}}$ Operating Modes Truth Table

$\overline{\text{DTRANS}}$	$\overline{\text{SKIP\_}}$	OPERATION DURING TRANSITION
X	H	$\overline{\text{SKIP\_}}$ sets the respective phase in forced-PWM mode. All positive and negative REFIN transitions are forced. PGOOD_ is blanked during the SLEW_ capacitor transition + 20µs.
H	L	$\overline{\text{SKIP\_}}$ sets the respective phase in pulse-skipping mode. Negative REFIN transitions are not forced, and the output voltage is discharged by the load.
L	L	$\overline{\text{SKIP\_}}$ sets the respective phase in pulse-skipping mode. All positive and negative REFIN transitions are forced. PGOOD_ is blanked during the SLEW_ capacitor transition + 20µs.

While ON2 is low, PGOOD2 is blanked high impedance. When ON2 goes high again, the PGOOD2 current-balance comparator is reenabled.

Current Balance (CCI2)

CCI2 is the output of the current-balance transconductance amplifier. The voltage level on CCI2 allows fine adjustment to the duty cycle of phase 2, keeping phase 2's current in balance with phase 1. When V_{CCI2} is 20% above or below V_{REF}, PGOOD2 goes low, indicating the currents in the two phases are not balanced.

Place a 47pF capacitor from CCI2 to AGND to integrate the current balance error. CCI2 is clamped to REF when ON2 is low.

CCI2 is unused in separate mode, and can be left unconnected.

Current-Limit Protection

The current-limit circuit uses differential current-sense inputs (CSH_ and CSL_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller turns off the high-side MOSFET (Figure 3). At the next rising edge of the internal oscillator, the PWM controller does not initiate a new cycle unless the current-sense signal drops below the current-limit threshold. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{IN}).

In forced-PWM mode, the MAX8775 also implements a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately -120% of the positive current limit and tracks the positive current limit.

The current limit is fixed at 30mV (typ).

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH_) source and sink 2A, and the low-side gate drivers (DL_) source 1.7A and sink 3.3A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by charge pumps at BST_ while the DL_ synchronous-rectifier drivers are powered directly by the external 5V supply (V_{DD}).

Adaptive dead-time circuits monitor the DL_ and DH_ drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX8775 interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL_ low is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_ edges, do not pull up the low-side MOSFETs' gate, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFETs' gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Adding a resistor less than 10Ω in series with BST_ might remedy the problem by increasing the turn-on time of the high-side MOSFET without degrading the turn-off time.

Power-Good Output (PGOOD_)

PGOOD_ is the open-drain output of a comparator that continuously monitors each SMPS output voltage for overvoltage and undervoltage conditions. PGOOD_ is actively held low in shutdown (ON_ = GND), soft-start, and soft-shutdown. Once the soft-start terminates, PGOOD_ becomes high impedance as long as the output does not drop below 150mV from the nominal regulation voltage set by REFIN_. PGOOD_ goes low once the output drops 150mV below its nominal regulation point, an output overvoltage fault occurs, or ON_ is pulled low. For a logic-level PGOOD_ output voltage, connect an external pullup resistor between PGOOD_ and +5V or +3.3V. A 100kΩ pullup resistor works well in most applications.

PGOOD_ is blanked high impedance during all transitions detected at REFIN_ until 20µs after the output reaches the regulation voltage.

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In combined mode (REFIN2 = V_{CC}), PGOOD1 indicates the output voltage is in regulation, while PGOOD2 indicates the currents between the two phases are in balance. PGOOD2 is the output of a comparator that monitors the voltage difference between CCI2 and REF. Since CCI2 is the output of a transconductance amplifier, even small current imbalance over a long time causes CCI2 to go high or low, depending on the current imbalance. Whenever CCI2 is 20% above or below REF (CCI2 ≥ 3V or CCI2 ≤ 2V), PGOOD2 goes low, indicating the currents in the two phases are not balanced. PGOOD2 is blanked high impedance during all transitions detected at REFIN_ until 20µs after the output reaches the regulation voltage.

Fault Protection

Output Overvoltage Protection

The MAX8775 includes an OVP_ pin that allows flexible setting of the overvoltage fault threshold. The overvoltage threshold is 200mV (typ) above the voltage at the OVP_ pin. This simplifies the configuration, allowing the OVP_ pin to be directly connected to REFIN_, eliminating the need for extra resistors to set the overvoltage level.

If the output voltage of either SMPS rises 200mV above its nominal regulation voltage, the corresponding controller sets its overvoltage fault latch, pulls PGOOD_ low, and forces DL_ high for the faulted side. The other controller is not affected. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse blows. Cycle V_{CC} below 1V or toggle both ON_ pins to clear the overvoltage fault latch and restart the SMPS controller.

In combined mode (REFIN2 = V_{CC}), OVP1 sets the overvoltage fault threshold for the combined output, while OVP2 is connected to REF when OVP is enabled, and to V_{CC} when OVP is disabled.

Output Undervoltage Protection

If the output voltage of either SMPS falls 300mV below its regulation voltage, the corresponding controller sets its undervoltage fault latch, pulls PGOOD_ low, and begins soft-shutdown for the faulted side by pulsing DL_. DH_ remains off during the soft-shutdown sequence initiated by an undervoltage fault. The other controller is not affected. After soft-shutdown has completed, the MAX8775 forces DL_ high and DH_ low. Cycle V_{CC} below 1V or toggle ON_ to clear the undervoltage fault latch and restart the SMPS controller.

V_{CC} POR and UVLO

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the PWM for operation. V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching, forces PGOOD_ low, and forces the DL_ gate drivers low.

If V_{CC} drops low enough to trip the UVLO comparator while ON_ is high, the MAX8775 immediately forces DH_ and DL_ low on both controllers. The output discharges to 0V at a rate dependent on the load and the total output capacitance. This prevents negative output voltages, eliminating the need for a Schottky diode to GND at the output.

Table 4. Operating Modes Truth Table

MODE	CONDITION	DESCRIPTION
Power-Up	V_{CC} UVLO	When ON_ is high, DL_ is forced low as V_{CC} falls below the 3.95V (typ) falling UVLO threshold. DL_ is forced high when V_{CC} falls below 1V (typ).
Run	ON1 or ON2 enabled	Normal operation.
Output Overvoltage Protection (OVP)	Either output > 200mV above nominal level	When the overvoltage comparator trips, the faulted side sets the OV latch, forcing PGOOD_ low and DL_ high. An OV fault on one SMPS does not affect the operation of the other SMPS. The OV latch is cleared by cycling V_{CC} below 1V or cycling both ON_ pins.
Output Undervoltage Protection (UVP)	Either output < 300mV below nominal level, UVP is enabled 6144 clock cycles ($1/f_{OSC}$) after the output is enabled (ON_ going high)	When the undervoltage comparator trips, the faulted side sets the UV latch, forcing PGOOD_ low and initiating the soft-shutdown sequence by pulsing only DL_. DL_ goes low after soft-shutdown. A UV fault on one SMPS does not affect the operation of the other SMPS. The UV latch is cleared by cycling V_{CC} below 1V or cycling the respective ON_ pin.
Shutdown	ON1 and ON2 are driven low	DL_ stays low after soft-shutdown is completed. All circuitry is shut down.
Thermal Shutdown	T_J > +160°C	Exited by POR or cycling ON1 and ON2. DL1 and DL2 remain low.

Thermal-Fault Protection

The MAX8775 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latches, pulls PGOOD_ low, and shuts down both SMPS controllers using the soft-shutdown sequence (see the *Soft-Start and Soft-Shutdown* section). Cycle V_{CC} below 1V or toggle ON1 and ON2 to clear the fault latches and restart the controllers after the junction temperature cools by 15°C.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point.** This choice provides trade-offs between size and efficiency and between transient response and output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 30% ripple current. When pulse skipping ($\overline{SKIP\_}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The per-phase switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{OSC} I_{LOAD(MAX)} LIR}$$

For example: $I_{LOAD(MAX)}$ = 15A, V_{IN} = 12V, V_{OUT} = 1.5V, f_{OSC} = 300kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{1.8V \times (12V - 1.8V)}{12V \times 300kHz \times 15A \times 0.3} = 0.97\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{OSC} L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output voltage sag is the sum of the voltage sag while the inductor is ramping up, and the voltage sag before the next pulse can occur:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}(V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(T - \Delta T)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor (see the *Electrical Characteristics*), T is the switching period (1 / f_{OSC}), and ΔT equals V_{OUT} / V_{IN} x T when in PWM mode, or L x 0.2 x I_{MAX} / (V_{IN} - V_{OUT}) when in skip

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mode. The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2 N_{PH} C_{OUT} V_{OUT}}$$

where N_{PH} is 2 in combined mode when both phases are active.

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The per-phase peak inductor current occurs at $I_{LOAD(MAX)}$ plus half the ripple current; therefore:

$$I_{LIMIT} > \frac{I_{LOAD(MAX)}}{N_{PH}} + \left(\frac{\Delta I_{INDUCTOR}}{2} \right)$$

where N_{PH} is 2 in combined mode, and I_{LIMIT} equals the minimum current-limit threshold voltage divided by the current-sense resistance ($R_{SENSE\_}$). For the 30mV default setting, the minimum current-limit threshold is 26mV.

The current-sense method (Figure 10) and magnitude determine the achievable current-limit accuracy and power loss. The sense resistor can be determined by:

$$R_{SENSE\_} = V_{LIM\_} / I_{LIMIT\_}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 10a. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. However, the parasitic inductance of the current-sense resistor can cause current-limit inaccuracies, especially when using low-value inductors and current-sense resistors. This parasitic inductance (L_{ESL}) can be cancelled by adding an RC circuit across the sense resistor with an equivalent time constant:

$$C_{EQ} R_{EQ} = \frac{L_{ESL}}{R_{SENSE}}$$

Alternatively, low-cost applications that do not require highly accurate current-limit protection may reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 10b) with an equivalent time constant:

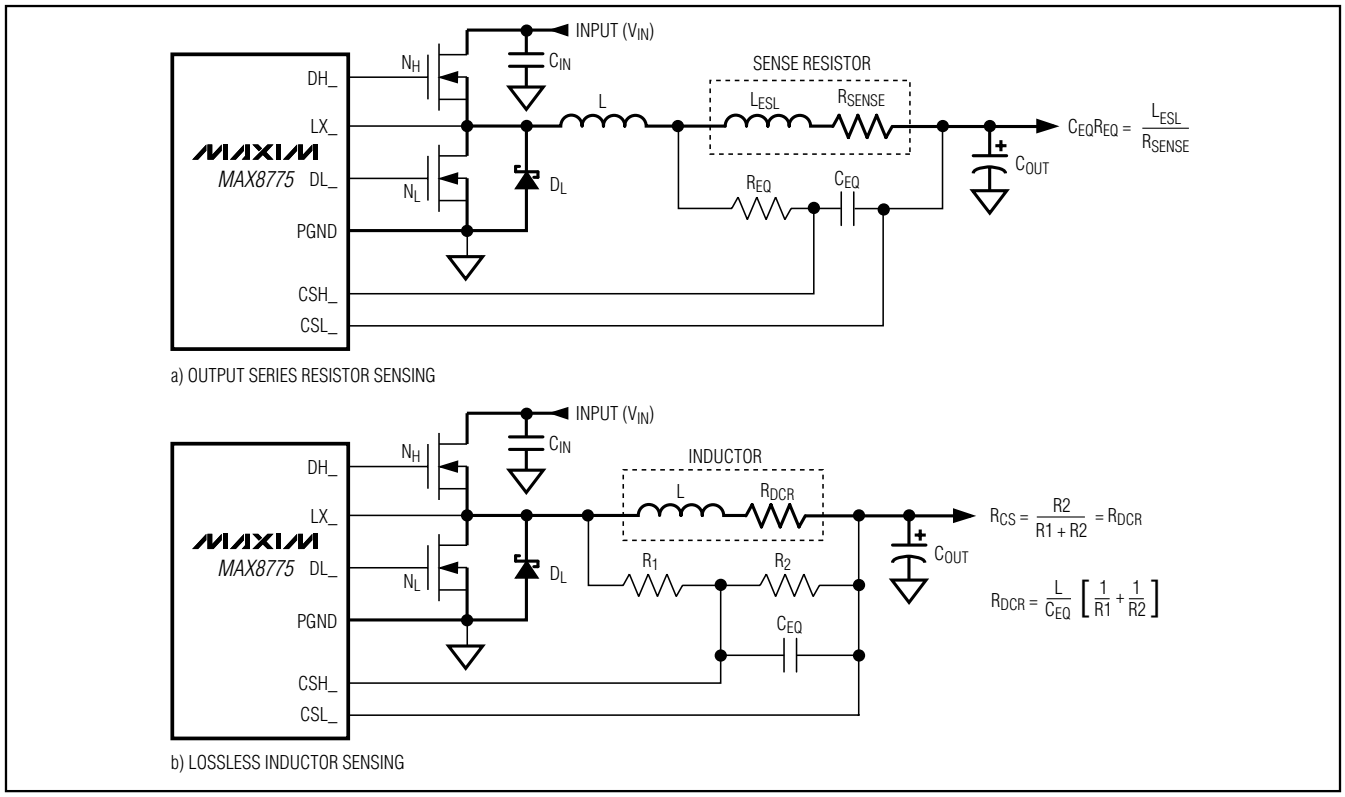

Figure 10. Current-Sense Configurations

$$R_{CS} = \frac{R2}{R1+R2} R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}} \times \left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors (see stability requirements), the filter capacitor's ESR dominates the output voltage ripple. Therefore, the output capacitor's size depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = R_{ESR} I_{LOAD(MAX)} LIR$$

In Idle Mode, the inductor current becomes discontinuous, with peak currents set by the Idle Mode current-sense threshold ($V_{IDLE} = 0.2V_{LIMIT}$). In Idle Mode, the no-load output ripple can be determined as follows:

$$V_{RIPPLE(P-P)} = \frac{V_{IDLE} R_{ESR}}{R_{SENSE}}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics). When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high ESR zeros that may affect the overall stability (see the *Output Capacitor Stability Considerations* section).

Output Capacitor Stability Considerations

Stability is determined by the value of the output zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$R_{ESR} < 2R_{SENSE} \text{ and } f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{(2\pi R_{ESR} + 4R_{SENSE})C_{OUT}}$$

For a typical 300kHz application, the output zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support $25mV_{P-P}$ ripple is 25mV/1.5A = 16.7mΩ. One 330µF/2.5V Sanyo polymer (TPE) capacitor provides 7mΩ (max) ESR. Together with the 1.5mΩ current-sense resistors, the output zero is 25kHz, zero is 25kHz, well within the bounds of stability.

The MAX8775 is optimized for low-duty-cycle operations. Steady-state operation at 45% duty cycle or higher is not recommended.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the RMS ripple current requirement (I_{RMS}) imposed by the switching currents. For a single step-down converter, the RMS input ripple current is defined by the output load current (I_{OUT}), input voltage, and output voltage, with the worst-case condition occurring at $V_{IN} = 2V_{OUT}$:

$$I_{RMS} = I_{OUT} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

For a dual +180° interleaved controller, the out-of-phase operation reduces the RMS input ripple current, effectively lowering the input capacitance requirements. When both outputs operate with a duty cycle less than 50% ($V_{IN} > 2V_{OUT}$), the RMS input ripple current is defined by the following equation:

$$I_{RMS} = \sqrt{\left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1}(I_{OUT1} - I_{IN}) + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}(I_{OUT2} - I_{IN})}$$

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where I_{IN} is the average input current:

$$I_{IN} = \left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1} + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}$$

In combined mode (REFIN2 = V_{CC}) with both phases active, the input RMS current simplifies to:

$$I_{RMS} = I_{OUT} \sqrt{\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{2} - \frac{V_{OUT}}{V_{IN}}\right)}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. Choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, optimum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX8775 DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power-MOSFET Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD\ (N_H\ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ Switching) = \left(\frac{V_{IN(MAX)} I_{LOAD} f_{SW}}{I_{GATE}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN(MAX)}^2 f_{SW}}{2}$$

where C_{RSS} is the reverse transfer capacitance of N_H, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\ (N_L\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$, but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT} - \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

where I_{LIMIT} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{Q_{GATE}}{200mV}$$

where Q_{GATE} is the total gate charge specified in the high-side MOSFETs' data sheet. For example, assume the SI7634DP n-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single SI7634DP has a gate charge of 21nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{13nC}{200mV} = 0.105\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by the maximum duty-cycle specification (see the *Electrical Characteristics* table). However, keep in mind that the transient performance gets worse as the step-down regulators approach the dropout voltage, so bulk output capacitance must be added (see the voltage sag and soar equations in the *Design Procedure* section). The absolute point of dropout occurs when the inductor current ramps down during the off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). This results in a minimum operating voltage defined by the following equation:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + h\left(\frac{1}{D_{MAX}} - 1\right)\left(V_{OUT} + V_{DIS}\right)$$

where V_{CHG} and V_{DIS} are the parasitic voltage drops in the charge and discharge paths, respectively. A reasonable minimum value for h is 1.5, while the absolute minimum input voltage is calculated with h = 1.

Maximum Input Voltage

The MAX8775 controller includes a minimum on-time specification, which determines the maximum input operating voltage that maintains the selected switching frequency (see the *Electrical Characteristics* table). Operation above this maximum input voltage results in pulse-skipping operation, regardless of the operating mode selected by $\overline{SKIP\_}$. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse, effectively skipping a cycle. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{OSC}t_{ON(MIN)}}\right)$$

where f_{OSC} is the switching frequency selected by OSC.

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 11). If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters,

where a single mΩ of excess trace resistance causes a measurable efficiency penalty.

- Minimize current-sensing errors by connecting CSH_ and CSL_ directly across the current-sense resistor ($R_{SENSE\_}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, REFIN_, CSH_, CSL_).

Layout Procedure

1) Place the power components first, with ground terminals adjacent ($N_{L\_}$ source, C_{IN}, $C_{OUT\_}$, and $D_{L\_}$ anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite $N_{L\_}$ and $N_{H\_}$ to keep LX_, GND, DH_, and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
3) Group the gate-drive components (BST_ capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figures 1, 2, and 11. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

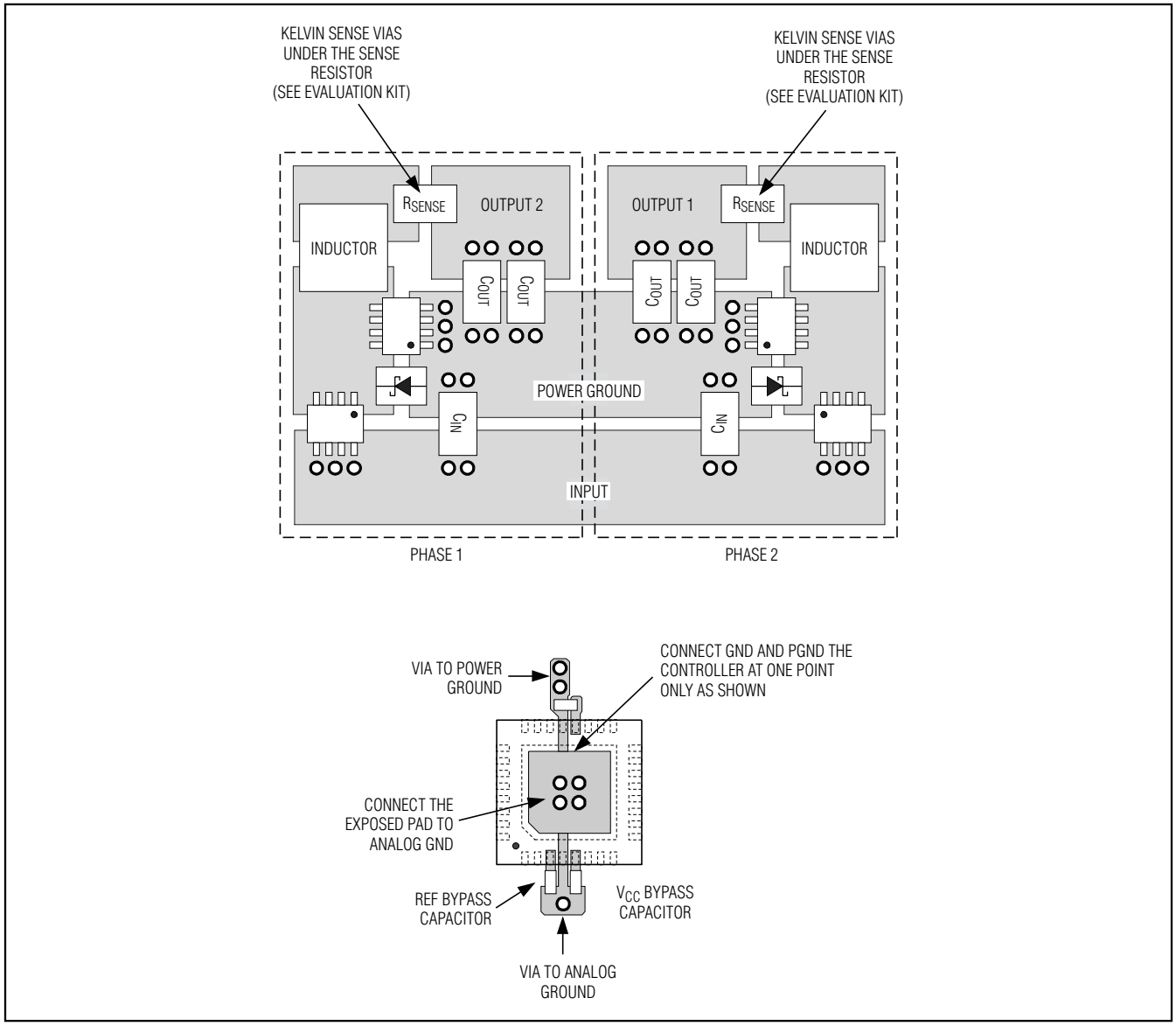


Figure 11. PCB Layout

Chip Information

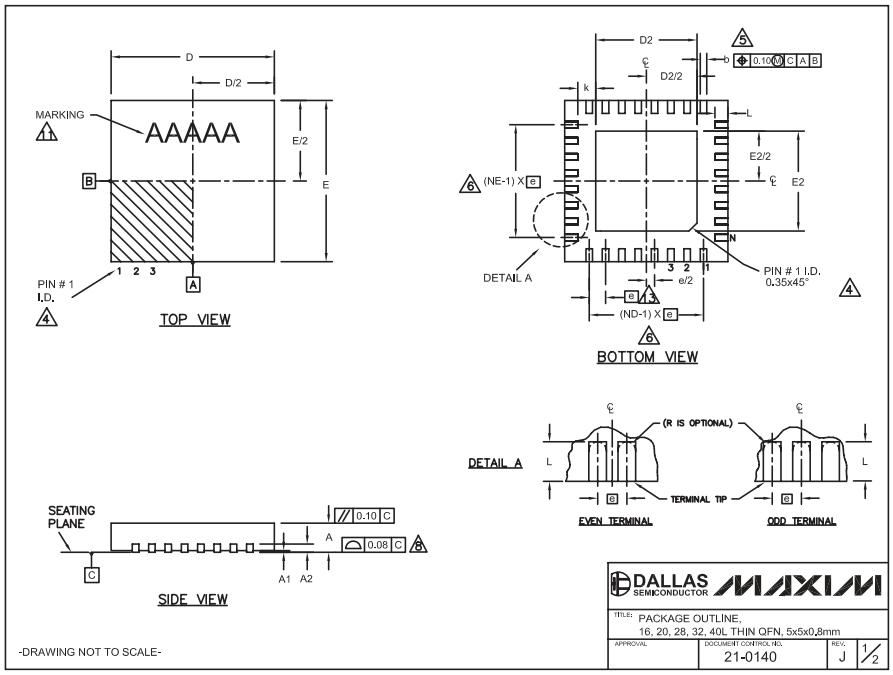
TRANSISTOR COUNT: 6372

PROCESS: BiCMOS

Dual and Combinable Graphics Core Controller for Notebook Computers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140
J
2/2