

# DATA SHEET

## **74ABT2245**

Octal transceiver with direction pin and  
30  $\Omega$  series termination resistors (3-State)

Product data  
Supersedes data of 1998 Jan 16

2002 Dec 17

# Octal transceiver with direction pin and 30 $\Omega$ series termination resistors (3-State)

## 74ABT2245

### FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +12 mA / -32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted
- Same as 74ABT245-1
- Outputs include series resistance of 30  $\Omega$ , making external termination resistors unnecessary
- Inputs are disabled during 3-State mode

### DESCRIPTION

The 74ABT2245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT2245 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ( $\overline{OE}$ ) input for easy cascading and a Direction (DIR) input for direction control.

The 74ABT2245 is designed with 30  $\Omega$  series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

The 74ABT2245 is the same as the 74ABT245-1. The part number has been changed to reflect industry standards.

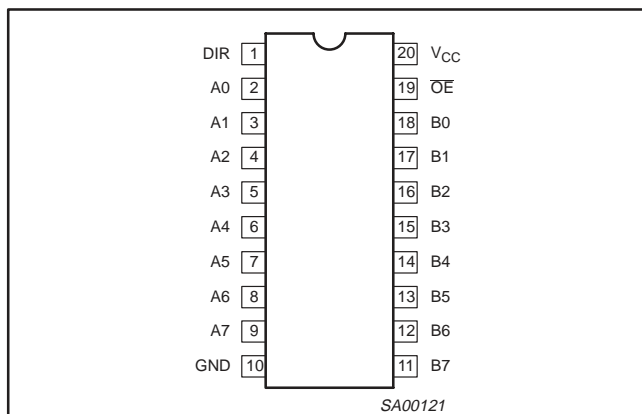
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; GND = 0 V	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$ ; $V_{CC} = 5\text{ V}$	3.9	ns
$C_{IN}$	Input capacitance DIR, $\overline{OE}$	$V_I = 0\text{ V}$ or $V_{CC}$	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_O = 0\text{ V}$ or $V_{CC}$	7	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	50	$\mu\text{A}$

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
20-Pin plastic SO	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT2245D	SOT163-1
20-Pin Plastic SSOP Type II	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT2245DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT2245PW	SOT360-1

### PIN CONFIGURATION



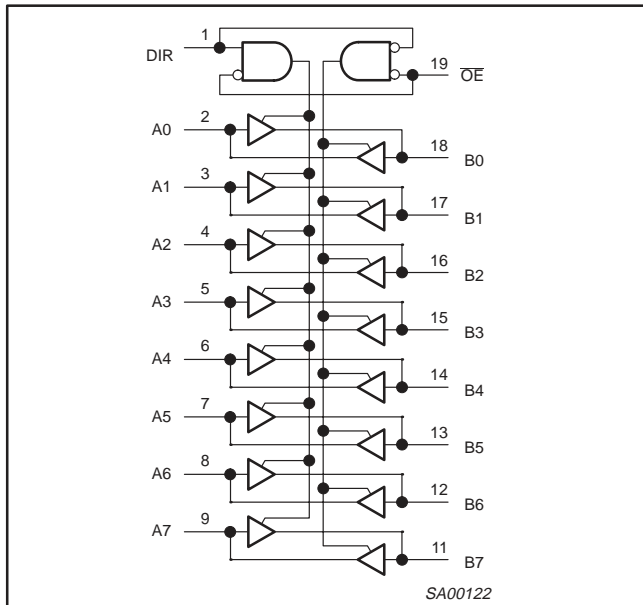
### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active-LOW)
10	GND	Ground (0 V)
20	$V_{CC}$	Positive supply voltage

# Octal transceiver with direction pin and 30 Ω series termination resistors (3-State)

74ABT2245

## LOGIC SYMBOL

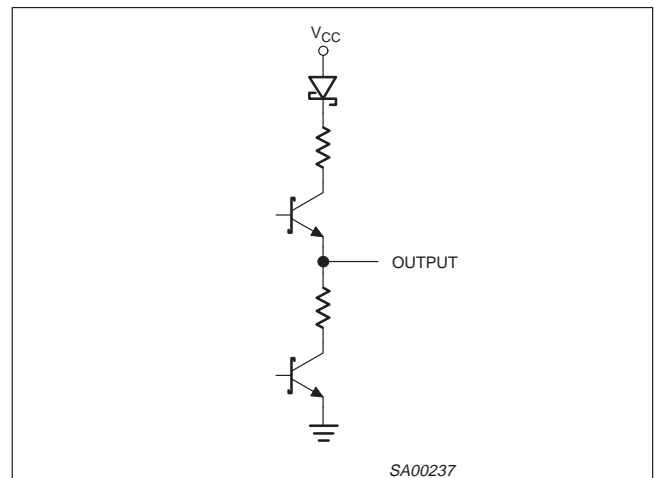


## FUNCTION TABLE

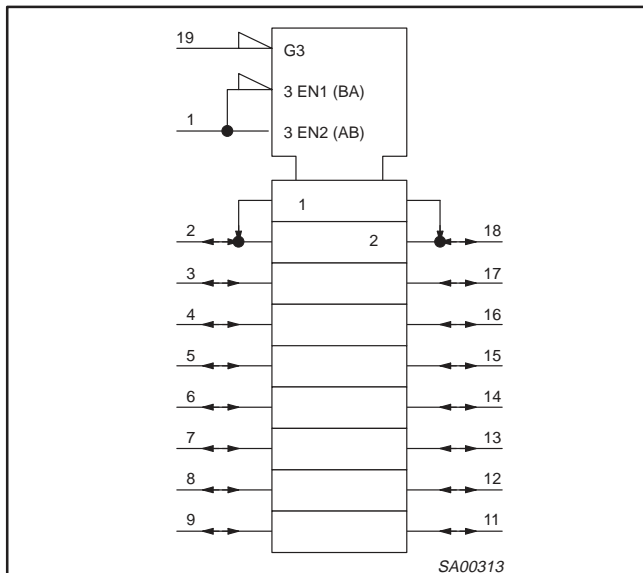
INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state

## SCHEMATIC OF EACH OUTPUT



## LOGIC SYMBOL IEEE/IEC



# Octal transceiver with direction pin and 30 $\Omega$ series termination resistors (3-State)

74ABT2245

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$ V	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$ V	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or HIGH state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in LOW state	128	mA
$T_{stg}$	Storage temperature range		-65 to 150	$^{\circ}$ C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150  $^{\circ}$ C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage	2.0	-	V
$V_{IL}$	LOW-level Input voltage	-	0.8	V
$I_{OH}$	HIGH-level output current	-	-32	mA
$I_{OL}$	LOW-level output current	-	12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	$^{\circ}$ C

# Octal transceiver with direction pin and 30 $\Omega$ series termination resistors (3-State)

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		
			Min	Typ	Max	Min	Max	
$V_{IK}$	Input clamp voltage	$V_{CC} = 4.5\text{ V}$ ; $I_{IK} = -18\text{ mA}$	–	–0.9	–1.2	–	–1.2	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 4.5\text{ V}$ ; $I_{OH} = -3\text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	2.5	2.9	–	2.5	–	V
		$V_{CC} = 5.0\text{ V}$ ; $I_{OH} = -3\text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	3.0	3.4	–	3.0	–	V
		$V_{CC} = 4.5\text{ V}$ ; $I_{OH} = -32\text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	2.0	2.4	–	2.0	–	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5\text{ V}$ ; $I_{OL} = 5\text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	–	0.32	0.55	–	0.55	V
		$V_{CC} = 4.5\text{ V}$ ; $I_{OL} = 12\text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	–	0.5	0.8	–	0.8	V
$I_I$	Input leakage current	Control pins $V_{CC} = 5.5\text{ V}$ ; $V_I = \text{GND}$ or $5.5\text{ V}$	–	$\pm 0.01$	$\pm 1.0$	–	$\pm 1.0$	$\mu\text{A}$
		Data pins $V_{CC} = 5.5\text{ V}$ ; $V_I = \text{GND}$ or $5.5\text{ V}$	–	$\pm 5$	$\pm 100$	–	$\pm 100$	$\mu\text{A}$
$I_{OFF}$	Power-off leakage current	$V_{CC} = 0.0\text{ V}$ ; $V_I$ or $V_O \leq 4.5\text{ V}$	–	$\pm 5.0$	$\pm 100$	–	$\pm 100$	$\mu\text{A}$
$I_{PU}/I_{PD}$	Power-up/down 3-State output current <sup>3</sup>	$V_{CC} = 2.1\text{ V}$ ; $V_O = 0.5\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $V_{OE} = \text{Don't care}$	–	$\pm 5.0$	$\pm 50$	–	$\pm 50$	$\mu\text{A}$
$I_{IH} + I_{OZH}$	3-State output High current	$V_{CC} = 5.5\text{ V}$ ; $V_O = 2.7\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$	–	5.0	50	–	50	$\mu\text{A}$
$I_{IL} + I_{OZL}$	3-State output Low current	$V_{CC} = 5.5\text{ V}$ ; $V_O = 0.5\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$	–	–5.0	–50	–	–50	$\mu\text{A}$
$I_{CEX}$	Output high leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_O = 5.5\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$	–	5.0	50	–	50	$\mu\text{A}$
$I_O$	Output current <sup>1</sup>	$V_{CC} = 5.5\text{ V}$ ; $V_O = 2.5\text{ V}$	–40	–100	–180	–40	–180	mA
$I_{CCH}$	Quiescent supply current	$V_{CC} = 5.5\text{ V}$ ; Outputs HIGH, $V_I = \text{GND}$ or $V_{CC}$	–	50	250	–	250	$\mu\text{A}$
$I_{CCL}$		$V_{CC} = 5.5\text{ V}$ ; Outputs LOW, $V_I = \text{GND}$ or $V_{CC}$	–	24	30	–	30	mA
$I_{CCZ}$		$V_{CC} = 5.5\text{ V}$ ; Outputs 3-State; $V_I = \text{GND}$ or $V_{CC}$	–	50	250	–	250	$\mu\text{A}$
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	Outputs enabled, one input at 3.4 V, other inputs at $V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	–	0.5	1.5	–	1.5	mA
		Outputs 3-State, one data input at 3.4 V, other inputs at $V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	–	50	250	–	250	$\mu\text{A}$
		Outputs 3-State, one enable input at 3.4 V, other inputs at $V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	–	0.5	1.5	–	1.5	mA

### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V with a transition time of up to 10 msec. From  $V_{CC} = 2.1\text{ V}$  to  $V_{CC} = 5\text{ V} \pm 10\%$ , a transition time of up to 100  $\mu\text{sec}$  is permitted.

# Octal transceiver with direction pin and 30 Ω series termination resistors (3-State)

74ABT2245

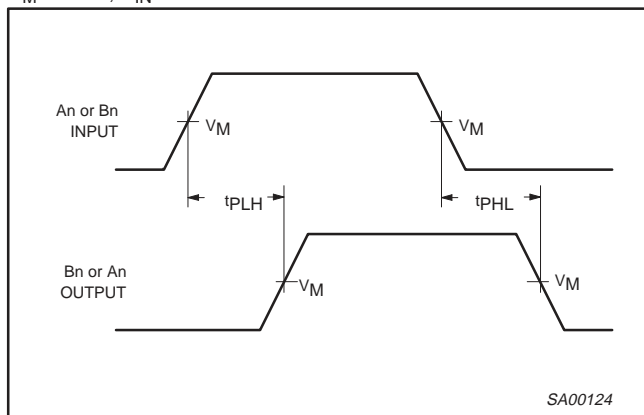
## AC CHARACTERISTICS

GND = 0 V;  $t_R = t_F = 2.5 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$

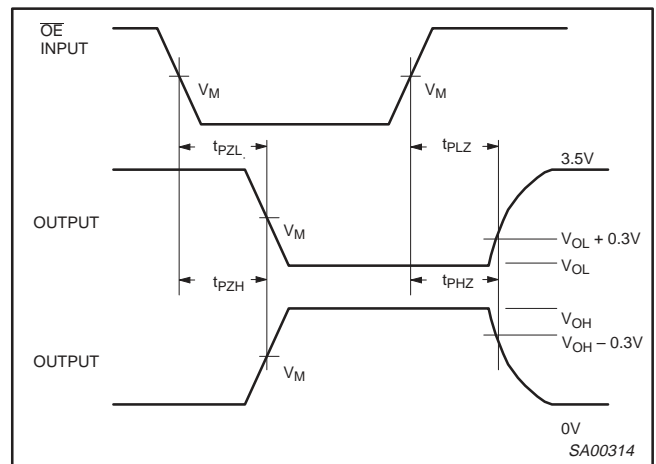
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{amb} = +25 \text{ }^\circ\text{C}$ $V_{CC} = +5.0 \text{ V}$			$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ $V_{CC} = +5.0 \text{ V } \pm 0.5 \text{ V}$		
			Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	1	1.0	2.8	4.2	1.0	4.7	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to HIGH and LOW level	2	1.3	3.5	4.6	1.3	5.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from HIGH and LOW Level	2	1.5	4.0	5.4	1.5	6.3	ns

## AC WAVEFORMS

$V_M = 1.5 \text{ V}$ ,  $V_{IN} = \text{GND to } 3.0 \text{ V}$



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

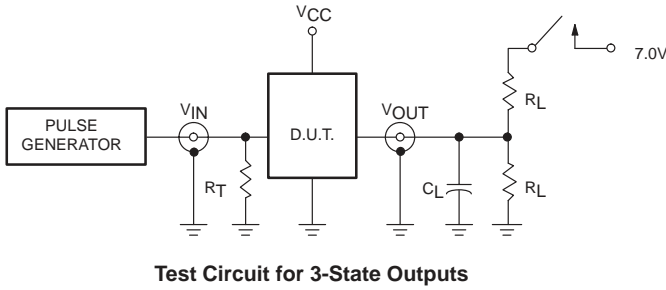


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

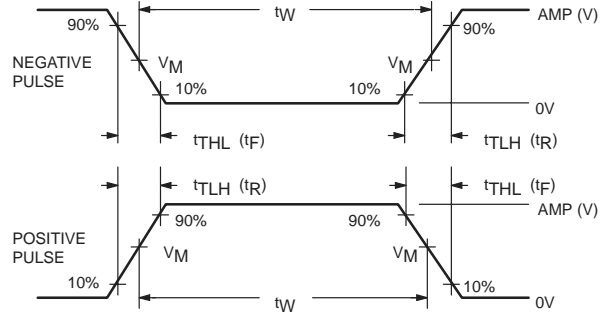
# Octal transceiver with direction pin and 30 Ω series termination resistors (3-State)

74ABT2245

## TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

### SWITCH POSITION

TEST	SWITCH
tPLZ	closed
tPZL	closed
All other	open

### DEFINITIONS

- RL = Load resistor; see AC CHARACTERISTICS for value.
- CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- RT = Termination resistance should be equal to ZOUT of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	tW	tR	tF
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

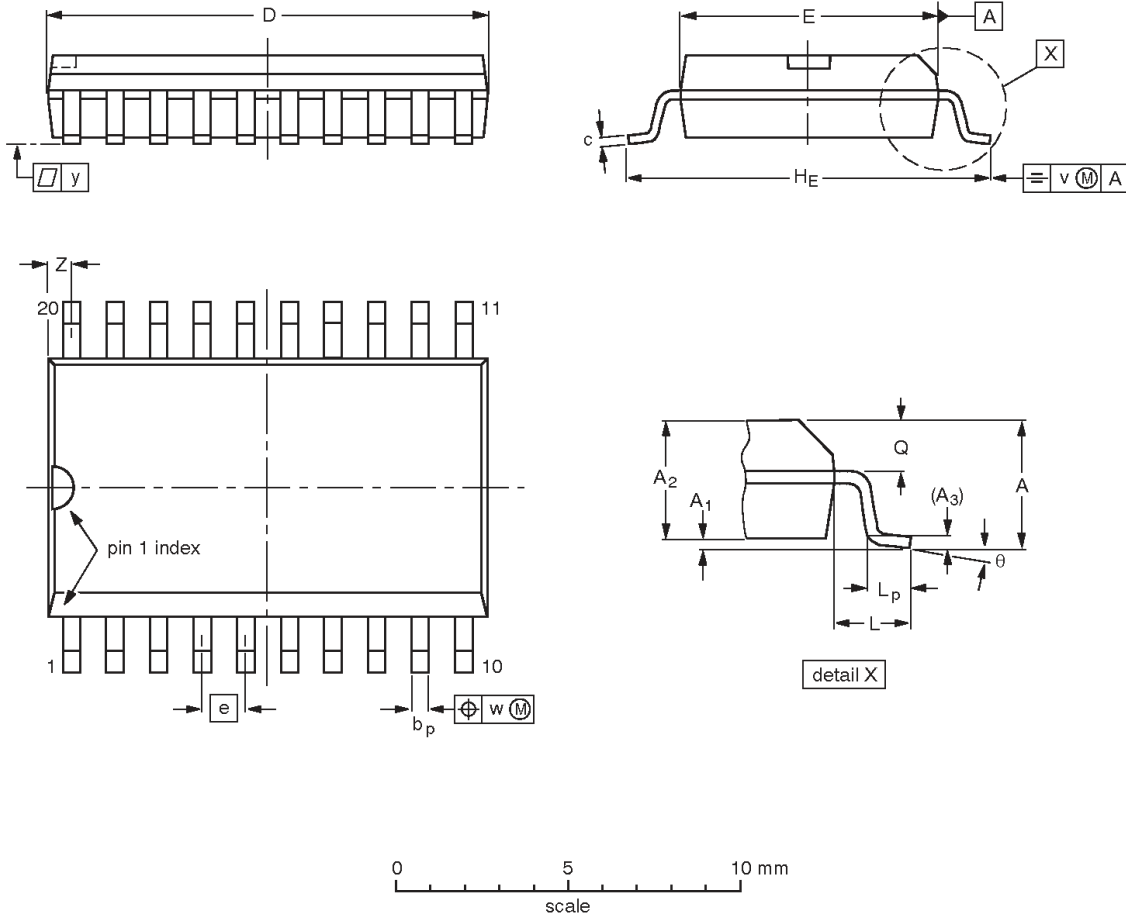
SA00012

# Octal transceiver with direction pin and 30 Ω series termination resistors (3-State)

74ABT2245

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				97-05-22 99-12-27

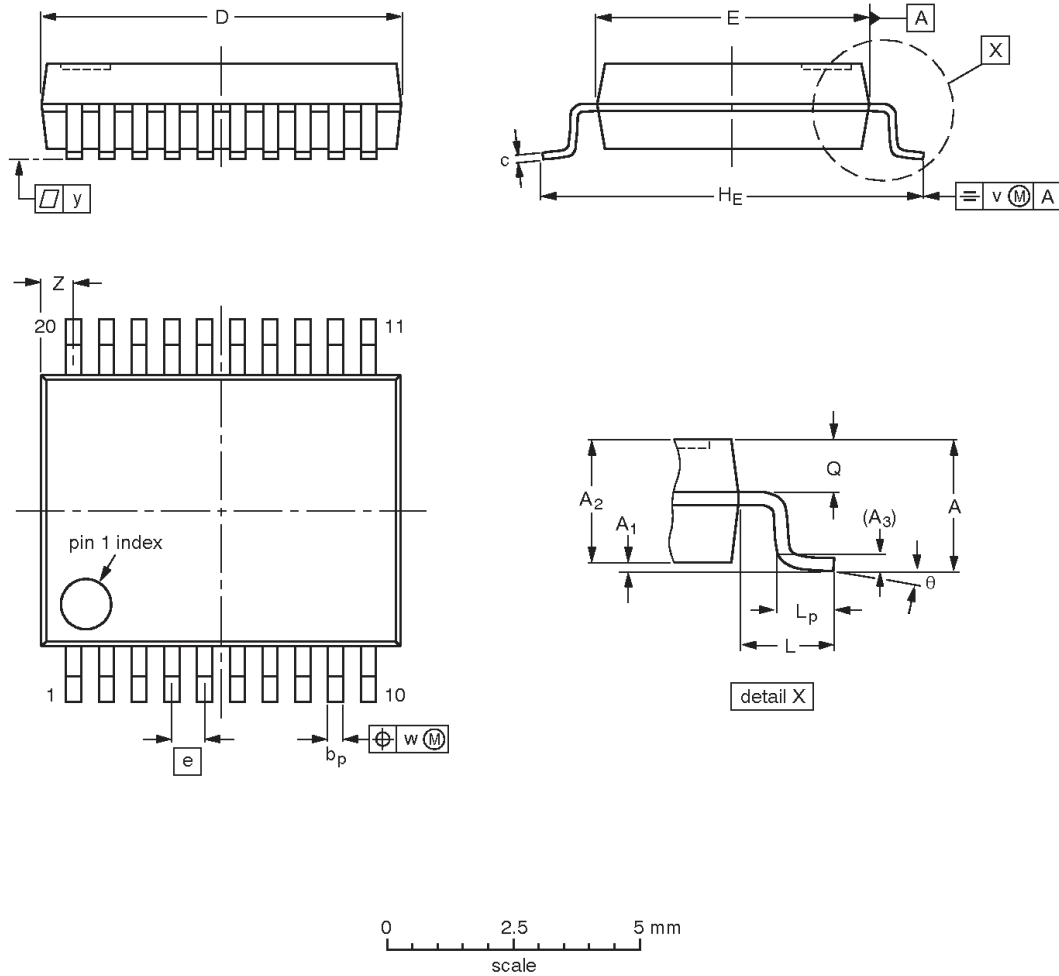


# Octal transceiver with direction pin and 30 Ω series termination resistors (3-State)

74ABT2245

**SSOP20:** plastic shrink small outline package; 20 leads; body width 5.3 mm

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

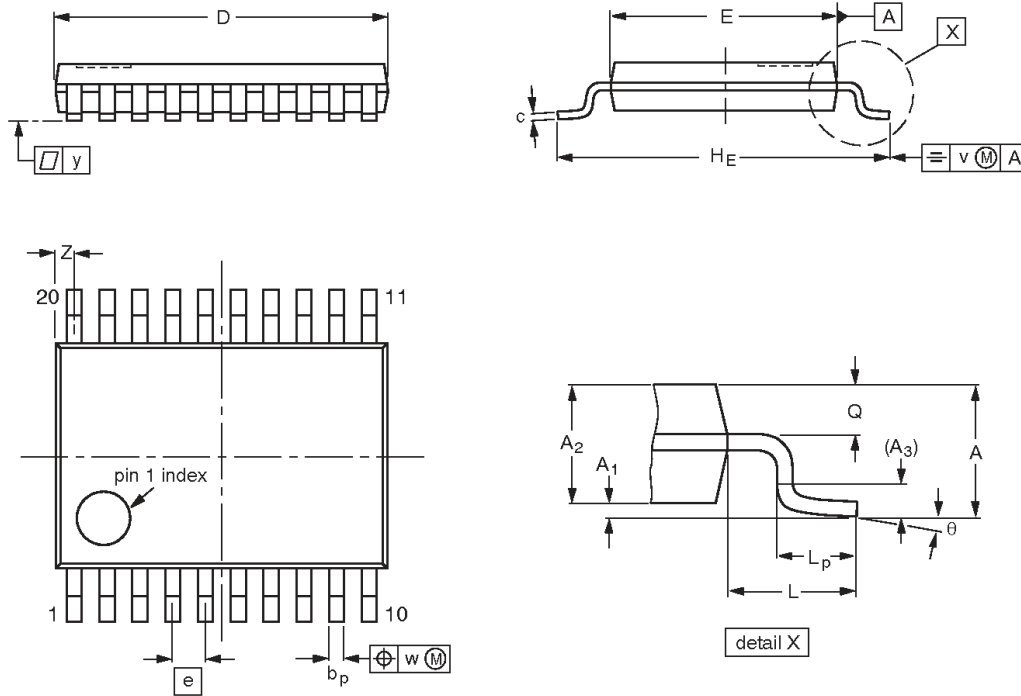
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150				95-02-04 99-12-27

# Octal transceiver with direction pin and 30 Ω series termination resistors (3-State)

74ABT2245

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				95-02-04 99-12-27

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**Octal transceiver with direction pin and  
30  $\Omega$  series termination resistors (3-State)**

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**74ABT2245****REVISION HISTORY**

Rev	Date	Description
_3	20021217	<b>Product data (9397 750 10846); ECN 853-1761 29292 of 12 December 2002. Supersedes data of 16 January 1998 (9397 750 03468).</b> Modifications: <ul style="list-style-type: none"><li>● Ordering information table: remove "North America" column; remove 74ABT2245N package offering.</li></ul>
_2	19980116	<b>Product specification (9397 750 03468); ECN 853-1761 18865 of 16 January 1998. Supersedes data of 1995 September 06.</b>
_1	19950906	<b>Product specification; ECN 853-1761 15701 of 06 September 1995.</b>

# Octal transceiver with direction pin and 30 $\Omega$ series termination resistors (3-State)

74ABT2245

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
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Document order number: 9397 750 10846

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