Using the TPS40222, a 5-V Input, 1.6-A Output, Nonsynchronous Buck Converter

The TPS40222EVM-001 evaluation module (EVM) is a nonsynchronous buck converter with a 4.5-V to 8-V input range with a built-in N-channel power FET, that can deliver 1.6 A of output current. The EVM is designed to operate with a minimum of components and yet has the features of more complex buck converters.

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1 Description

The TPS40222EVM-001 is designed to use a 4.5- to 8-V input voltage to produce a high-current, regulated 1.4-V output at up to 1.6 A of load current. This application board is designed to demonstrate the TPS40222 in a typical voltage bus to low-voltage application while providing a number of test points to evaluate the performance of the IC. Users can modify the EVM to support output voltages from 0.8 V to 6.3 V by changing a single resistor. The TPS402224EVM-001 was built to the application example used in the TPS40222 data sheet with the internal clock operating at 1.25 MHz.

1.1 Features

- 4.5-V to 8-V input range
- 0.8-V to 6.3-V output, adjustable with single resistor
- 1.6-Adc steady-state output current
- Internally compensated error amplifier
- Fixed 1.25-MHz switching frequency
- Internal N-channel FET
- Surface-mount design on a two-layer, 1.1 x 1.875-inch evaluation board
- Convenient test points for probing critical waveforms and noninvasive loop response testing

1.2 Applications

- Non-isolated point of load and low-voltage bus converters.
- Merchant power modules
- Disk drives
- Point of load power
- ASIC power supplies

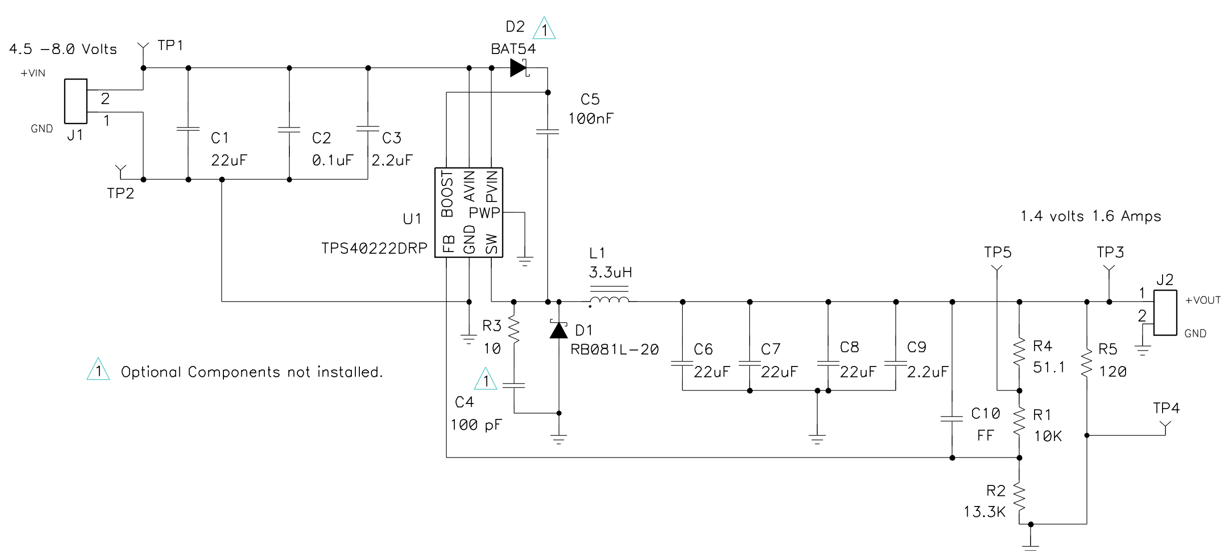
2 Electrical Specifications

2.1 *TPS40222EVM-001 Electrical Performance Specifications*

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Voltage Range			4.5		8	V
Max Input Current	V_{IN} = 5 V, I_{OUT} = 1.0 A				0.375	A
No-Load Input Current	V_{IN} = 5 V, I_{OUT} = 0 A, R5 = 120 Ω (10 mA Load)			11		mA
OUTPUT CHARACTERISTICS						
Output Voltage	R2 = 10.0 k R1 = 7.5 k(1)		1.358	1.40	1.442	V
Output Voltage Regulation	Line Regulation (4.5 V < V_{IN} < 5.5 V, I_{OUT} = 1 A)			0.1%		
	Load Regulation (0 A < I_{OUT} < 1.0 A, V_{IN} = 5 V)			0.15%		
Output Voltage Ripple	V_{IN} = 5 V, I_{OUT} = 1.0 A			10		mVpp
Output Load Current			0		1.6	A
Output Over Current				2.6		A
SYSTEM CHARACTERISTICS						
Switching Frequency			1.0	1.25	1.5(1)	MHz
Peak Efficiency	V_{OUT} = 3.3 V, 0.1 A < I_{OUT} < 1.0 A	V_{5V_IN} = 4.5 V		89%		
		V_{5V_IN} = 5 V		90%		
		V_{5V_IN} = 5.5 V		91%		
Full Load Efficiency	V_{OUT} = 1.25 V, I_{OUT} = 1.6 A	V_{5V_IN} = 4.5 V		73%		
		V_{5V_IN} = 5 V		74%		
		V_{5V_IN} = 5.5 V		75%		

(1) Set-point accuracy determined by reference voltage and user-selected resistor accuracy.

3 Schematic



NOTE: For reference only, see Table 2: Bill of Materials for Specific Values

Figure 1. TPS40222EVM-001 Schematic

3.1 Adjusting Output Voltage (R1and R2)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R1 and R2). The output voltage is given by Equation 1:

$$V_{out} = V_{FB}\left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where V_{FB} = 0.800 V and R1 = 10 kΩ

Table 1 contains common values for R2 to generate popular output voltages. The TPS40222EVM-001 is stable through these output voltages with the efficiency improving with increasing output voltage.

Table 1. Common Values for R2

Output Voltage — V_{OUT}	R2, 1% (kΩ)
3.3	3.16
2.5	4.70
2.2	5.62
2	6.65
1.8	8.06
1.5	11.5
1.4	13.3
1.2	20

3.2 Test Setup

3.2.1 Equipment

3.2.1.1 Voltage Source

V_{5V_IN} – The input voltage source (V_{5V_IN}) should be a 0-V to 15-V variable DC source capable of 5 Adc. Connect V_{5V_IN} to J1 as shown in Figure 2.

3.2.1.2 Meters

- A1: 0- to 5-Adc ammeter
- V1: V_{5V_IN}, 0-V to -15-V voltmeter
- V2: V_{1V4_OUT}, 0-V to 5-V voltmeter

3.2.1.3 Loads

LOAD1 – The Output Load (LOAD1) should be an electronic constant-current-mode load capable of 0—10 Adc at 1.4 V.

3.2.1.4 Recommended Wire Gauge

V_{5V_IN} to J1 – The connection between the source voltage, V_{5V_IN} and J1 of HPA163 can carry as much as 2 Adc. The minimum recommended wire size is 16 AWG with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J2 to LOAD1 (Power) – The power connection between J2 of HPA163 and LOAD1 can carry as much as 3 Adc. The minimum recommended wire size is 2x 16 AWG, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

OSCILLOSCOPE – A 60-MHz or faster oscilloscope can be used to determine the ripple voltage on 1V4_OUT. The oscilloscope should be set for 1-MΩ impedance, AC coupling, 0.5-µs/division horizontal resolution, 10-mV/division vertical resolution for taking output ripple measurements. TP3 and TP4 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP3 and holding the ground barrel to TP4 as shown in Figure 3. For a hands-free approach, the loop in TP4 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

3.3 Equipment Setup

Figure 3 shows the basic test setup recommended to evaluate the TPS40222EVM-001. Note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 2.

3.3.1 Procedure

1. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{5V_IN}, it is advisable to limit the source current from V_{5V_IN} to 2 A maximum. Ensure that V_{5V_IN} is initially set to 0 V and connected as shown in Figure 2.
3. Connect the ammeter A1 (0–5-A range) between V_{5V_IN} and J1 as shown in Figure 2.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
5. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant-current mode to sink 0 Adc before V_{5V_IN} is applied.
6. Connect voltmeter, V2 across TP3 and TP4 as shown in Figure 2.
7. Connect oscilloscope probe to TP3 and TP4 as shown in Figure 3.

3.3.2 Diagram

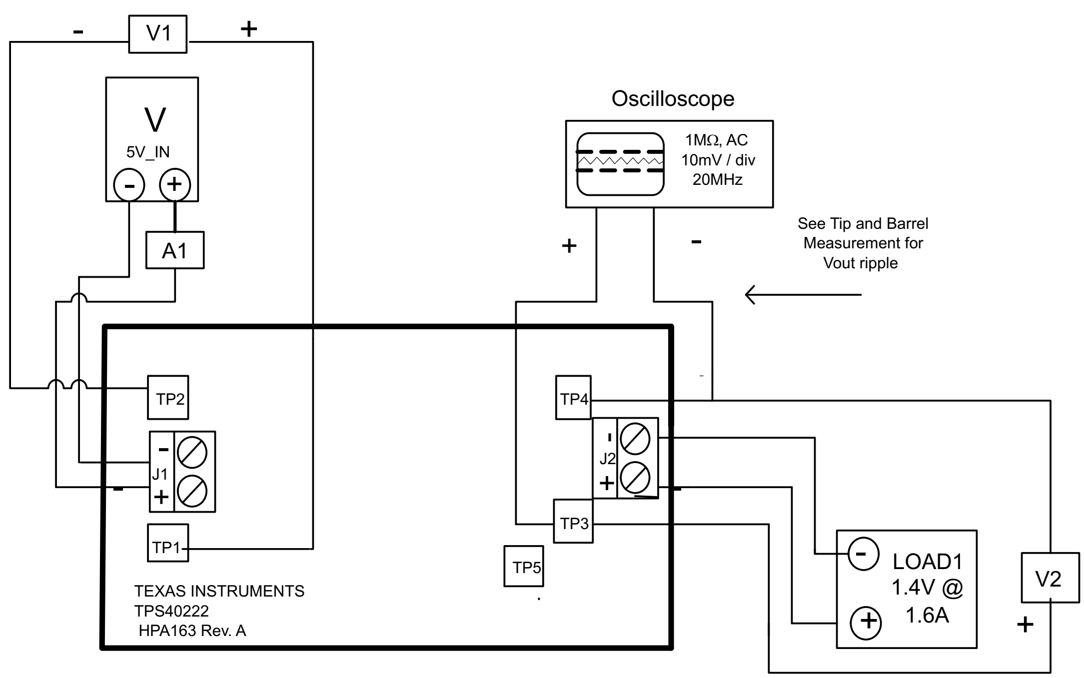


Figure 2. TPS40222EVM-001 Recommended Test Setup

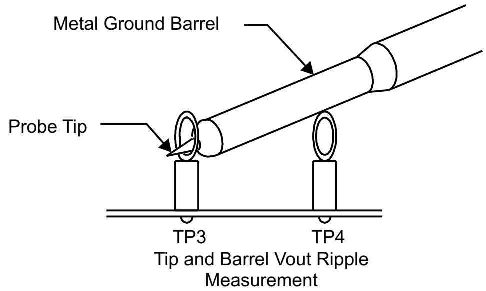


Figure 3. Output Ripple Measurement – Tip and Barrel Using TP15 and TP16

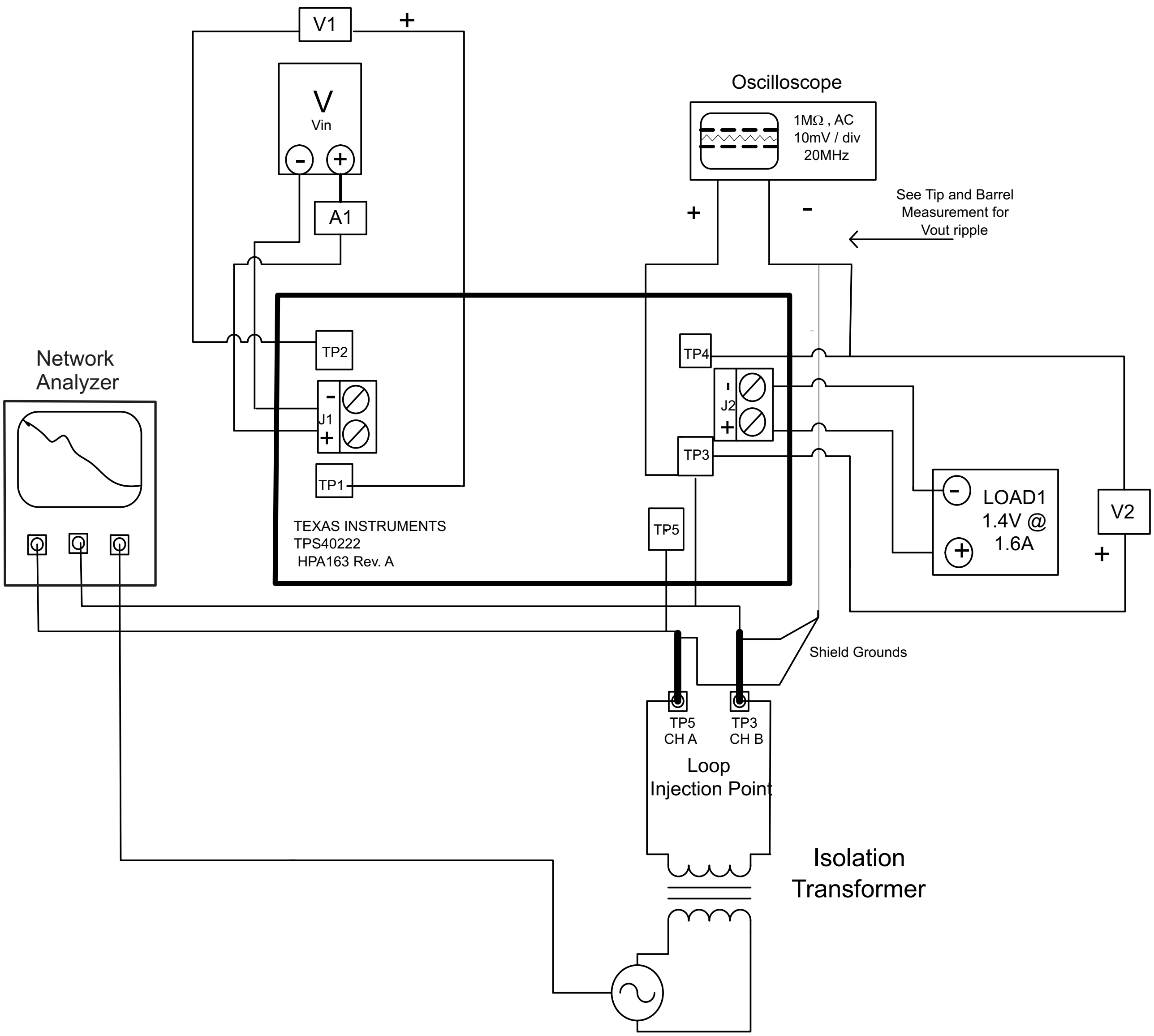


Figure 4. Control Loop Measurement Setup

3.4 Start -Up/Shutdown Procedure

1. Increase V_{5V_IN} (V1) from 0 V to 5 Vdc.
2. Vary LOAD1 from 0 to 1 Adc
3. Vary V_{5V_IN} (V1) from 5 Vdc to 8 Vdc
4. Decrease LOAD1 to 0 A.
5. Decrease V_{5V_IN} to 0 V.

3.5 Control Loop Gain and Phase Measurement Procedure

1. Connect 1-kHz to 1-MHz isolation transformer to TP5 and TP3 as show in Figure 4.
2. Connect input signal amplitude measurement probe (Channel A) to TP5 as shown in Figure 4.
3. Connect output signal amplitude measurement probe (Channel B) to TP3 as shown in Figure 4.
4. Connect ground lead of channel A and channel B to TP4 as shown in Figure 4.
5. Inject 25-mV or less signal across R4 through isolation transformer.
6. Sweep frequency from 1 kHz to 1 MHz with 10-Hz or lower post filter.
7. Control loop gain can be measured by: $20 \times \text{LOG}\left(\frac{\text{ChannelB}}{\text{ChannelA}}\right)$
8. Control loop phase is measured by the phase difference between channel A and channel B disconnect isolation transformer from TP5 and TP3 before making other measurements (signal injection into feedback may interfere with accuracy of other measurements.

3.6 Equipment Shutdown

1. Shut down oscilloscope.
2. Shut down LOAD1.
3. Shut down V_{5V_IN}.

4 TPS40222EVM Typical Performance Data and Characteristic Curves

Figure 4 through Figure 7 present typical performance curves for the TPS40222EVM-001. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

4.1 Efficiency

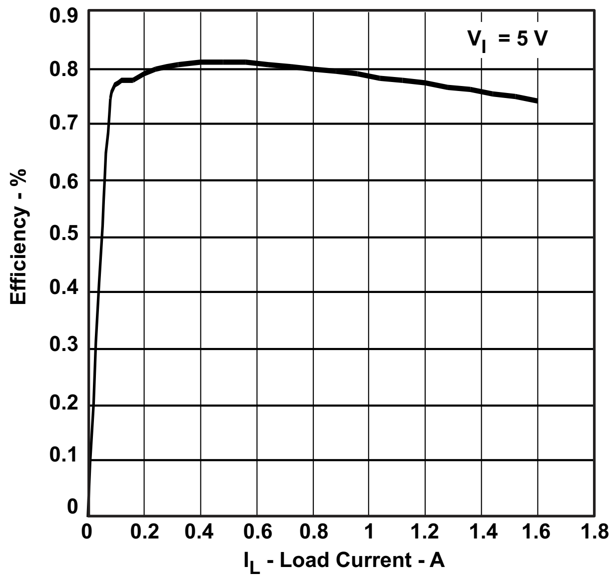


Figure 5. TPS40222EVM-001 Efficiency 1.4 V Out
(V_{5V_IN} = 4.5–8 V, V_{1V4_OUT} = 1.4 V, I_{1V5_OUT} = 0–1.6 A)

4.2 Line and Load Regulation

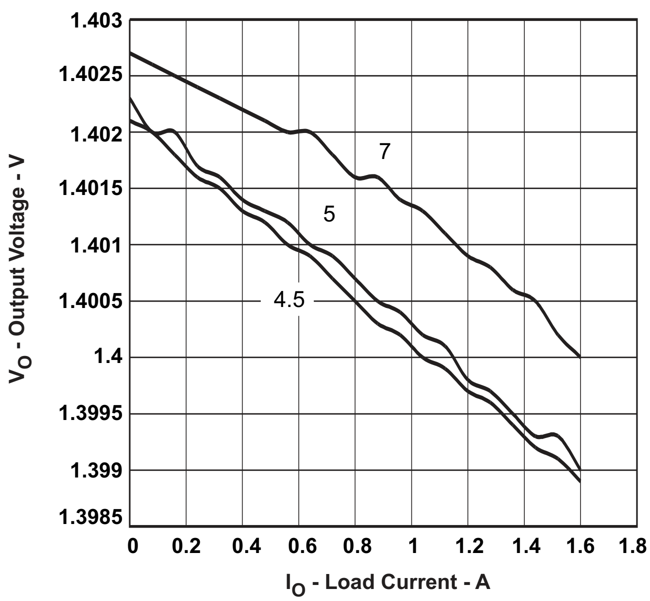


Figure 6. TPS402222EVM-001 Line and Load Regulation

4.3 Typical Ripple Voltage

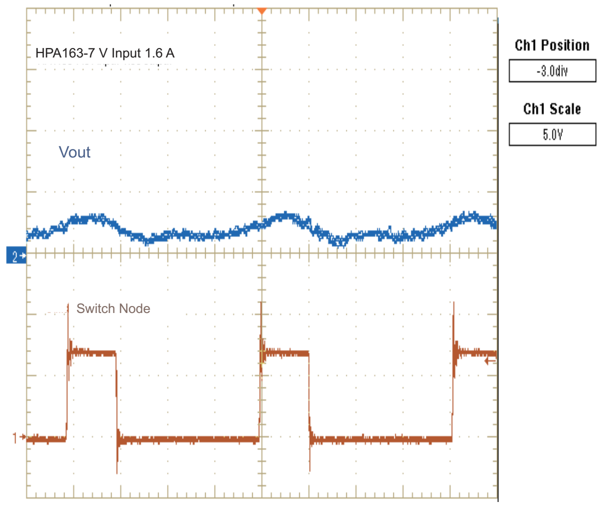


Figure 7. TPS40222EVM-001 Switch Node and Output Ripple at 1.6 A

5 EVM Assembly Drawings and Layout

The following figures (Figure 7 through Figure 11) show the design of the TPS40222EVM-001 printed-circuit board. The EVM has been designed using a 2-layer, 2-oz copper-clad circuit board 1.10 × 1.875 inch with all components on the top side to allow the user to easily view, probe, and evaluate the TPS40222 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

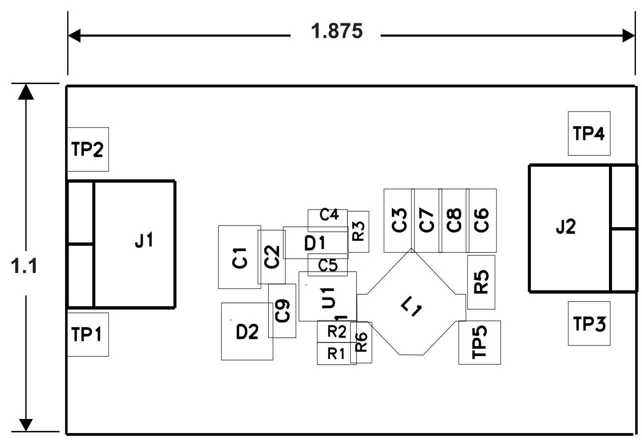


Figure 8. TPS40222EVM-001 Component Placement (Viewed From Top)

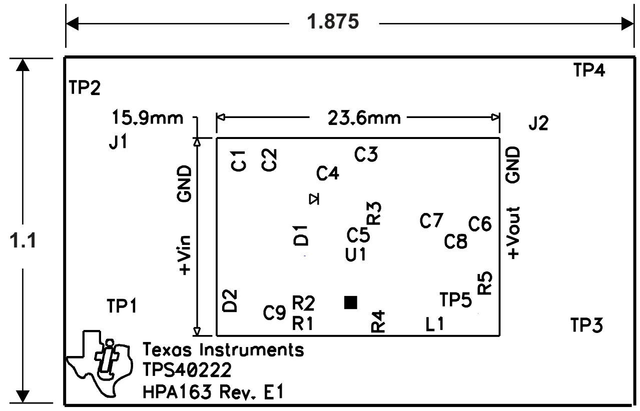


Figure 9. TPS40222EVM-001 Silkscreen (Viewed From Top)

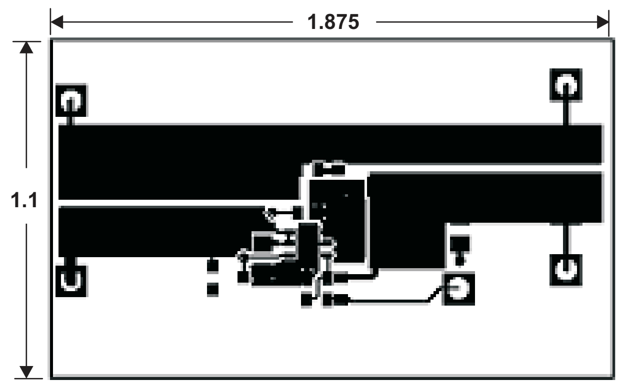


Figure 10. TPS40222EVM-001 Top Copper (Viewed From Top)

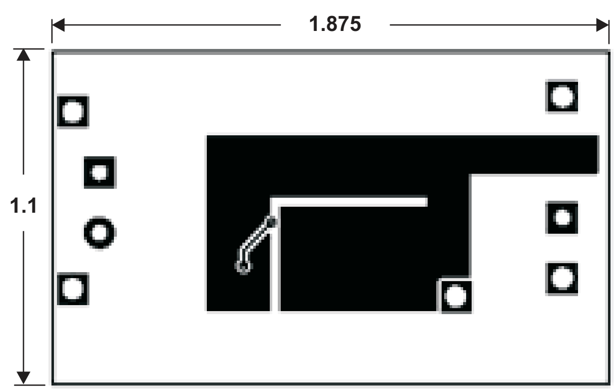


Figure 11. TPS40222EVM-001 Bottom Copper (X-Ray View From Top)

6 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1 and Figure 2.

Table 2. TPS40222EVM-001 Bill of Materials(1)(2)

Count	Reference Designator	Value	Description	Size	Part Number	MFR
1	C1	22µF	Capacitor, Ceramic, 22µF, 16V, [+80 -20%]	1210	ECJ4YF1C226Z	Panasonic
1	C2	0.1µF	Capacitor, Ceramic,0.1µF, 50V, X7R , 20%	0805	Std	Panasonic
1	C3	2.2 µF	Capacitor, Ceramic, 2.2µF, 16V, X5R, 20%	0805	ECJ2FB1C225M	Panasonic
1	C4	100pF	Capacitor, Ceramic, 100pF, 50-V, COG, 20%	0603	Std	Murata
1	C5	100nF	Capacitor, Ceramic, 16V, X7R	0603	Std	Murata
3	C6–C8	22µF/6.3V	Capacitor, Ceramic, 6.3V, 22µF, 20%	1206	ECJ3YB1C225M	Panasonic
1	C9	2.2µF	Capacitor, Ceramic, 16V, 2.2µF, 20%	1206	ECJ3YB1C225M	Panasonic
1	D1	RB081L-20	Diode, Schottky Barrier, 5A, 20V	SOD-106	RBO81L-20	Rohm
1	D2	BAT54	Diode, Schottky, 200mA, 30V	SOT23	BAT54	Vishay
2	J1, J2	ED1609-ND	Terminal Block, 2-pin, 15A, 5,1mm	0.40 × 0.35	ED1609	OST
1	L1	3.3µH	Inductor, SMT, 3.3µH, 1.9A, 32mΩ	0.236 × 0.236	ELL6PV3R3N	Panasonic
1	R1	10kΩ	Resistor, Chip, 10kΩ, 1/16W, 1%	0603	Std	Std
1	R2	13.3kΩ	Resistor, Chip, 13.3kΩ,1/16W, 1%	0603	Std	Std
1	R3	10Ω	Resistor, Chip, 10Ω, 1/16W, 1%	0603	Std	Std
1	R4	51.1Ω	Resistor, Chip, 51.1Ω, 1/16W, 1%	0603	Std	Std
1	R5	120Ω	Resistor, Chip, 120Ω, 1/10W, 1%	0805	Std	Std
1	U1	TPS40222	IC, 6 pin Non-Synchronous Buck Converter	DRP-6	TPS40222DRP	TI
1	PCB		PCB, 1.875 In × 1.1 In × 62 In		HPA163A	Any

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 16 V and the output voltage range of 0 V to 6.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 49°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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