Complementary Silicon Plastic Power Transistors

DPAK-3 for Surface Mount Applications

Designed for low voltage, low-power, high-gain audio amplifier applications.

Features

- High DC Current Gain
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Low Collector–Emitter Saturation Voltage
- High Current-Gain Bandwidth Product
- Annular Construction for Low Leakage
- Epoxy Meets UL 94 V-0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V _{CB}	100	Vdc
Collector-Emitter Voltage	V _{CEO}	100	Vdc
Emitter-Base Voltage	V _{EB}	7.0	Vdc
Collector Current – Continuous	۱ _C	4.0	Adc
Collector Current – Peak	I _{CM}	8.0	Adc
Base Current	Ι _Β	1.0	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	12.5 0.1	W W/°C
Total Device Dissipation @ T _A = 25°C (Note 2) Derate above 25°C	P _D	1.4 0.011	W W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	С	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted on minimum pad sizes recommended.

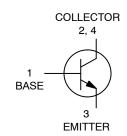


ON Semiconductor®

www.onsemi.com

4.0 A, 100 V, 12.5 W POWER TRANSISTOR

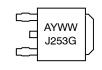
COMPLEMENTARY





CASE 369C STYLE 1

MARKING DIAGRAM



= Assembly Location

= Year

A

- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NJVMJD253T4G-VF01*	DPAK (Pb–Free)	2,500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

	Unit
10	°C/W
	10 89.3

2. When surface mounted on minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

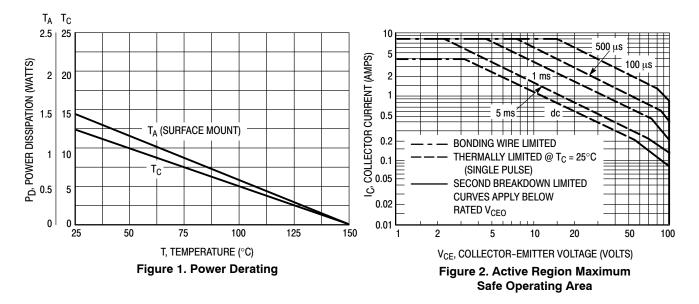
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			1	
Collector-Emitter Sustaining Voltage (Note 3) $(I_{C} = 10 \text{ mAdc}, I_{B} = 0)$	V _{CEO(sus)}	100	_	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)	I _{CBO}		100 100	nAdc μAdc
Emitter Cutoff Current (V _{BE} = 7.0 Vdc, I _C = 0)	I _{EBO}	-	100	nAdc
DC Current Gain (Note 3) ($I_C = 200 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$)	h _{FE}	40 15	180	-
Collector-Emitter Saturation Voltage (Note 3) ($I_C = 500$ mAdc, $I_B = 50$ mAdc) ($I_C = 1.0$ Adc, $I_B = 100$ mAdc)	V _{CE(sat)}		0.3 0.6	Vdc
Base-Emitter Saturation Voltage (Note 3) $(I_C = 2.0 \text{ Adc}, I_B = 200 \text{ mAdc})$	V _{BE(sat)}	-	1.8	Vdc
Base-Emitter On Voltage (Note 3) (I _C = 500 mAdc, V _{CE} = 1.0 Vdc)	V _{BE(on)}	-	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain – Bandwidth Product (Note 4) (I _C = 100 mAdc, V _{CE} = 10 Vdc, f _{test} = 10 MHz)	f _T	40	_	MHz
	C _{ob}		50	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 3. Pulse Test: Pulse Width = $300 \ \mu$ s, Duty Cycle $\approx 2\%$.

50

 $(V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz})$

4. $f_T = |h_{FE}| \bullet f_{test}$.



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

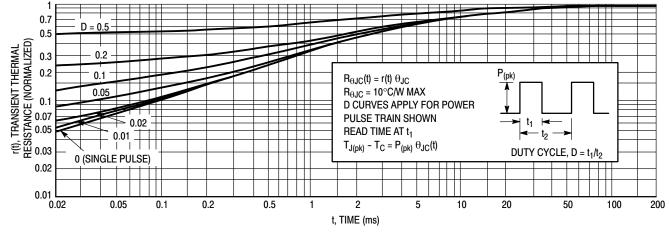
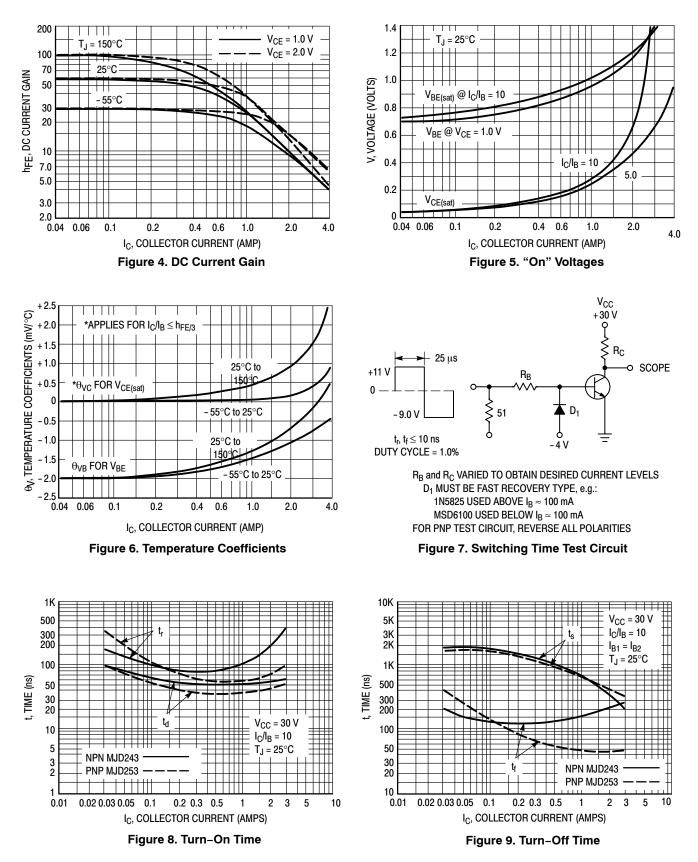
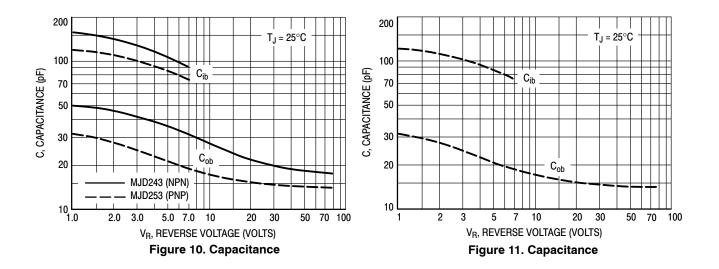


Figure 3. Thermal Response

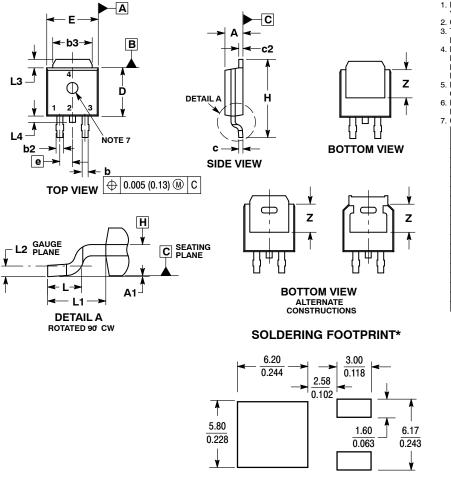




PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C

ISSUE F



NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME
- Y14.5M, 1994. 2. CONTROLLING DIMENSION: INCHES.
- 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3, L3 and Z.
- A DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
е	0.090	BSC	2.29 BSC	
н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90 REF	
L2	0.020	BSC	0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

STYLE 1: PIN 1. BASE 2. COLLECTOR

 $\left(\frac{mm}{inches}\right)$

SCALE 3:1

EMITTER COLLECTOR 3.

4

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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