

## OPAx187 0.001- $\mu\text{V}/^\circ\text{C}$ Drift, Low Power, Rail-to-Rail Output 36-V Operational Amplifiers Zero-Drift Series

### 1 Features

- Low offset voltage: 10  $\mu\text{V}$  (maximum)
- Zero drift: 0.001  $\mu\text{V}/^\circ\text{C}$
- Low noise: 15  $\text{nV}/\sqrt{\text{Hz}}$
- PSRR: 160 dB
- CMRR: 140 dB
- AOL: 160 dB
- Quiescent Current: 100  $\mu\text{A}$
- Wide supply voltage:  $\pm 2.25\text{ V}$  to  $\pm 18\text{ V}$
- Rail-to-rail output operation
- Input includes negative rail
- Low bias current: 100 pA (typical)
- EMI filtered inputs
- Microsize packages

### 2 Applications

- [Analog input module](#)
- [Mixed module \(AI, AO, DI, DO\)](#)
- [Flow transmitter](#)
- [Pressure transmitter](#)
- [Test and measurement](#)
- [Semiconductor test](#)
- [Semiconductor manufacturing](#)
- [Process analytics \(pH, gas, concentration, force, and humidity\)](#)

### 3 Description

The OPAx187 series operational amplifiers use auto-zeroing techniques to simultaneously provide low-offset voltage (1  $\mu\text{V}$ ), and near zero drift over time and temperature. These miniature, high-precision, low-quiescent current amplifiers offer high-input impedance and rail-to-rail output swing within 5 mV of the rails into high-impedance loads. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4.5 V to 36 V ( $\pm 2.25\text{ V}$  to  $\pm 18\text{ V}$ ).

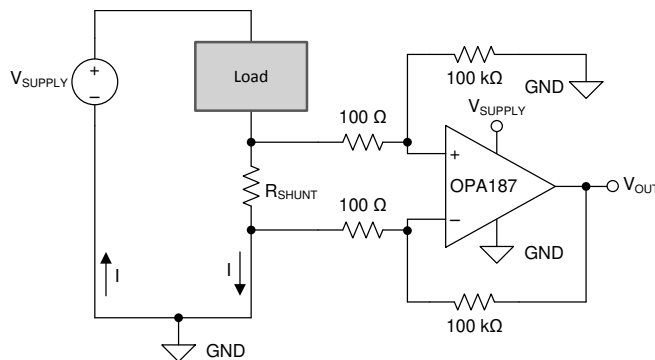
The single version OPAx187 device is available in microsize 8-pin VSSOP, 5-pin SOT-23, and 8-pin SOIC packages. The dual version is offered in 8-pin VSSOP and 8-pin SOIC packages. The quad version is offered in 14-pin SOIC, 14-pin TSSOP, and 16-pin WQFN packages. All versions are specified for operation from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA187	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2187	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4187	SOIC (14)	8.70 mm × 3.90 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

### OPAx187 Offers Precision Low-Side Current Measurement Capability



$$G = 1000 \cdot R_{\text{SHUNT}} \cdot I$$



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (December 2018) to Revision E</b>	<b>Page</b>
• Changed OPA4187 RUM (WQFN) package from preview to production data (active) .....	1

<b>Changes from Revision C (December 2018) to Revision D</b>	<b>Page</b>
• Changed OPA4187 SOIC and TSSOP packages from product preview to production data .....	1
• Changed offset drift (high and low supply) max to $\pm 15\text{nV}/^\circ\text{C}$ .....	9

<b>Changes from Revision B (October 2018) to Revision C</b>	<b>Page</b>
• First release of production OPA187 SOIC device .....	1

<b>Changes from Revision A (July 2017) to Revision B</b>	<b>Page</b>
• Changed OPA187 SOIC status to preview .....	1
• Changed OPA4187 SOIC, TSSOP and WQFN status to preview .....	1
• Changed offset drift (high supply) typical from $\pm 5\text{ nV}/^\circ\text{C}$ to $\pm 1\text{ nV}/^\circ\text{C}$ and max from $\pm 50\text{ nV}/^\circ\text{C}$ to $\pm 20\text{ nV}/^\circ\text{C}$ .....	8
• Changed input bias current max (high supply) from $\pm 5\text{ nA}$ to $\pm 7.5\text{ nA}$ .....	8
• Changed input offset current max (high supply) from $\pm 5\text{ nA}$ to $\pm 14.5\text{ nA}$ .....	8
• Changed offset drift (low supply) typical from $\pm 5\text{ nV}/^\circ\text{C}$ to $\pm 1\text{ nV}/^\circ\text{C}$ and max from $\pm 50\text{ nV}/^\circ\text{C}$ to $\pm 20\text{ nV}/^\circ\text{C}$ .....	9
• Changed Offset Voltage Production Distribution figure .....	11

**Changes from Original (December 2016) to Revision A****Page**

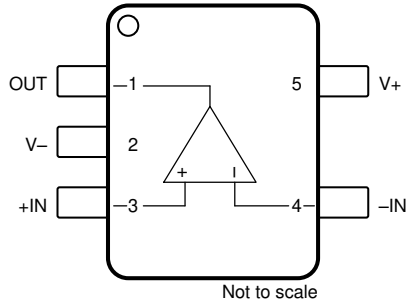
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• Deleted VSON package option from the Description .....	1
• Deleted VSON package option from the <i>Device Information</i> table .....	1
• Added WQFN package option to the <i>Device Information</i> table.....	1
• Deleted OPA187 DRG package option from <i>Pin Configuration and Functions</i> .....	4
• Added WQFN package to <i>Pin Configuration and Functions</i> .....	5

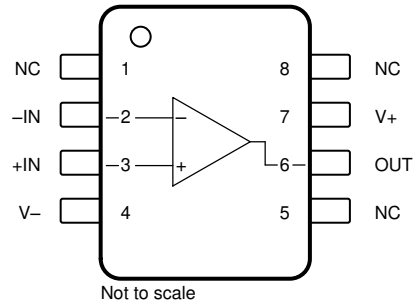
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## 5 Pin Configuration and Functions

OPA187: DBV Package  
5-Pin SOT-23  
Top View



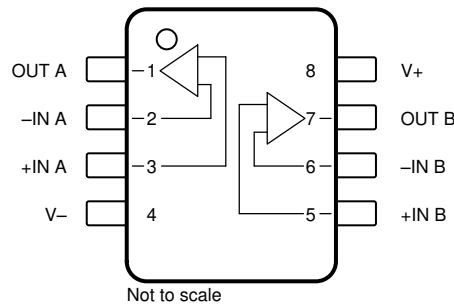
OPA187: D and DGK Packages  
8-Pin SOIC and 8-pin VSSOP  
Top View



Pin Functions: OPA187

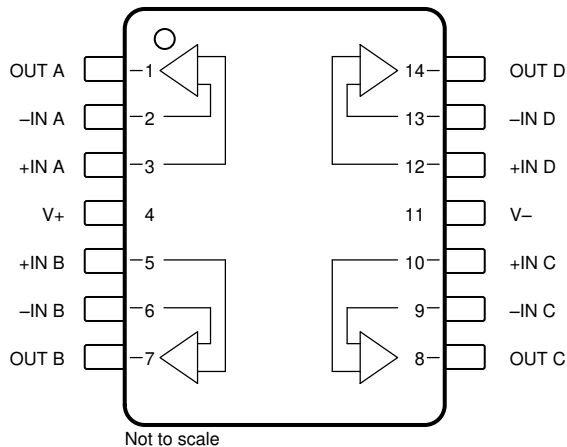
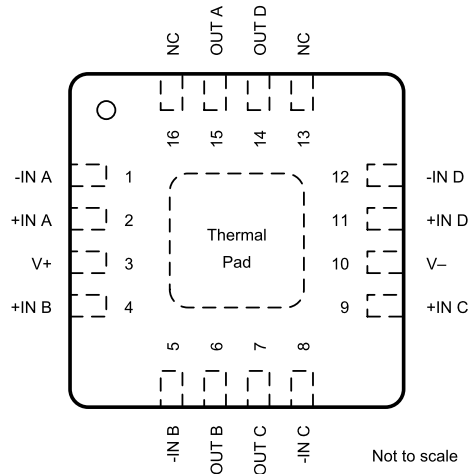
NAME	PIN		I/O	DESCRIPTION
	DBV	D and DGK		
+IN	3	3	I	Non-inverting input
-IN	4	2	I	Inverting input
NC	—	1, 5, 8	—	No connection (can be left floating)
OUT	1	6	O	Output signal
V+	5	7	—	Positive (highest) supply voltage
V-	2	4	—	Negative (lowest) supply voltage

OPA2187: D and DGK Packages  
8-Pin SOIC and 8-Pin VSSOP  
Top View



Pin Functions: OPA2187

NAME	PIN		I/O	DESCRIPTION
	D and DGK			
+IN A	3		I	Non-inverting input, channel A
-IN A	2		I	Inverting input, channel A
+IN B	5		I	Non-inverting input, channel B
-IN B	6		I	Inverting input, channel B
OUT A	1		O	Output, channel A
OUT B	7		O	Output, channel B
V+	8		—	Positive (highest) supply voltage
V-	4		—	Negative (lowest) supply voltage

**OPA4187: D and PW Packages  
14-pin SOIC and 14-Pin TSSOP  
Top View**

**OPA4187: RUM Package  
16-pin WQFN  
Top View**

**Pin Functions: OPA4187**

NAME	PIN		I/O	DESCRIPTION
	D and PW	RUM		
+IN A	3	2	I	Non-inverting input, channel A
-IN A	2	1	I	Inverting input, channel A
+IN B	5	4	I	Non-inverting input, channel B
-IN B	6	5	I	Inverting input, channel B
+IN C	10	9	I	Non-inverting input, channel C
-IN C	9	8	I	Inverting input, channel C
+IN D	12	11	I	Non-inverting input, channel D
-IN D	13	12	I	Inverting input, channel D
OUT A	1	15	O	Output, channel A
OUT B	7	6	O	Output, channel B
OUT C	8	7	O	Output, channel C
OUT D	14	14	O	Output, channel D
V+	4	3	—	Positive (highest) supply voltage
V-	11	10	—	Negative (lowest) supply voltage
NC	—	13, 16	—	No internal connection (can be left floating)

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply, $V_S = (V^+) - (V^-)$		40	V
	Signal input pin <sup>(2)</sup>	$(V^-) - 0.5$	$(V^+) + 0.5$	
	Signal output pin <sup>(3)</sup>	$(V^-) - 0.5$	$(V^+) + 0.5$	
Current	Signal input pin <sup>(2)</sup>	-10	10	mA
	Signal output pin <sup>(3)</sup>	-55	55	mA
	Output short-circuit <sup>(4)</sup>	Continuous	Continuous	
Temperature	Operating range, $T_A$	-55	150	°C
	Junction, $T_J$		150	
	Storage, $T_{stg}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to  $\pm 10$  mA or less.
- (3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5 V beyond the supply rails should be current limited to  $\pm 55$  mA or less.
- (4) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 4000$	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 1500$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$(V^+) - (V^-)$	Supply voltage	4.5 ( $\pm 2.25$ )		36 ( $\pm 18$ )	V
$T_A$	Operating temperature	-40		150	°C

## 6.4 Thermal Information: OPA187

THERMAL METRIC <sup>(1)</sup>		OPA187			UNIT
		5 PINS	8 PINS		
		DBV (SOT-23)	DGK (VSSOP)	D (SOIC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	273.8	159	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.8	37	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.9	49	41.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	10.9	1.2	4.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	84.9	77.1	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Thermal Information: OPA2187

THERMAL METRIC <sup>(1)</sup>		OPA2187		UNIT
		8 PINS		
		DGK (VSSOP)	D (SOIC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	159	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49	41.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.2	4.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	77.1	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Thermal Information: OPA4187

THERMAL METRIC <sup>(1)</sup>		OPA4187			UNIT
		14 PINS	16 PINS		
		PW (TSSOP)	D (SOIC)	RUM (WQFN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	83.8	35.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	70.7	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	59.5	12.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.5	11.6	0.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	51.6	37.7	12.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	3.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.7 Electrical Characteristics: High-Voltage Operation

at  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 4\text{ V}$  to  $\pm 18\text{ V}$  ( $V_S = +8\text{ V}$  to  $+36\text{ V}$ ),  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2^{(1)}$ , and  $V_{CM} = V_{OUT} = V_S / 2^{(1)}$  (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage			$\pm 1$	$\pm 10$	$\mu\text{V}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.001$	$\pm 0.015$	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4.5\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.01$	$\pm 1$	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{CM} = V_S / 2$		$\pm 100$	$\pm 350$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 7.5$	$\text{nA}$
$I_{OS}$	Input offset current			$\pm 100$	$\pm 500$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 14.5$	$\text{nA}$
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.4		$\mu\text{V}_{PP}$
		$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		60		$\text{nV}_{RMS}$
	Input voltage noise density	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		160		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range		$(V-) - 0.1$		$(V+) - 2$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ , $V_S = \pm 18\text{ V}$	126	140		$\text{dB}$
		$(V-) < V_{CM} < (V+) - 2\text{ V}$ , $V_S = \pm 18\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	130	145		$\text{dB}$
<b>INPUT IMPEDANCE</b>						
$Z_{ID}$	Differential			$100 \parallel 6$		$\text{M}\Omega \parallel \text{pF}$
$Z_{IC}$	Common-mode			$6 \parallel 4.2$		$10^{12}\ \Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ , $(V-) + 0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$ , $R_L = 10\text{ k}\Omega$	132	160		$\text{dB}$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product			550		$\text{kHz}$
SR	Slew rate	$V_O = 10\text{-V}$ step, $G = +1$		0.2		$\text{V}/\mu\text{s}$
$t_S$	Settling time	0.1%	$V_S = \pm 18\text{ V}$ , $G = 1$ , $10\text{-V}$ step	46		$\mu\text{s}$
		0.01%	$V_S = \pm 18\text{ V}$ , $G = 1$ , $10\text{-V}$ step	48		$\mu\text{s}$
$t_{OR}$	Overload recovery time	$V_{IN} \times G = V_S$		8		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	1 kHz, $G = +1$ , $V_{OUT} = 3.5\text{ V}_{RMS}$ , No Load		0.035%		
<b>OUTPUT</b>						
	Voltage output swing from rail	$V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ , No Load		5	15	$\text{mV}$
		$V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ , $R_L = 10\text{ k}\Omega$		75	100	
		$V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		100	125	
$I_{SC}$	Short-circuit current	$V_S = \pm 18\text{ V}$ , Sinking		-30		$\text{mA}$
		$V_S = \pm 18\text{ V}$ , Sourcing		+30		$\text{mA}$
$R_O$	Open-loop output resistance	$f = 550\text{ kHz}$ , $I_O = 0$ , See <a href="#">Figure 21</a>		1.4		$\text{k}\Omega$
$C_{LOAD}$	Capacitive load drive			See <a href="#">Typical Characteristics</a>		
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current (per amplifier)	$V_S = \pm 4\text{ V}$ to $V_S = \pm 18\text{ V}$		100	145	$\mu\text{A}$
		$I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				150

(1)  $V_S / 2 = \text{midsupply}$ .



## 6.8 Electrical Characteristics: Low-Voltage Operation

at  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 2.25\text{ V}$  to  $< \pm 4\text{ V}$  ( $V_S = +4.5\text{ V}$  to  $< +8\text{ V}$ ),  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2^{(1)}$ , and  $V_{CM} = V_{OUT} = V_S / 2^{(1)}$  (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage			$\pm 1$	$\pm 15$	$\mu\text{V}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.001$	$\pm 0.015$	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4.5\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.01$	$\pm 1$	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{CM} = V_S / 2$		$\pm 100$	$\pm 350$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 5$	$\text{nA}$
$I_{OS}$	Input offset current			$\pm 100$	$\pm 500$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 5$	$\text{nA}$
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.4		$\mu\text{V}_{PP}$
		$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		60		$\text{nV}_{RMS}$
	Input voltage noise density	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		160		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range		$(V-) - 0.1$		$(V+) - 2$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ , $V_S = \pm 2.25\text{ V}$	114	130		$\text{dB}$
		$(V-) < V_{CM} < (V+) - 2\text{ V}$ , $V_S = \pm 2.25\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	120	137		$\text{dB}$
<b>INPUT IMPEDANCE</b>						
$Z_{ID}$	Differential			$100 \parallel 6$		$\text{M}\Omega \parallel \text{pF}$
$Z_{IC}$	Common-mode			$6 \parallel 4.2$		$10^{12}\ \Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_S = \pm 2.25\text{ V}$ to $\pm 4\text{ V}$ , $(V-) + 0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$ , $R_L = 10\text{ k}\Omega$	120	140		$\text{dB}$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product			550		$\text{kHz}$
SR	Slew rate	$V_O = 1\text{-V}$ step, $G = +1$		0.2		$\text{V}/\mu\text{s}$
$t_{OR}$	Overload recovery time	$V_{IN} \times G = V_S$		8		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	1 kHz, $G = +1$ , $V_{OUT} = 1\text{ V}_{RMS}$ , No Load		0.05%		
<b>OUTPUT</b>						
	Voltage output swing from rail	$V_S = \pm 2.25\text{ V}$ to $\pm 4\text{ V}$ , No Load		5	15	$\text{mV}$
		$V_S = \pm 2.25\text{ V}$ to $\pm 4\text{ V}$ , $R_L = 10\text{ k}\Omega$		15	25	
		$V_S = \pm 2.25\text{ V}$ to $\pm 4\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		15	30	
$I_{SC}$	Short-circuit current	$V_S = \pm 2.25$ , Sinking		-20		$\text{mA}$
		$V_S = \pm 2.25$ , Sourcing		+20		$\text{mA}$
$R_O$	Open-loop output resistance	$f = 550\text{ kHz}$ , $I_O = 0$ , See <a href="#">Figure 21</a>		1.4		$\text{k}\Omega$
$C_{LOAD}$	Capacitive load drive		See <a href="#">Typical Characteristics</a>			
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current (per amplifier)	$V_S = \pm 2.25\text{ V}$ to $V_S = \pm 4\text{ V}$		100	145	$\mu\text{A}$
		$I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			150	$\mu\text{A}$

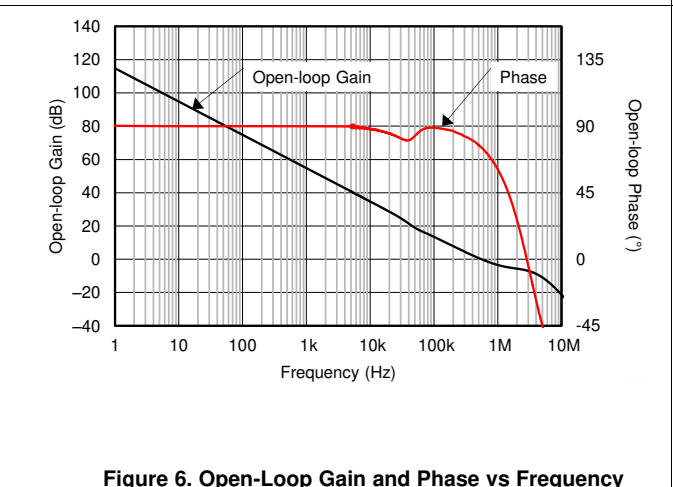
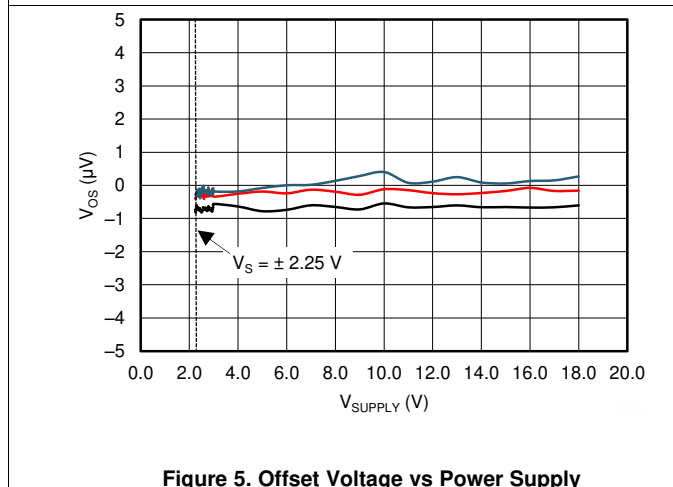
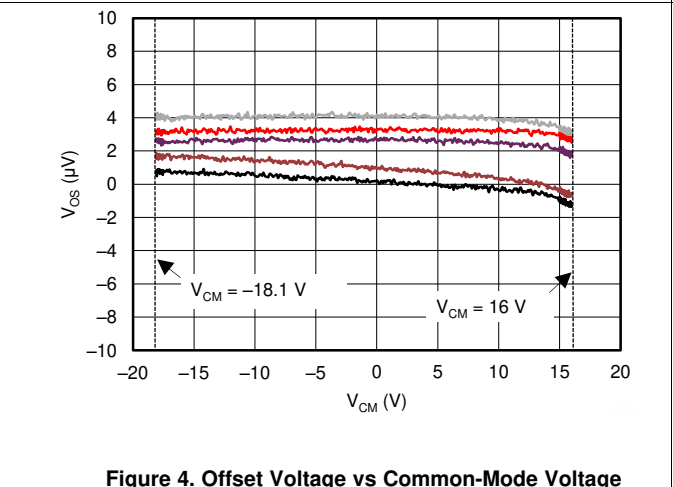
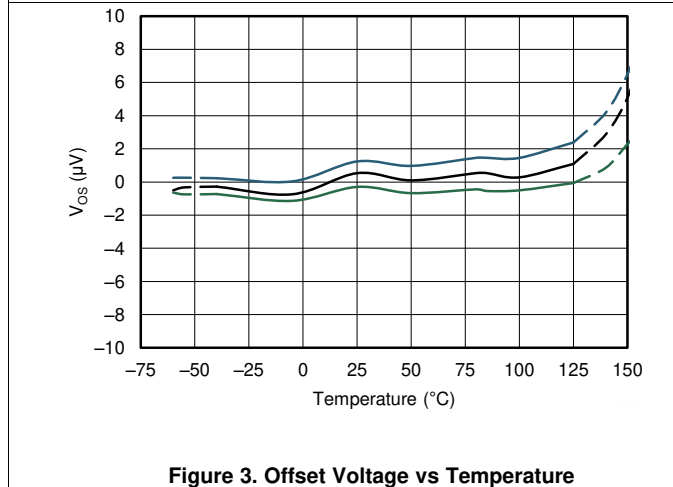
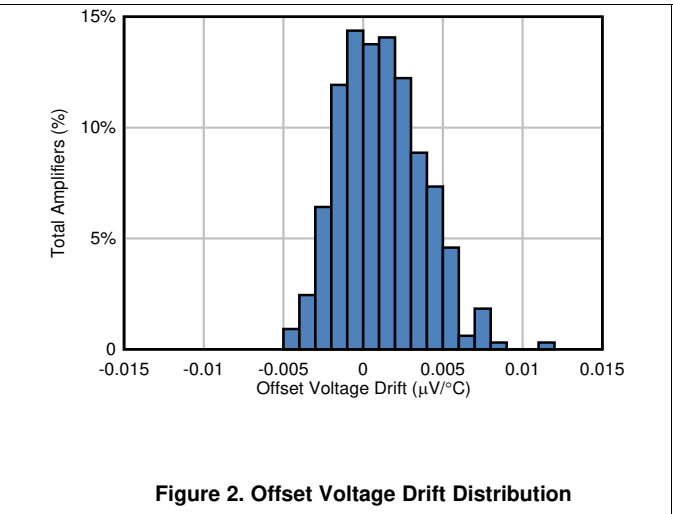
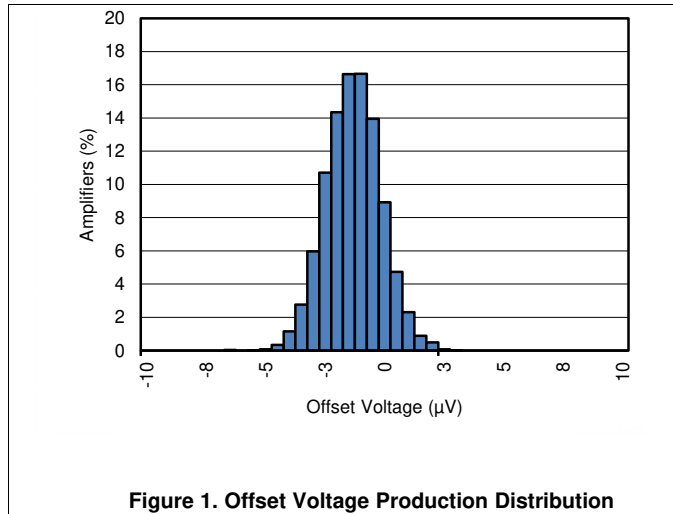
(1)  $V_S / 2 = \text{midsupply}$ .

## 6.9 Typical Characteristics

**Table 1. Typical Characteristic Graphs**

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	<a href="#">Figure 1</a>
Offset Voltage Drift Distribution	<a href="#">Figure 2</a>
Offset Voltage vs Temperature	<a href="#">Figure 3</a>
Offset Voltage vs Common-Mode Voltage	<a href="#">Figure 4</a>
Offset Voltage vs Power Supply	<a href="#">Figure 5</a>
Open-Loop Gain and Phase vs Frequency	<a href="#">Figure 6</a>
Closed-Loop Gain vs Frequency	<a href="#">Figure 7</a>
$I_B$ vs Common-Mode Voltage	<a href="#">Figure 8</a>
Input Bias Current vs Temperature	<a href="#">Figure 9</a>
Output Voltage Swing vs Output Current	<a href="#">Figure 10</a>
CMRR and PSRR vs Frequency (Referred-to-Input)	<a href="#">Figure 11</a>
CMRR vs Temperature	<a href="#">Figure 12</a>
PSRR vs Temperature	<a href="#">Figure 13</a>
0.1-Hz to 10-Hz Noise	<a href="#">Figure 14</a>
Input Voltage Noise Spectral Density vs Frequency	<a href="#">Figure 15</a>
THD+N Ratio vs Frequency	<a href="#">Figure 16</a>
THD+N vs Output Amplitude	<a href="#">Figure 17</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 18</a>
Quiescent Current vs Temperature	<a href="#">Figure 19</a>
Open-Loop Gain vs Temperature	<a href="#">Figure 20</a>
Open-Loop Output Impedance vs Frequency	<a href="#">Figure 21</a>
Small-Signal Overshoot vs Capacitive Load ( $G = 1$ ) (10-mV Output Step)	<a href="#">Figure 22</a>
No Phase Reversal	<a href="#">Figure 23</a>
Positive Overload Recovery	<a href="#">Figure 24</a>
Negative Overload Recovery	<a href="#">Figure 25</a>
Small-Signal Step Response (10 mV)	<a href="#">Figure 26</a> , <a href="#">Figure 27</a>
Large-Signal Step Response	<a href="#">Figure 28</a> , <a href="#">Figure 29</a>
Large-Signal Settling Time (10-V Positive Step)	<a href="#">Figure 30</a>
Large-Signal Settling Time (10-V Negative Step)	<a href="#">Figure 31</a>
Short-Circuit Current vs Temperature	<a href="#">Figure 32</a>
Maximum Output Voltage vs Frequency	<a href="#">Figure 33</a>
Crosstalk vs Frequency	<a href="#">Figure 34</a>
EMIRR IN+ vs Frequency	<a href="#">Figure 35</a>

at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

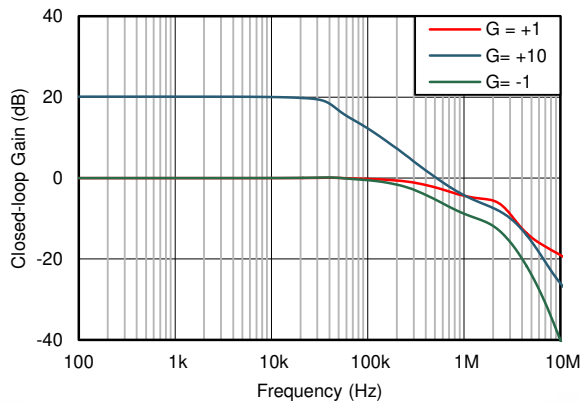


Figure 7. Closed-Loop Gain vs Frequency

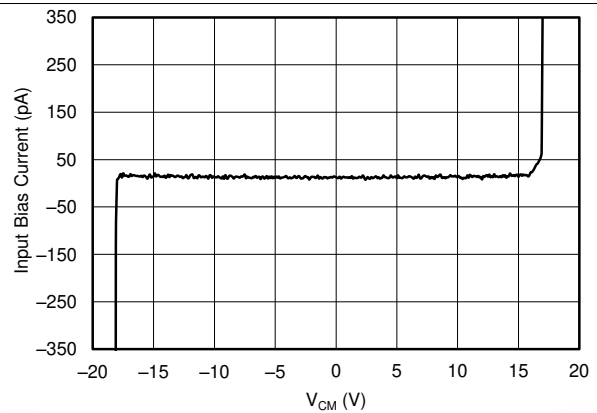


Figure 8.  $I_B$  vs Common-Mode Voltage

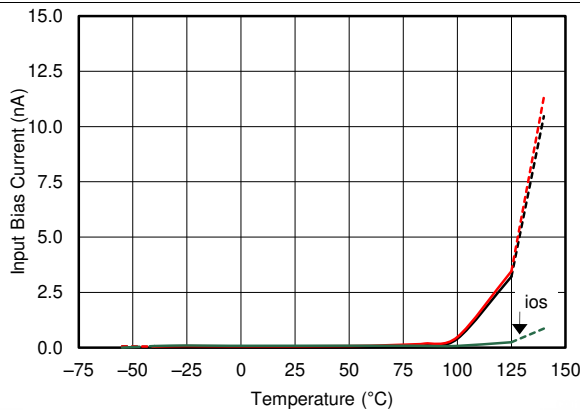


Figure 9. Input Bias Current vs Temperature

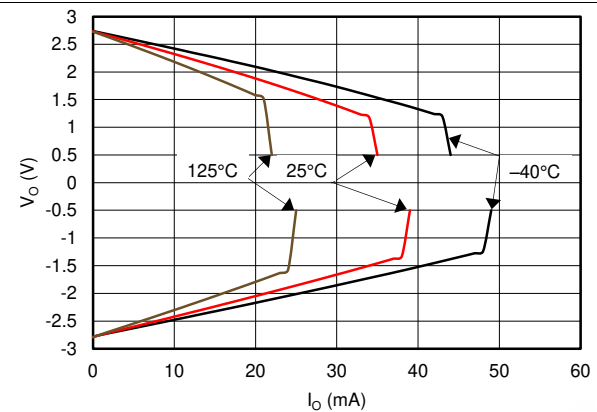


Figure 10. Output Voltage Swing vs Output Current

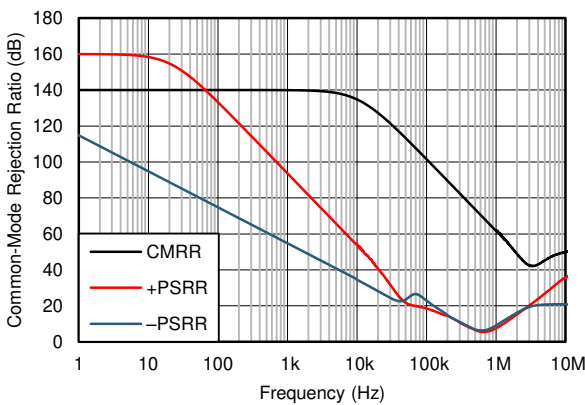


Figure 11. CMRR and PSRR vs Frequency (Referred-to-Input)

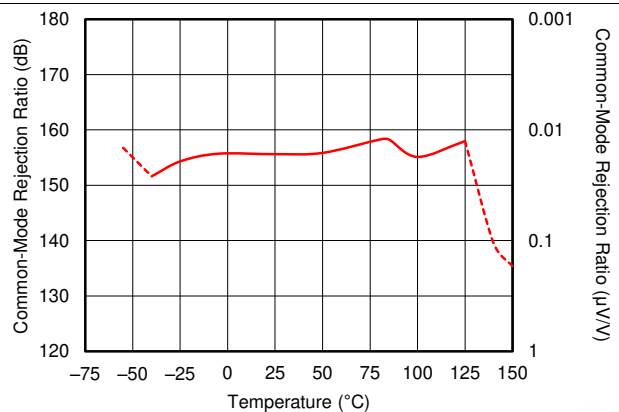
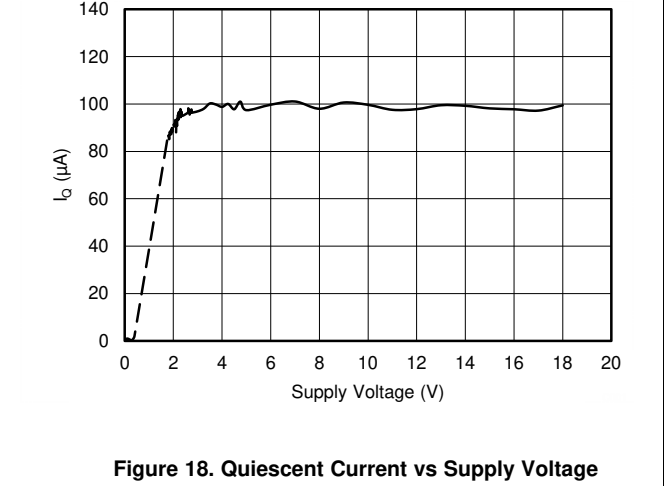
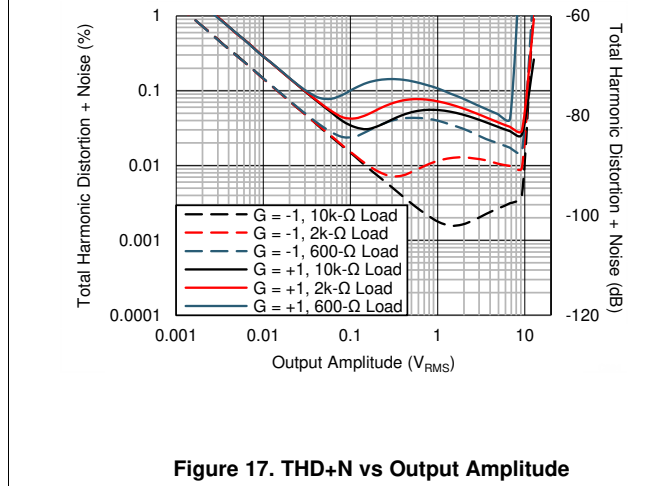
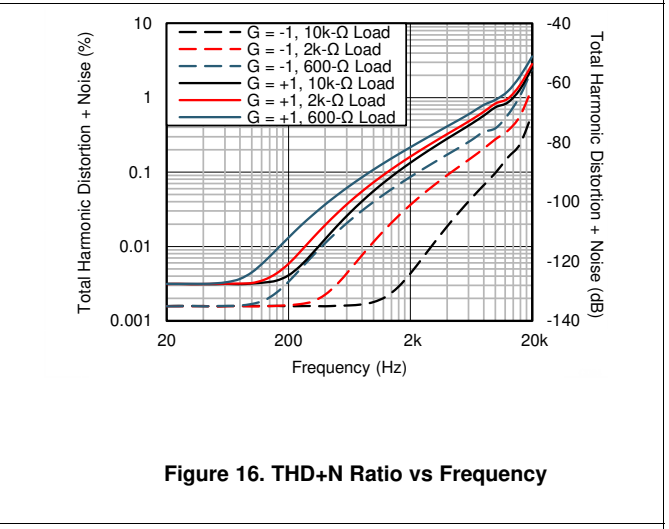
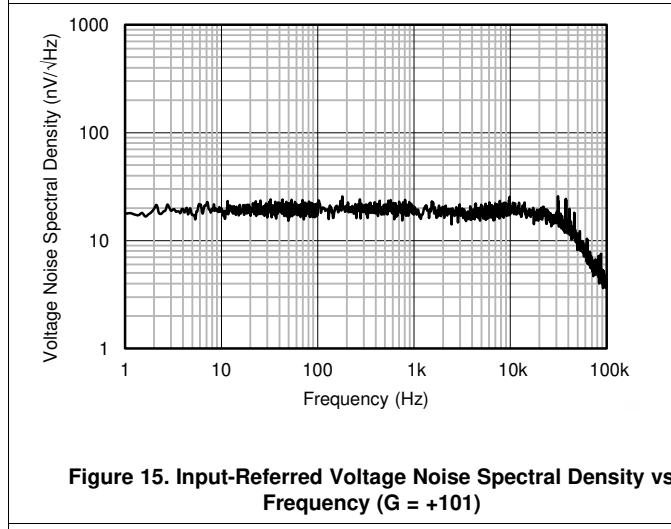
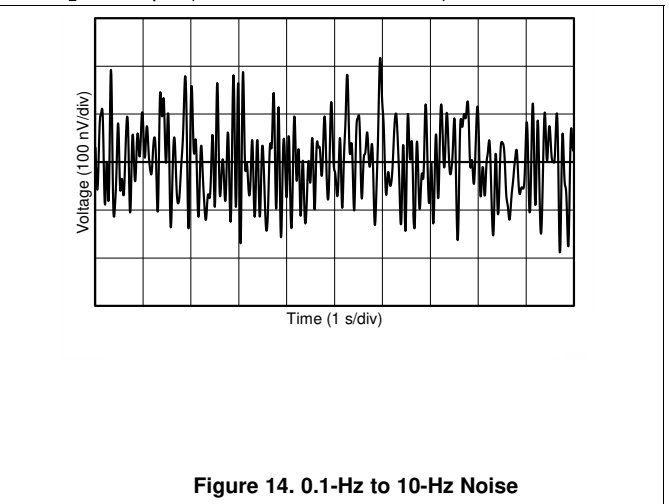
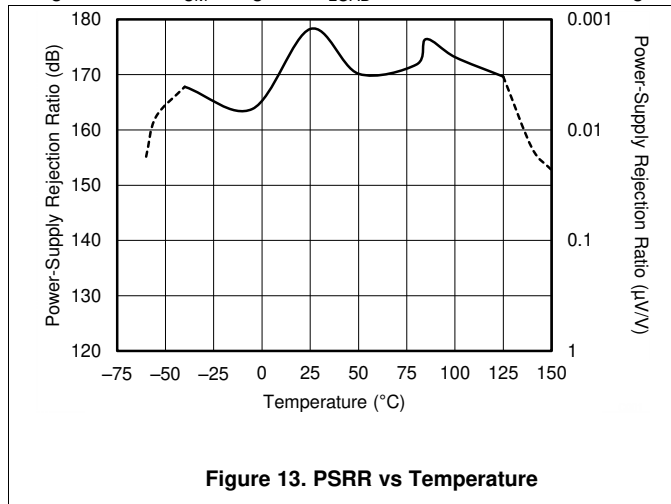


Figure 12. CMRR vs Temperature

at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

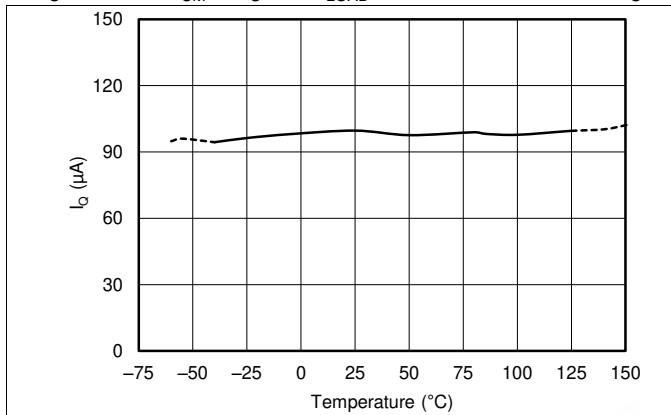


Figure 19. Quiescent Current vs Temperature

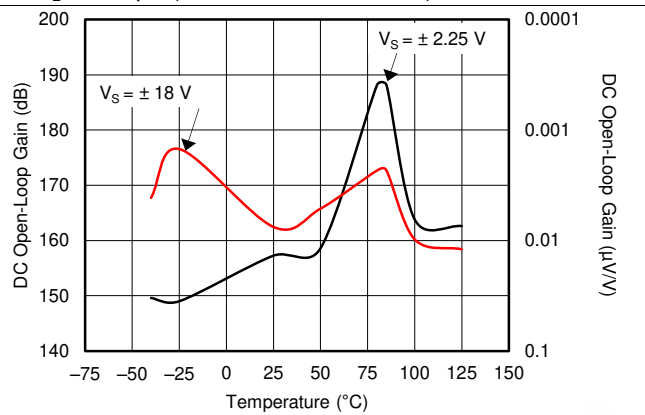


Figure 20. Open-Loop Gain vs Temperature

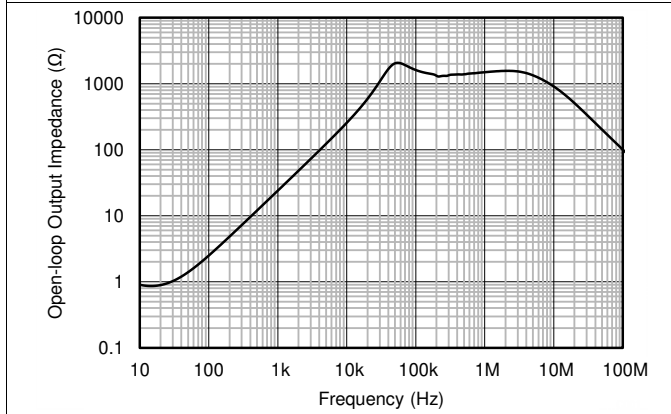


Figure 21. Open-Loop Output Impedance vs Frequency

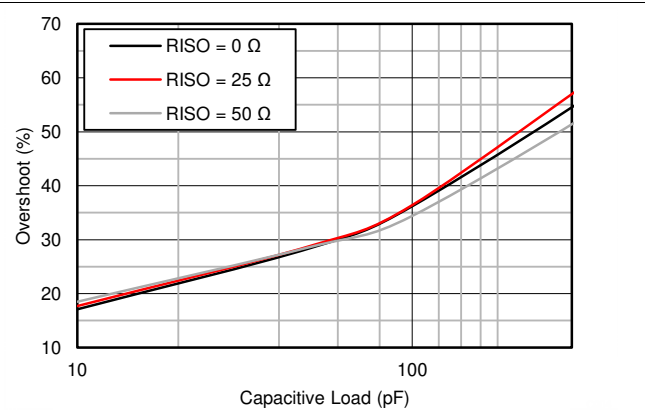


Figure 22. Small-Signal Overshoot vs Capacitive Load ( $G = +1$ ) (10-mV Output Step)

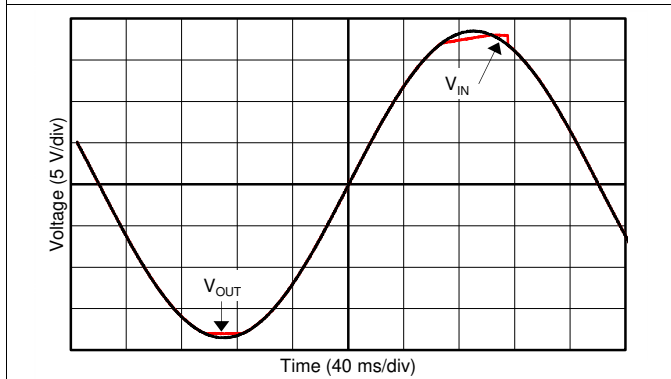


Figure 23. No Phase Reversal

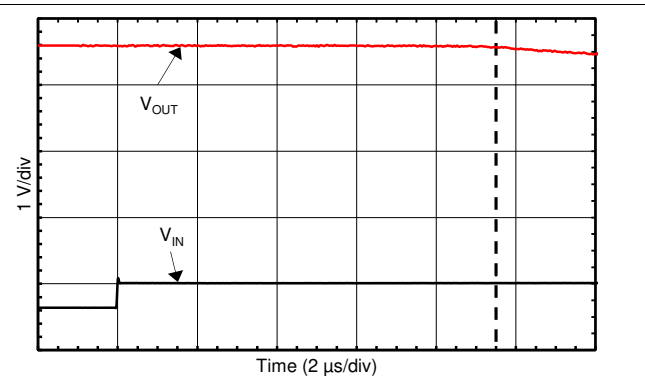
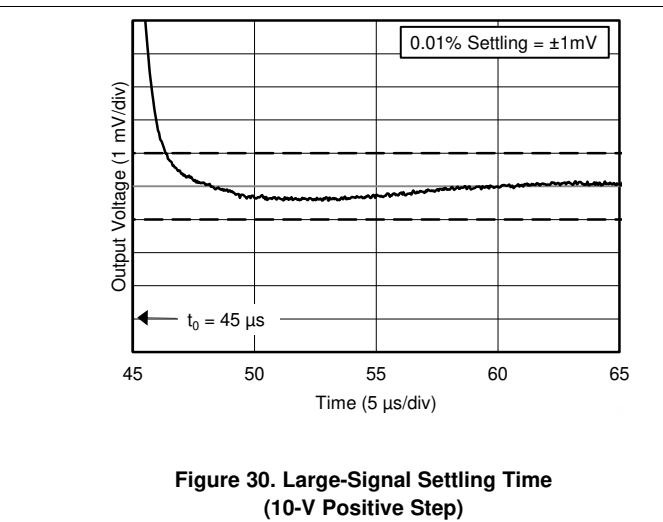
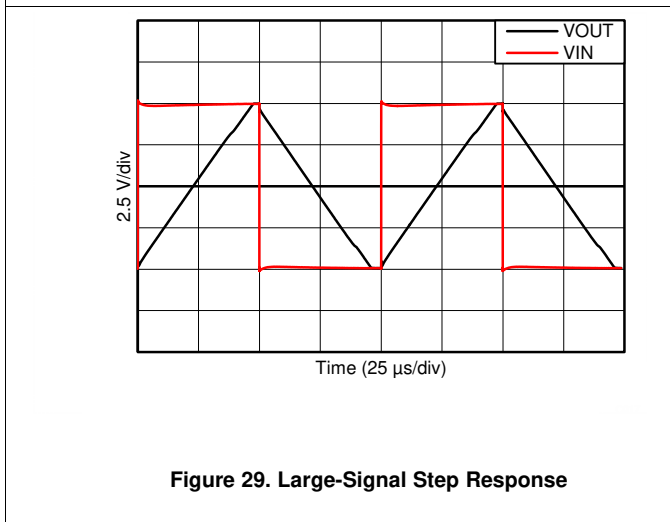
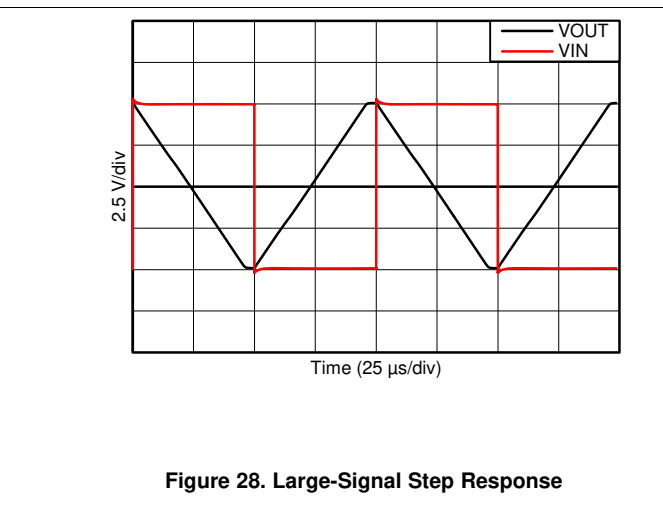
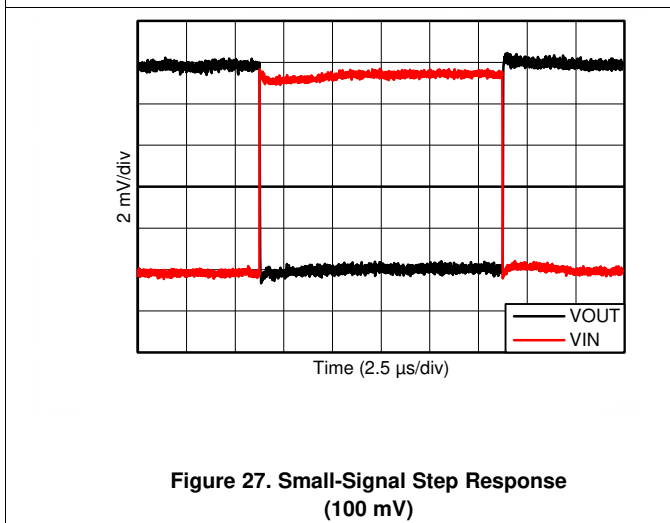
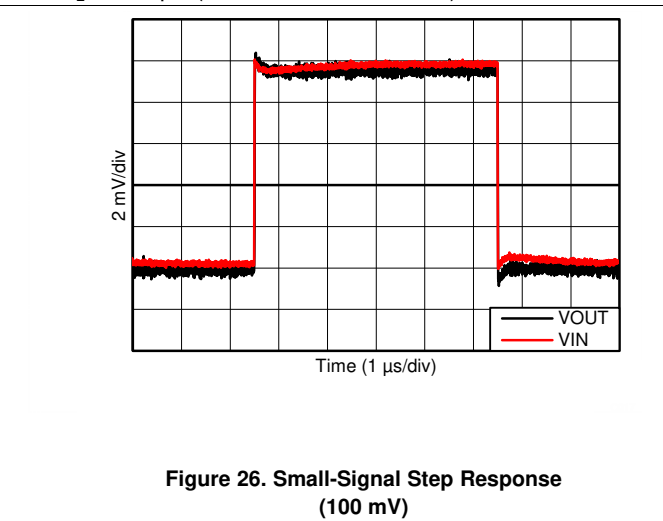
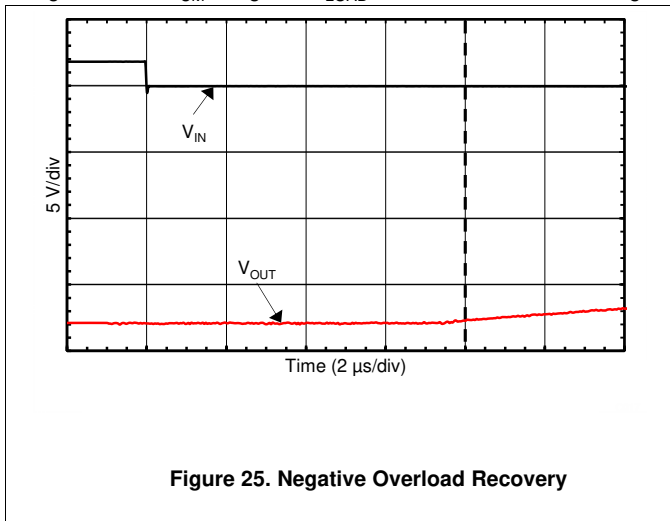


Figure 24. Positive Overload Recovery

at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

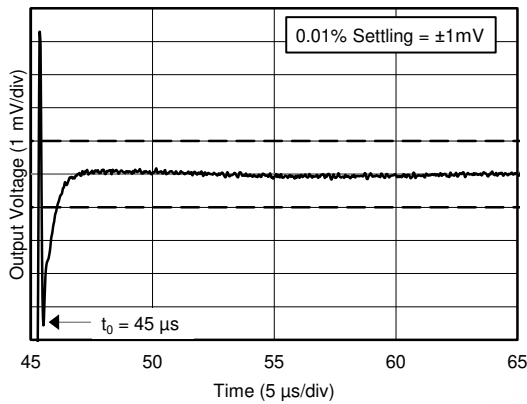


Figure 31. Large-Signal Settling Time (10-V Negative Step)

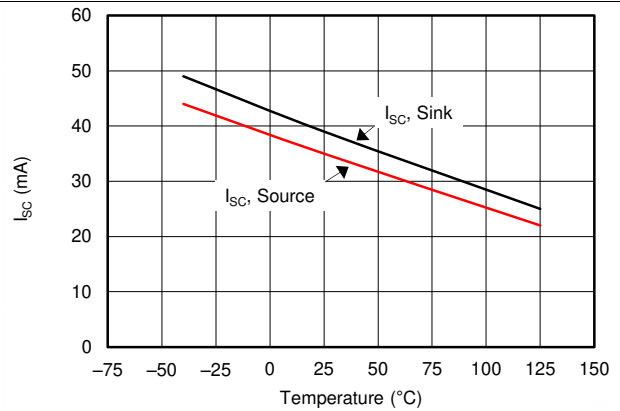


Figure 32. Short-Circuit Current vs Temperature

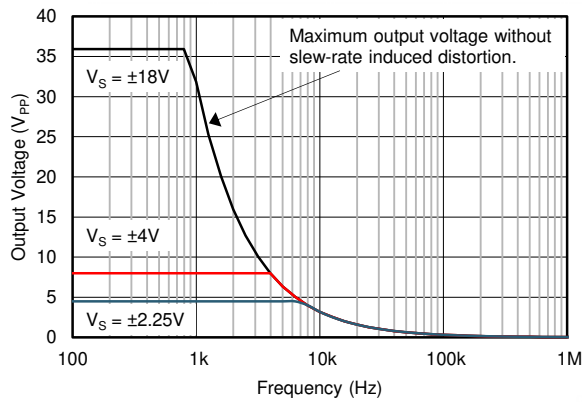


Figure 33. Maximum Output Voltage vs Frequency

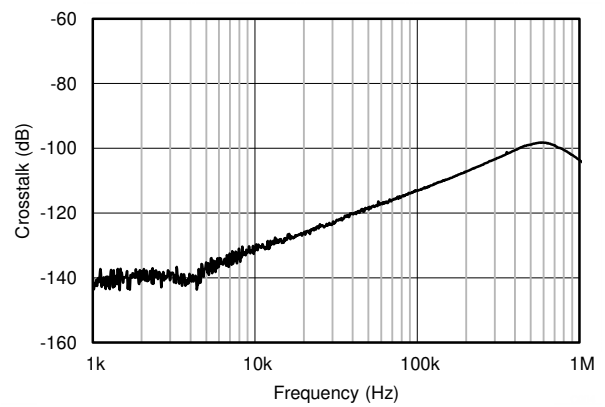


Figure 34. Crosstalk vs Frequency

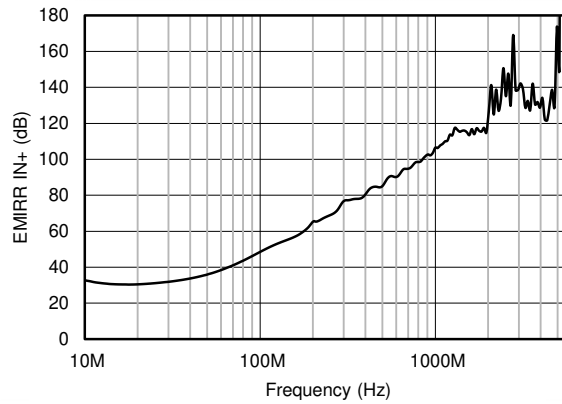


Figure 35. EMIRR IN+ vs Frequency



## 7 Detailed Description

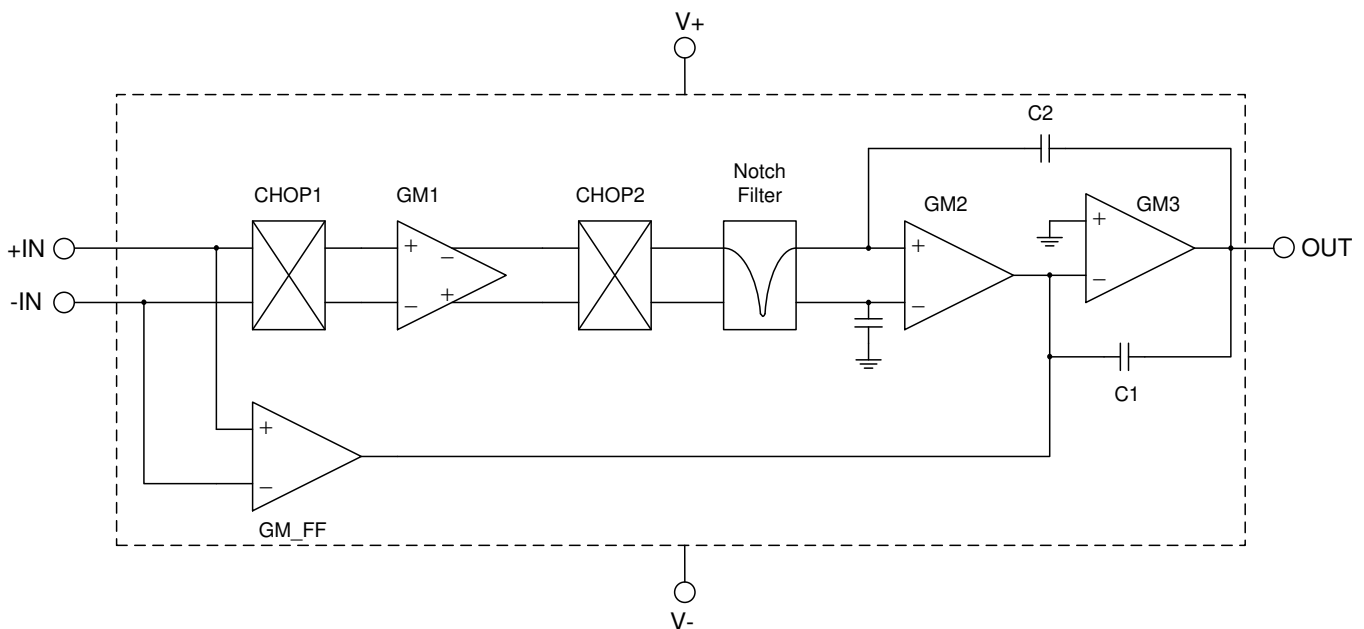
### 7.1 Overview

The OPA187, OPA2187, and OPA4187 (OPAx187) operational amplifiers combine precision offset and drift with excellent overall performance, making these devices an excellent choice for many precision applications. The precision offset drift of only  $0.001 \mu\text{V}/^\circ\text{C}$  provides stability over the entire temperature range. In addition, these devices offer excellent overall performance with high CMRR, PSRR, and  $A_{OL}$ . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases,  $0.1\text{-}\mu\text{F}$  capacitors are adequate.

The OPAx187 is part of a family of zero-drift, low-power, rail-to-rail output operational amplifiers. These devices operate from  $4.5\text{ V}$  to  $36\text{ V}$ , are unity-gain stable, and are designed for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low input offset voltage, and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise and zero flicker noise.

### 7.2 Functional Block Diagram

The functional block diagram shows a representation of the proprietary OPAx187 architecture. Functional blocks CHOP1 and CHOP2 operate such that the non-idealities of GM1 are cancelled while the input signal is left in-phase. The integrated notch filter of the OPAx187 family suppresses most of the auto-zero amplifier carrier.



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## 7.3 Feature Description

The OPAx187 are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary, periodic autocalibration technique to provide ultra-low input offset voltage and near zero input offset voltage drift over temp and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure they are equal on both input pins. Other layout and design considerations include:

Use low thermoelectric-coefficient conditions (avoid dissimilar metals).

Thermally isolate components from power supplies or other heat sources.

Shield operational amplifier and input circuitry from air currents, such as cooling fans.

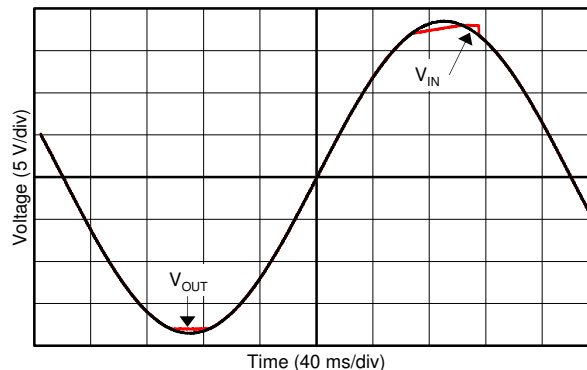
Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1  $\mu\text{V}/^\circ\text{C}$  or higher, depending on the materials used.

### 7.3.1 Operating Characteristics

The OPAx187 are specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V). Many specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

### 7.3.2 Phase-Reversal Protection

The OPAx187 have an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx187 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. [Figure 36](#) shows this performance.



**Figure 36. No Phase Reversal**

### 7.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers, such as the OPAx187, use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. An extremely short duration prevents these pulses from being amplified; however, the pulses may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

### 7.3.4 Internal Offset Correction

The OPAx187 op amps use an auto-calibration technique with a time-continuous 125-kHz op amp in the signal path. This amplifier is zero-corrected every 22  $\mu\text{s}$  using a proprietary technique. At power-up, the amplifier requires approximately 100  $\mu\text{s}$  to achieve the specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

## Feature Description (continued)

### 7.3.5 EMI Rejection

The OPAx187 devices use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx187 benefit from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 37](#) shows the results of this testing on the OPAx187. [Table 2](#) lists the EMIRR IN+ values for the OPAx187 at particular frequencies commonly encountered in real-world applications. Applications listed in [Table 2](#) may be centered on or operated near the particular frequency shown. Detailed information can also be found in the [EMI Rejection Ratio of Operational Amplifiers application report](#), available for download from [www.ti.com](http://www.ti.com).

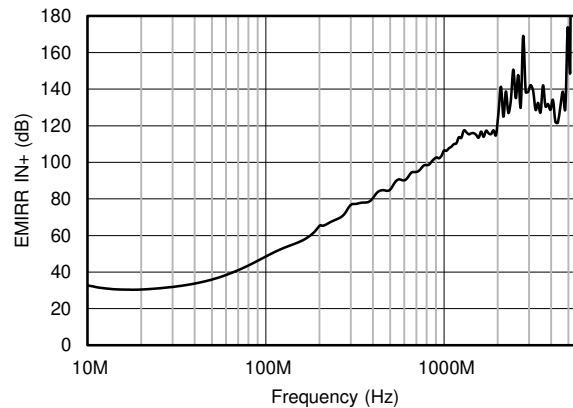


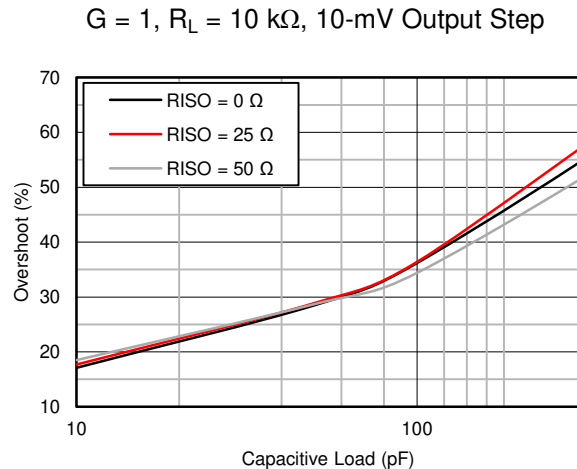
Figure 37. EMIRR Testing

Table 2. OPAx187 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	81.8 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	102.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	115.4 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	150.7 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	142.0 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	173.8 dB

### 7.3.6 Capacitive Load and Stability

The dynamic characteristics of the OPAx187 are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example,  $R_{OUT}$  equal to 50  $\Omega$ ) in series with the output. [Figure 38](#) illustrates small-signal overshoot versus capacitive load for several values of  $R_{OUT}$ . Also, for details of analysis techniques and application circuits, refer to the [Feedback Plots Define Op Amp AC Performance application report](#), available for download from [www.ti.com](http://www.ti.com).



**Figure 38. Small-Signal Overshoot vs Capacitive Load**

### 7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See [Figure 39](#) for an illustration of the ESD circuits contained in the OPAx187 (indicated by the dashed-line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the op amp. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the op amp core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPAx187, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

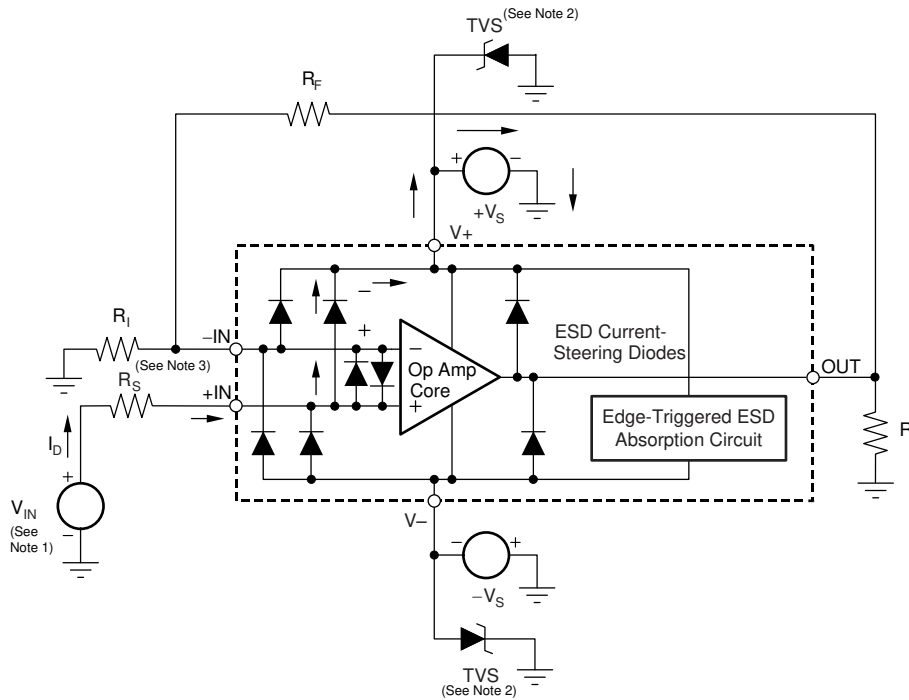
When the operational amplifier connects into a circuit (see [Figure 39](#)), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths, and rarely involves the absorption device.

[Figure 39](#) shows a specific example where the input voltage ( $V_{IN}$ ) exceeds the positive supply voltage ( $+V_S$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $+V_S$  can sink the current, one of the upper input steering diodes conducts and directs current to  $+V_S$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data-sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while power supply  $+V_S$  or  $-V_S$  is at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level less than the input signal amplitude. If the supplies are high impedance, then the operational amplifier supply current may be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external transient voltage suppressor (TVS) diodes to the supply pins, as shown in Figure 39. Select the TVS voltage so that the diode does not turn on during normal operation. However, make sure that the TVS voltage is low enough so that the TVS diode conducts if the supply pin exceeds the safe operating supply voltage level.



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NOTE 1:  $V_{IN} = +V_S + 500 \text{ mV}$ .

NOTE 2: TVS:  $+V_{S(max)} > V_{TVSBR (min)} > +V_S$ .

NOTE 3: Suggested value is approximately 1 k $\Omega$ .

**Figure 39. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

The OPAx187 input pins are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 39. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or  $G = 1$  circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPAx187. Figure 39 shows an example configuration that implements a current-limiting feedback resistor.

## 7.4 Device Functional Modes

The OPAx187 have a single functional mode and are operational when the power-supply voltage is greater than 4.5 V ( $\pm 0.25$  V). The maximum power supply voltage for the OPAx187 is 36 V ( $\pm 18$  V).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

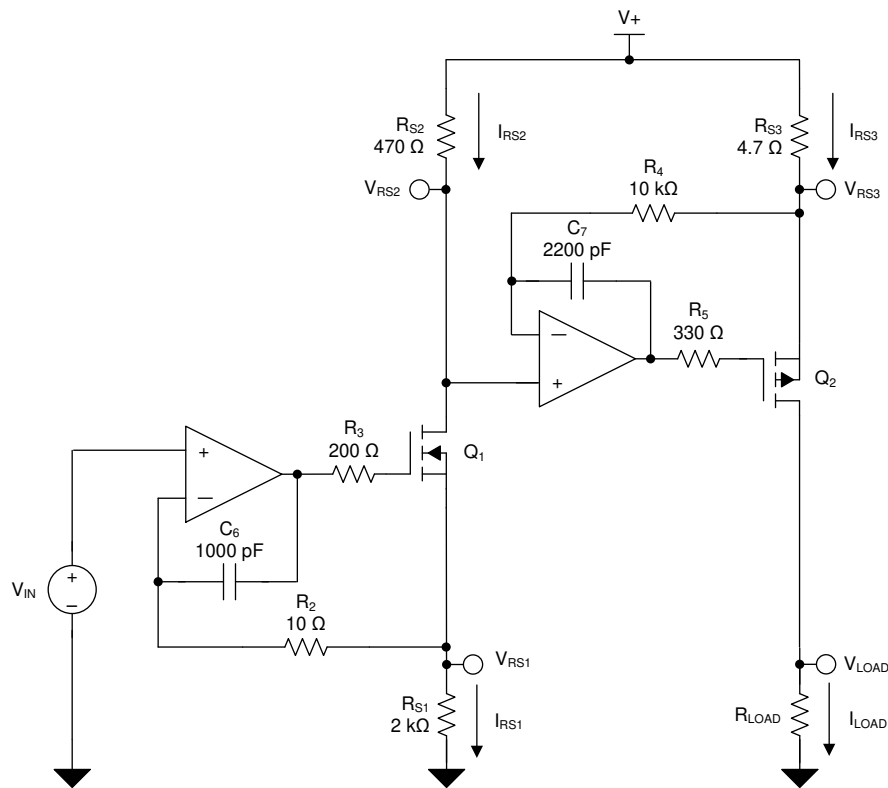
The OPAx187 operational amplifier family combines precision offset and drift with excellent overall performance, making this device an excellent choice for many precision applications. The precision offset drift of only  $0.001 \mu\text{V}/^\circ\text{C}$  provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and  $A_{OL}$  dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases,  $0.1\text{-}\mu\text{F}$  capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx187 can be used.

### 8.2 Typical Applications

#### 8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in [Figure 40](#) is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V into an output current of 0 mA to 100 mA. [Figure 41](#) shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2187 facilitate excellent dc accuracy for the circuit.



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**Figure 40. High-Side Voltage-to-Current (V-I) Converter**

## Typical Applications (continued)

### 8.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

### 8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage,  $V_{IN}$ , and the three current sensing resistors,  $R_{S1}$ ,  $R_{S2}$ , and  $R_{S3}$ . The relationship between  $V_{IN}$  and  $R_{S1}$  determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between  $R_{S2}$  and  $R_{S3}$ .

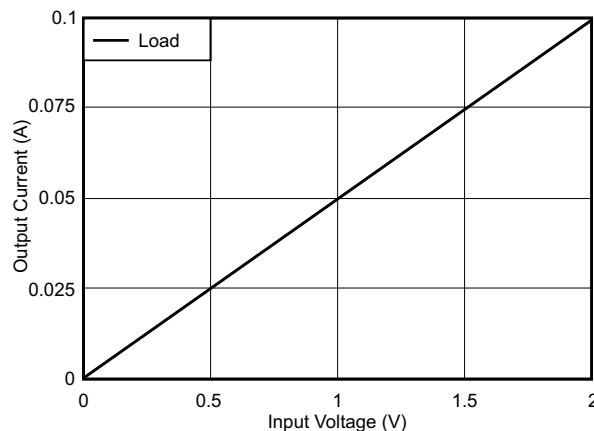
This application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPAx187 CMOS operational amplifiers are high-precision, ultra-low offset, ultra-low drift amplifier, optimized for wide-voltage, single-supply operation, with an output swing to within 5 mV of the positive rail. The OPAx187 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this device appropriate for precise dc control. The rail-to-rail output stage of the OPAx187 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, a step-by-step process to design a [High-Side Voltage-to-Current \(V-I\) Converter](#).

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIPD102, High-Side Voltage-to-Current \(V-I\) Converter](#).

### 8.2.1.3 Application Curve

Figure 41 shows the measured transfer function for the high-side voltage-to-current converter shown in Figure 40.



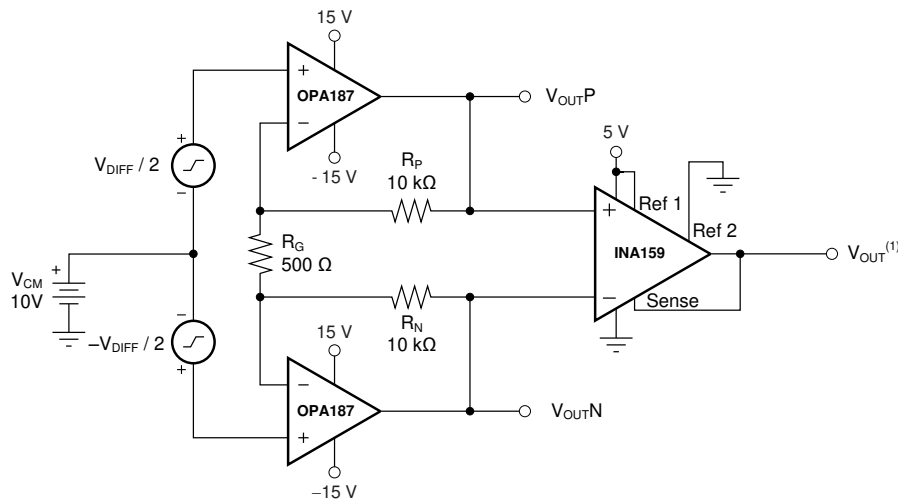
**Figure 41. Measured Transfer Function for High-Side V-I Converter**

## 8.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

### NOTE

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI web folder](#).

Figure 42 shows an example of how the OPA187 is used as a high-voltage, high-impedance front-end for a precision, discreet instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link to download the TINA-TI file: [Discrete INA](#).



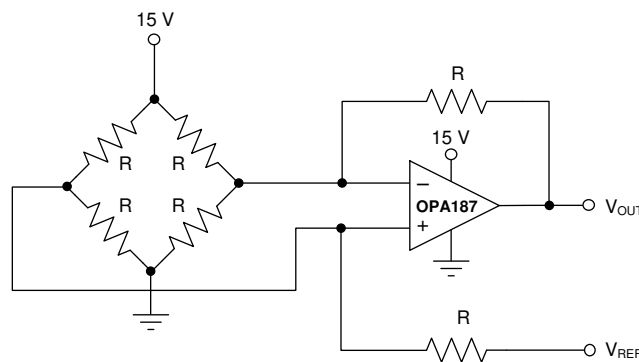
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$$(1) \quad V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref\ 1) / 2.$$

**Figure 42. Discrete INA + Attenuation for ADC With a 3.3-V Supply**

### 8.2.3 Bridge Amplifier

Figure 43 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: [Bridge Amplifier Circuit](#).



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**Figure 43. Bridge Amplifier**

### 8.2.4 Low-Side Current Monitor

Figure 44 shows the OPA187 configured in a low-side, current-sensing application. The load current ( $I_{LOAD}$ ) creates a voltage drop across the shunt resistor ( $R_{SHUNT}$ ). This voltage is amplified by the OPA187, with a gain of 201. The load current is set from 0 A to 500 mA, and corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: [Current-Sensing Circuit](#).



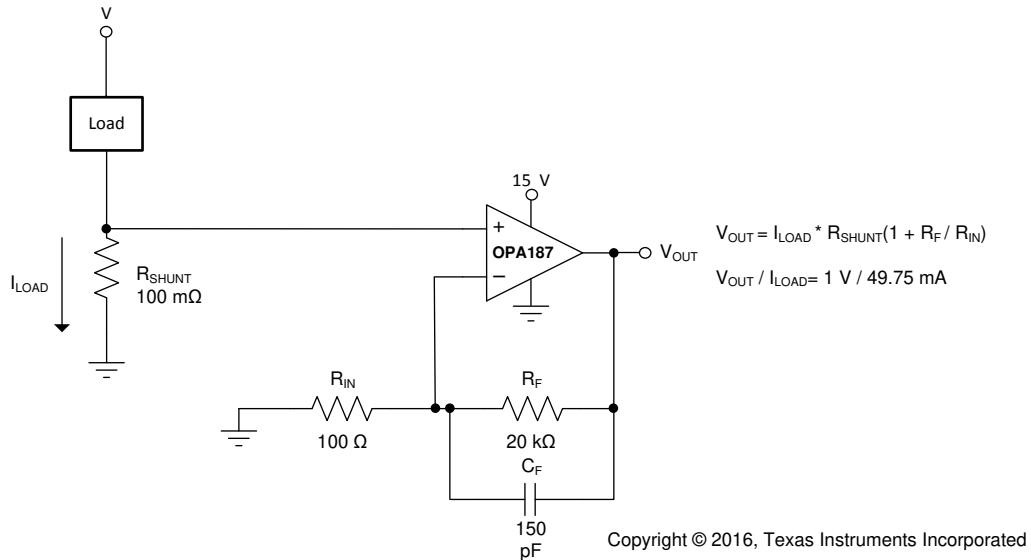


Figure 44. Low-Side Current Monitor

### 8.2.5 Programmable Power Supply

Figure 45 shows the OPA187 configured as a precision, programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPA187 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: [Programmable Power-Supply Circuit](#).

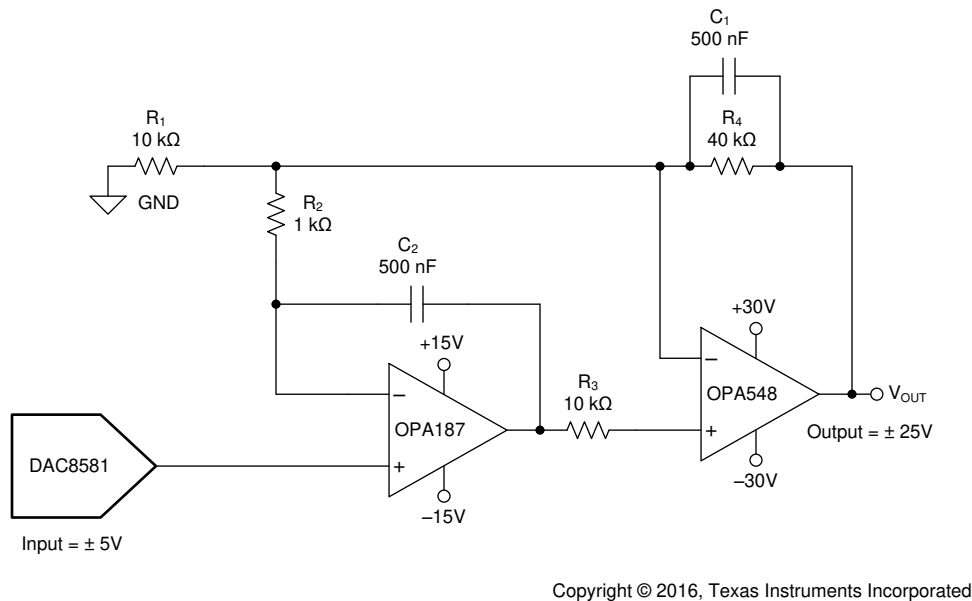
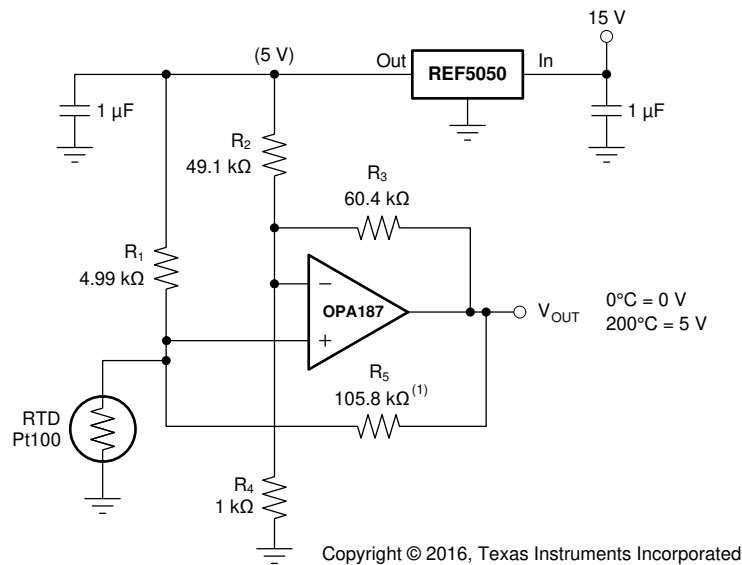


Figure 45. Programmable Power Supply

## 8.2.6 RTD Amplifier With Linearization

See the [Analog Linearization Of Resistance Temperature Detectors](#) technical brief, for an in-depth analysis of Figure 46. Click the following link to download the TINA-TI file: [RTD Amplifier With Linearization](#).



**Figure 46. RTD Amplifier With Linearization**

## 9 Power Supply Recommendations

The OPAx187 is specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . The [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

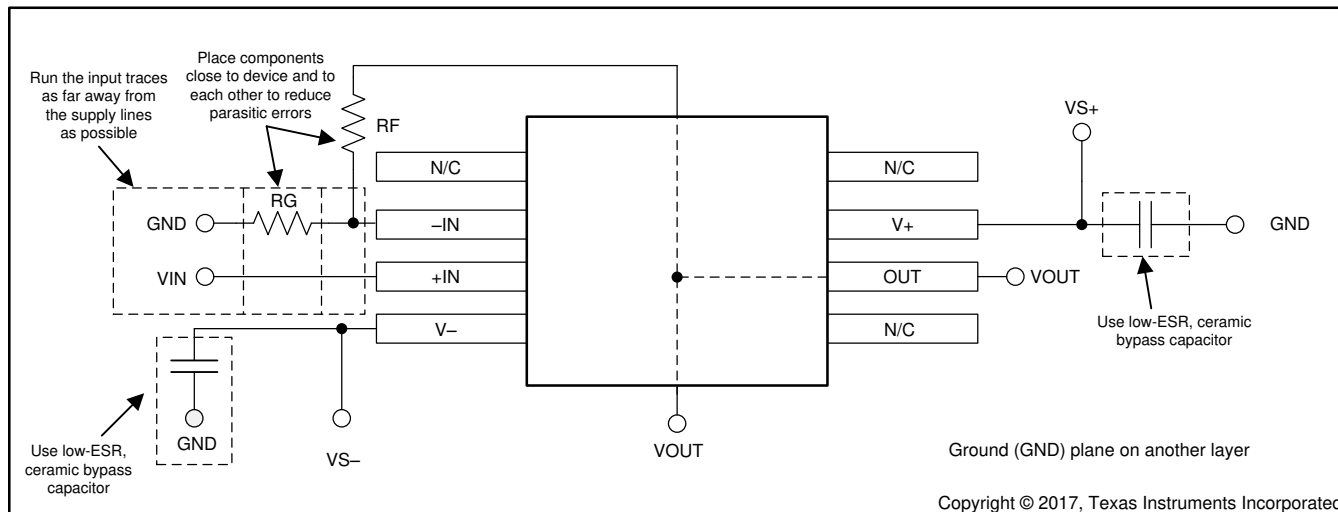
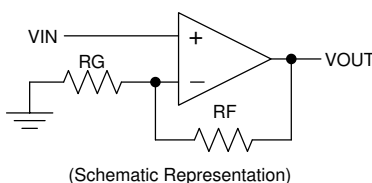
## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Low-ESR, 0.1- $\mu$ F ceramic bypass capacitors must be connected between each supply pin and ground; place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 10.2 Layout Example



**Figure 47. Layout Example**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models, in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that lets users format results various ways. Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

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##### 11.1.1.2 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts which offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

##### 11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets users create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH Design Center, [WEBENCH® Filter Designer](#) lets users design, optimize, and simulate complete multistage active filter solutions within minutes.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Operational Amplifier Gain Stability, Part 3: AC Gain-Error Analysis](#) technical brief
- Texas Instruments, [Operational Amplifier Gain Stability, Part 2: DC Gain-Error Analysis](#) technical brief
- Texas Instruments, [Using Infinite-Gain, MFB Filter Topology In Fully Differential Active Filters](#) technical brief
- Texas Instruments, [Op Amp Performance Analysis](#) application bulletin
- Texas Instruments, [Single-Supply Operation of Operational Amplifiers](#) application bulletin
- Texas Instruments, [Tuning in Amplifiers](#) application bulletin
- Texas Instruments, [Shelf-Life Evaluation of Lead-Free Component Finishes](#) application report

### 11.3 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE AND BUY	TECHNICAL DOCUMENTS	TOOLS AND SOFTWARE	SUPPORT AND COMMUNITY
OPA187	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA2187	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA4187	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on the *Alert me* button to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document

### 11.5 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.6 Trademarks

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 Bluetooth is a registered trademark of Bluetooth SIG, Inc.  
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 All other trademarks are the property of their respective owners.

### 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA187ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA187	<a href="#">Samples</a>
OPA187IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CUV	<a href="#">Samples</a>
OPA187IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CUV	<a href="#">Samples</a>
OPA187IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-2-260C-1 YEAR	-40 to 125	1D96	<a href="#">Samples</a>
OPA187IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG   SN	Level-2-260C-1 YEAR	-40 to 125	1D96	<a href="#">Samples</a>
OPA187IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA187	<a href="#">Samples</a>
OPA2187ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2187	<a href="#">Samples</a>
OPA2187IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16TV	<a href="#">Samples</a>
OPA2187IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16TV	<a href="#">Samples</a>
OPA2187IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2187	<a href="#">Samples</a>
OPA4187ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	<a href="#">Samples</a>
OPA4187IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	<a href="#">Samples</a>
OPA4187IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	<a href="#">Samples</a>
OPA4187IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	<a href="#">Samples</a>
OPA4187IRUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4187	<a href="#">Samples</a>
OPA4187IRUMT	ACTIVE	WQFN	RUM	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4187	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

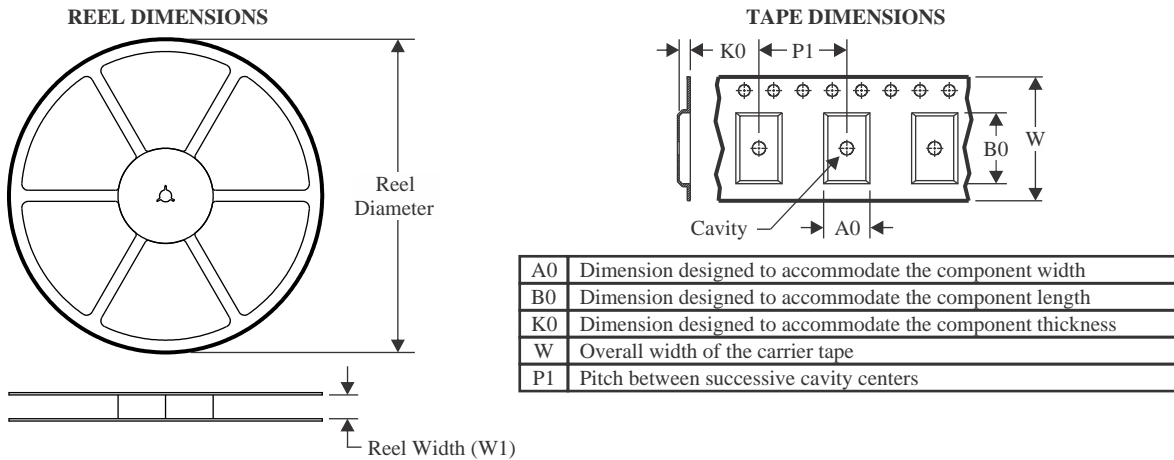
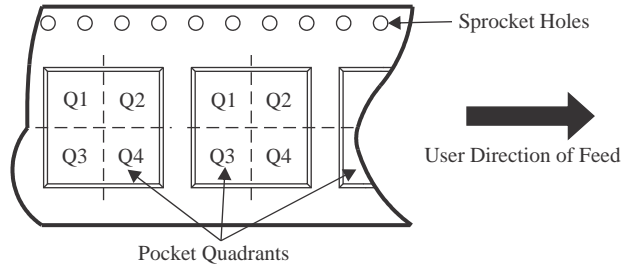
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA187IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA187IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA187IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA187IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA187IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2187IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2187IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2187IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4187IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4187IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4187IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA4187IRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA187IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA187IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA187IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA187IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA187IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2187IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2187IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2187IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4187IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4187IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4187IRUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
OPA4187IRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA187ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2187ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4187ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4187IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

## GENERIC PACKAGE VIEW

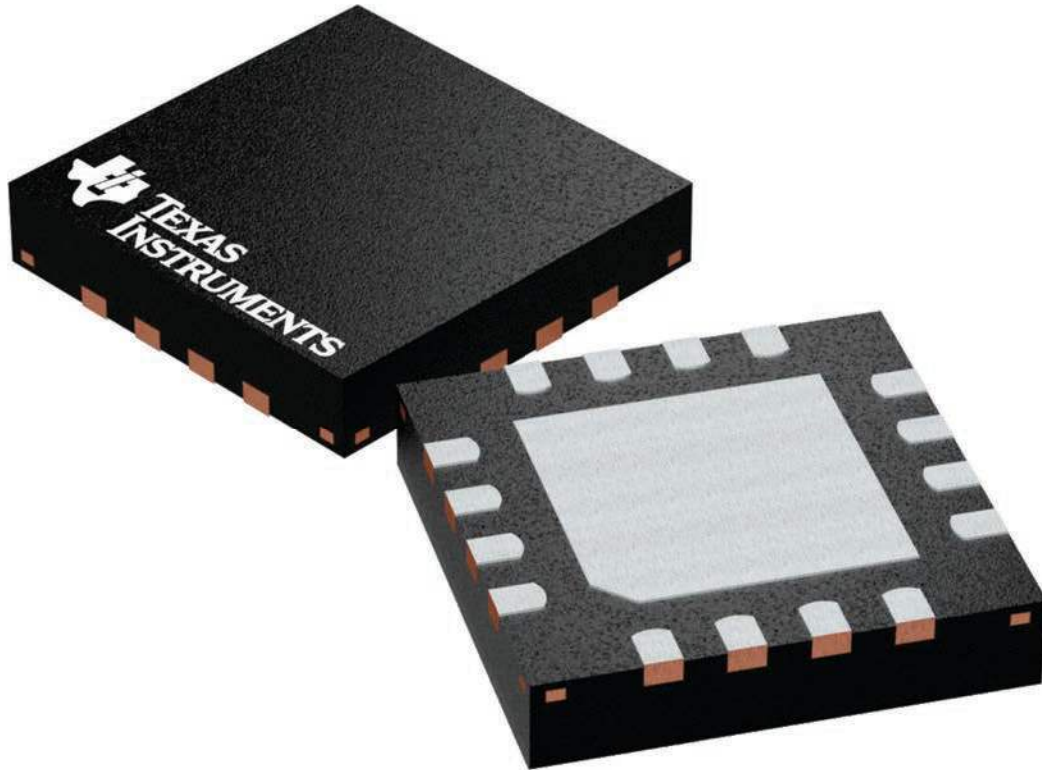
**RUM 16**

**WQFN - 0.8 mm max height**

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224843/A

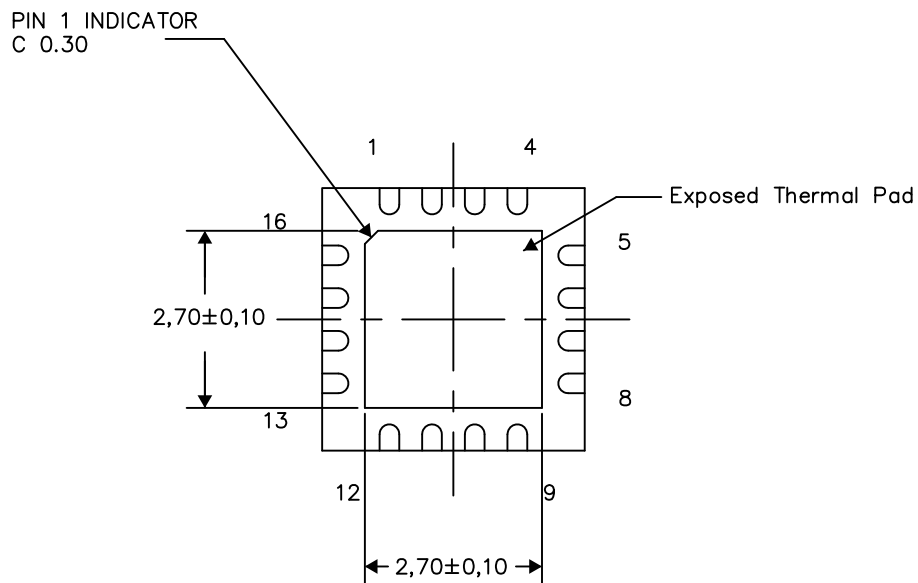


**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

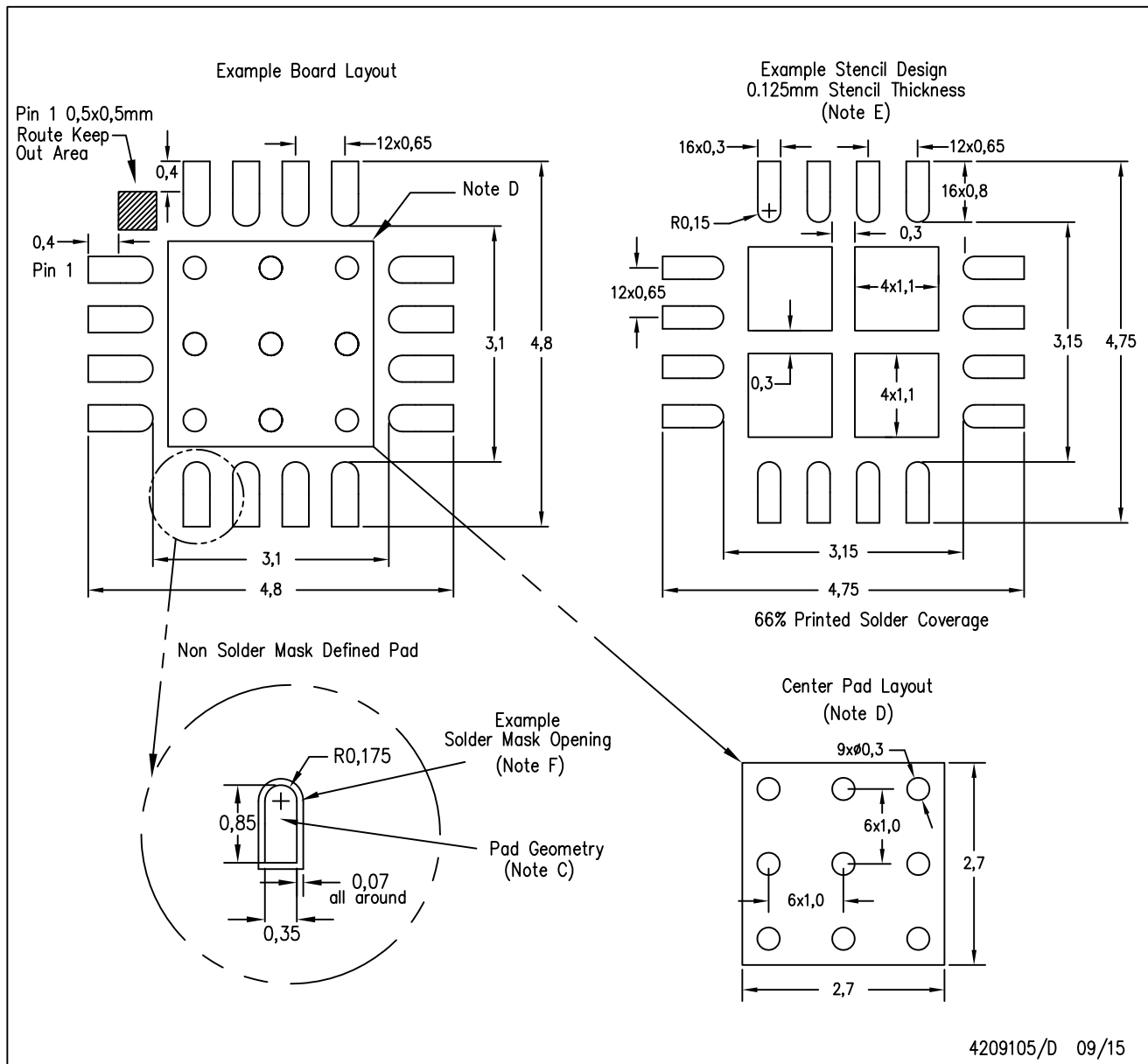
Exposed Thermal Pad Dimensions

4209093-2/F 09/15

NOTES: All linear dimensions are in millimeters

RUM (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

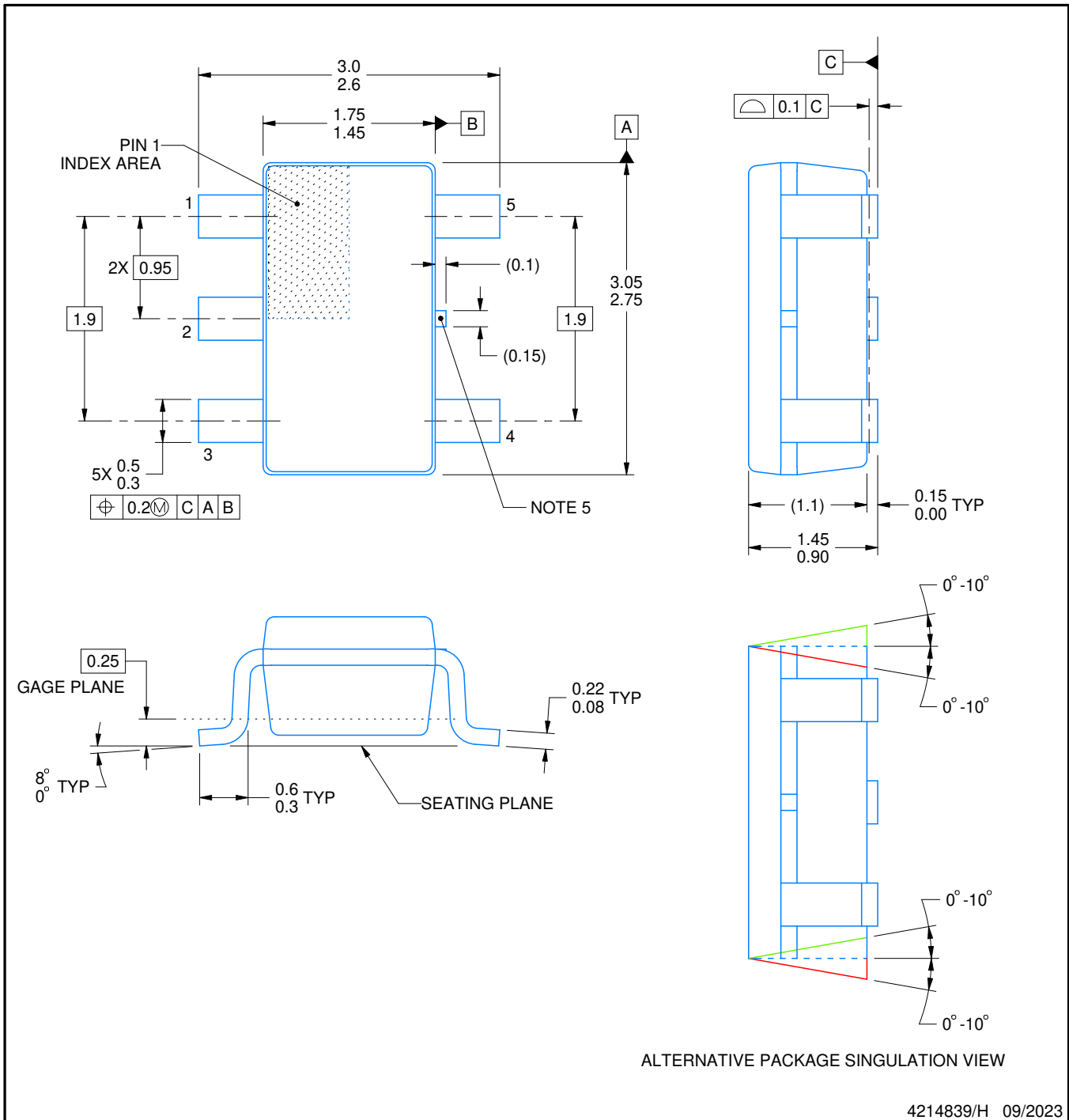
# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



**NOTES:**

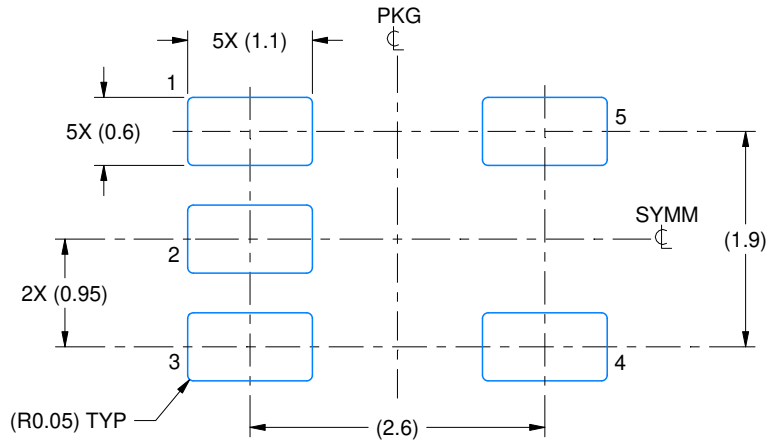
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

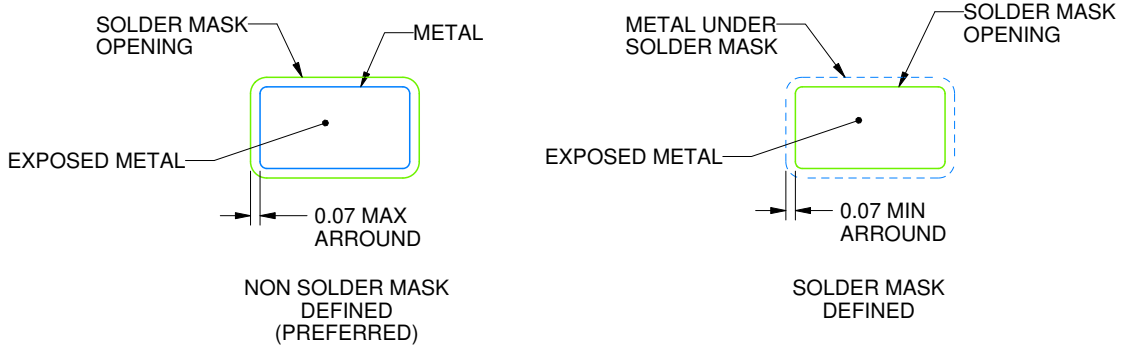
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

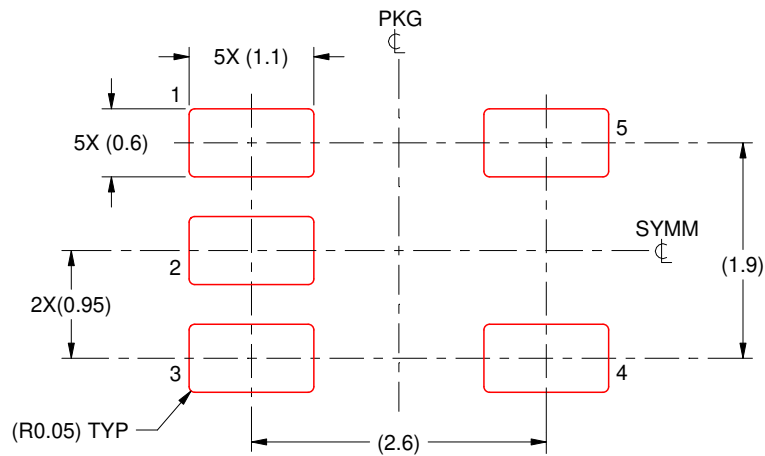


# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

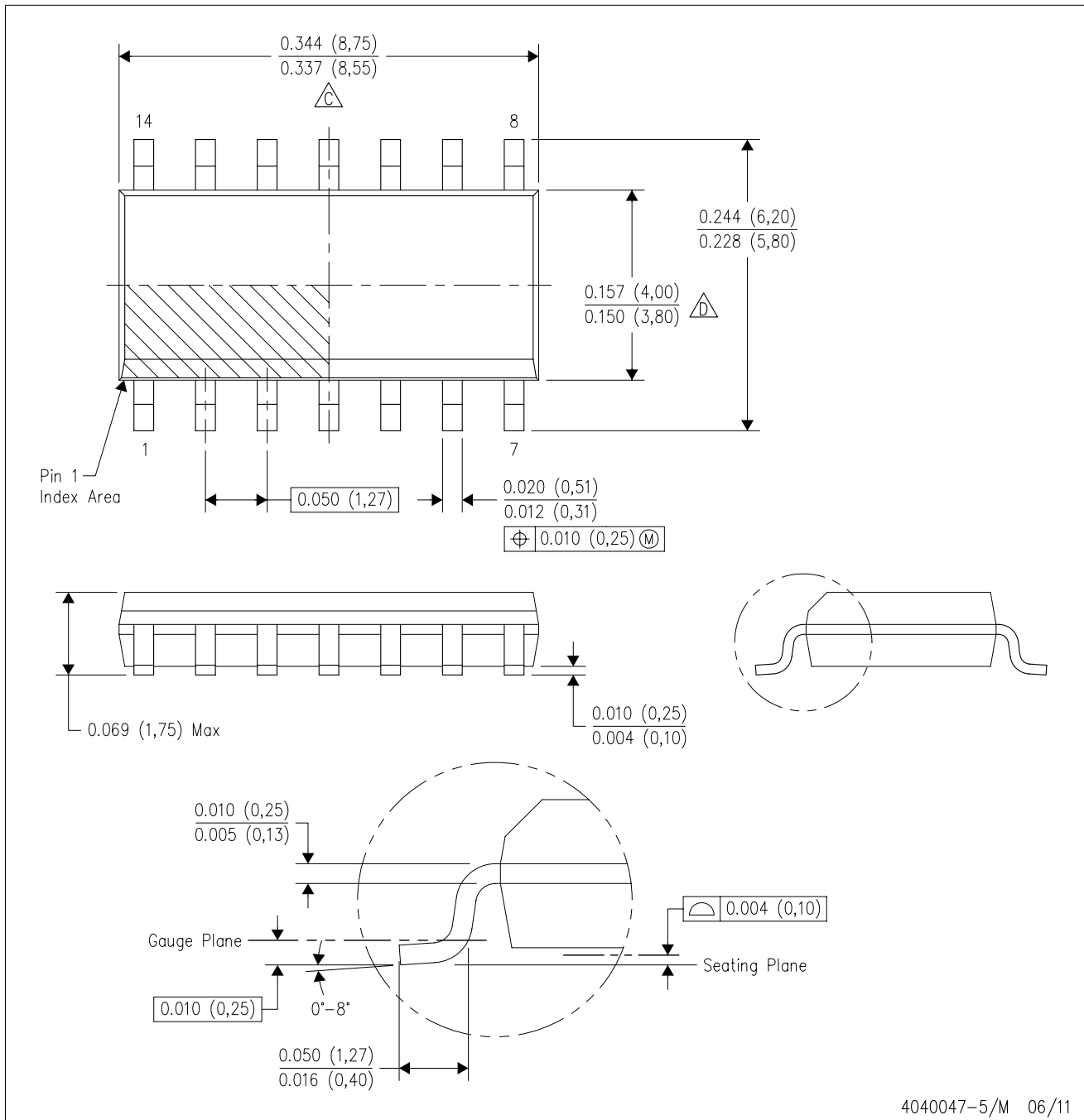
4214839/H 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

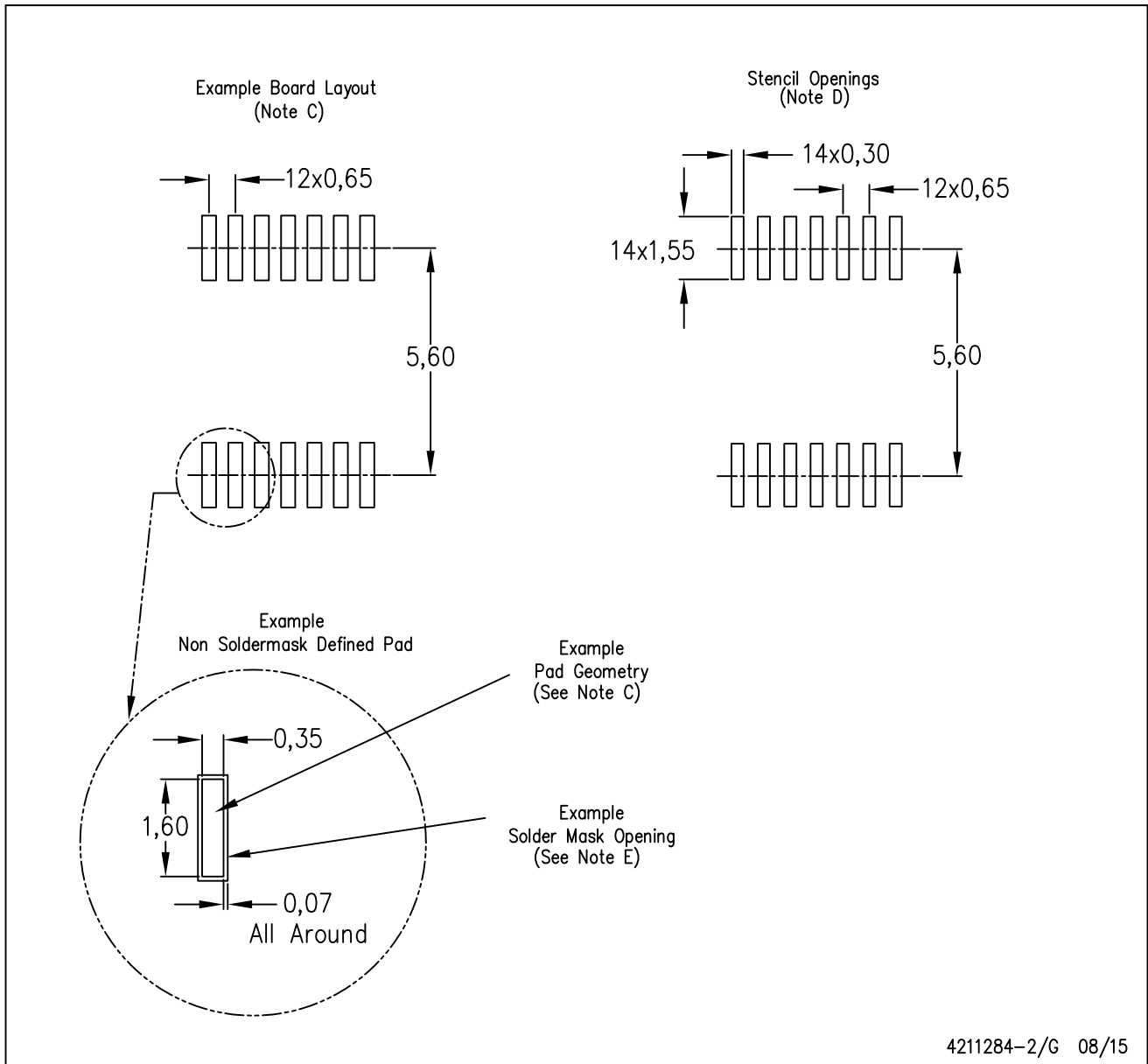


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

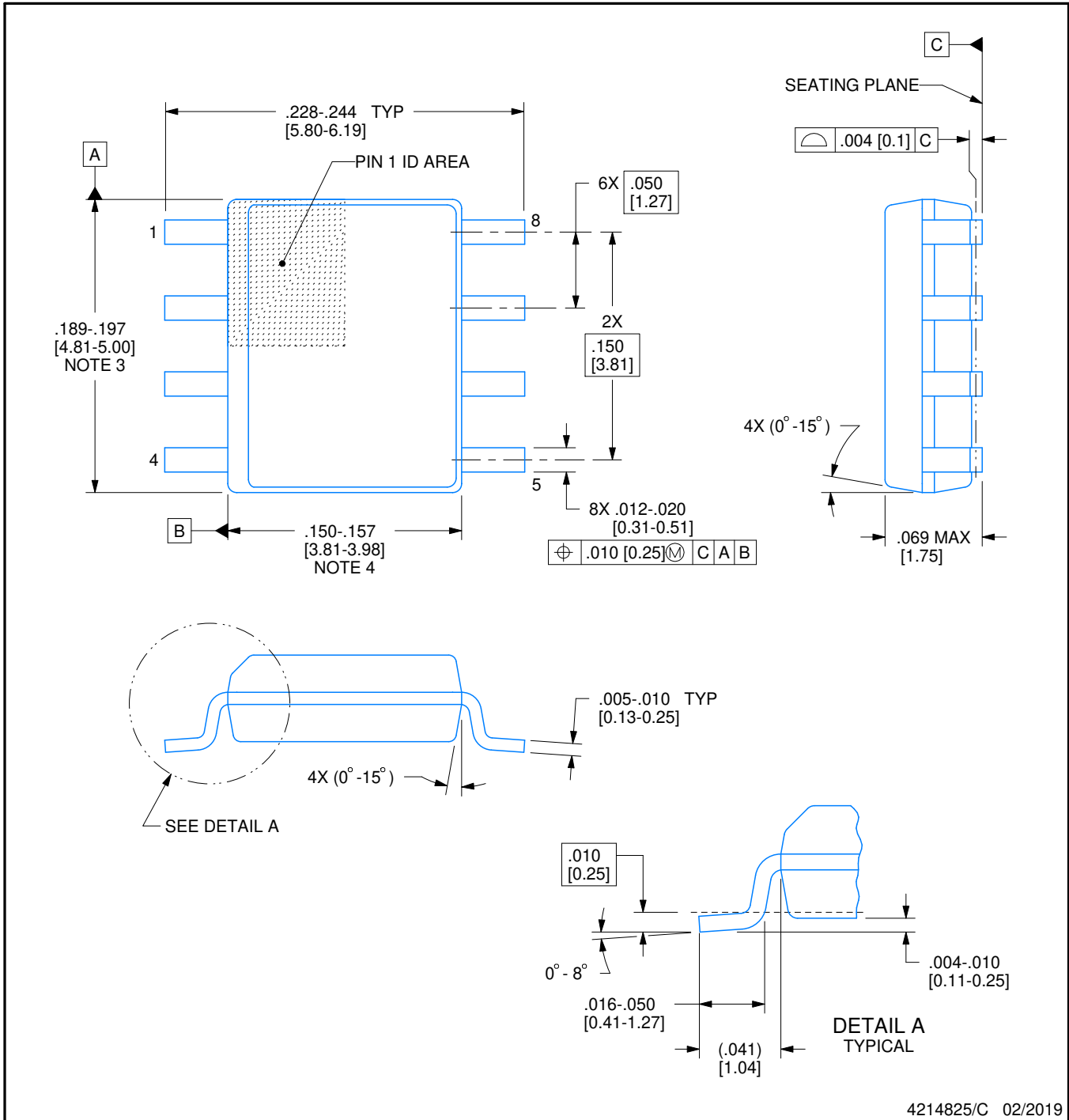


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

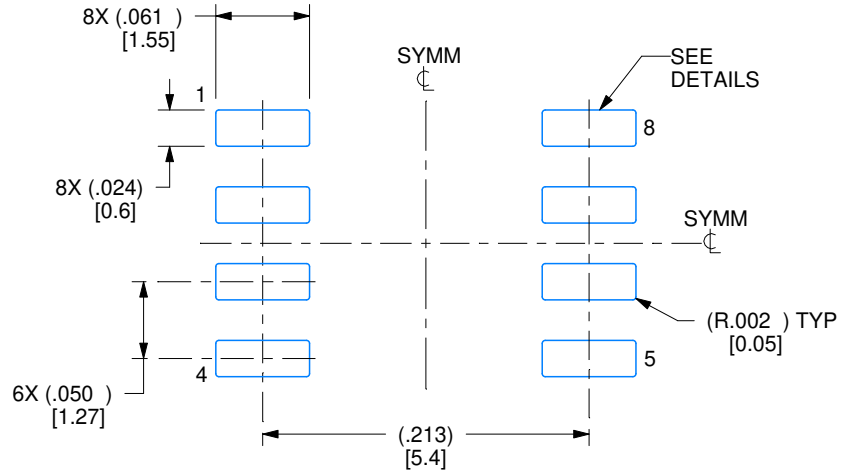
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

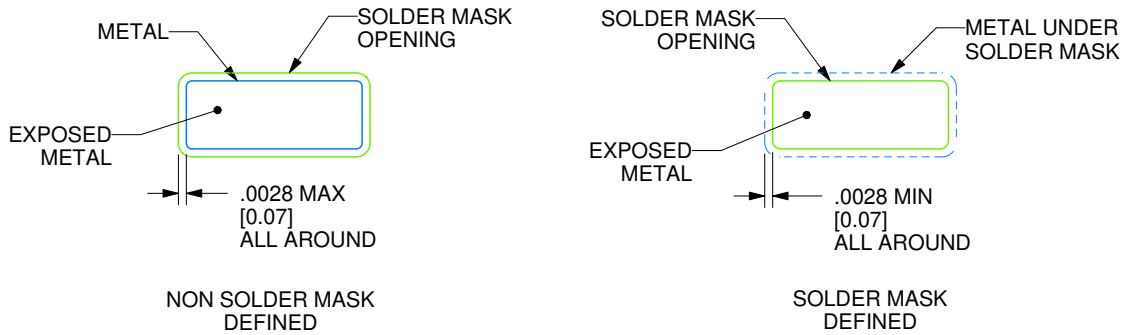
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

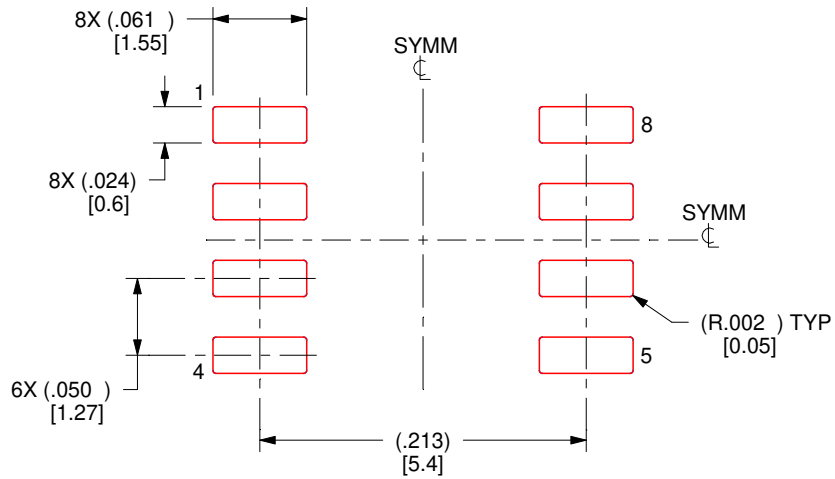
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

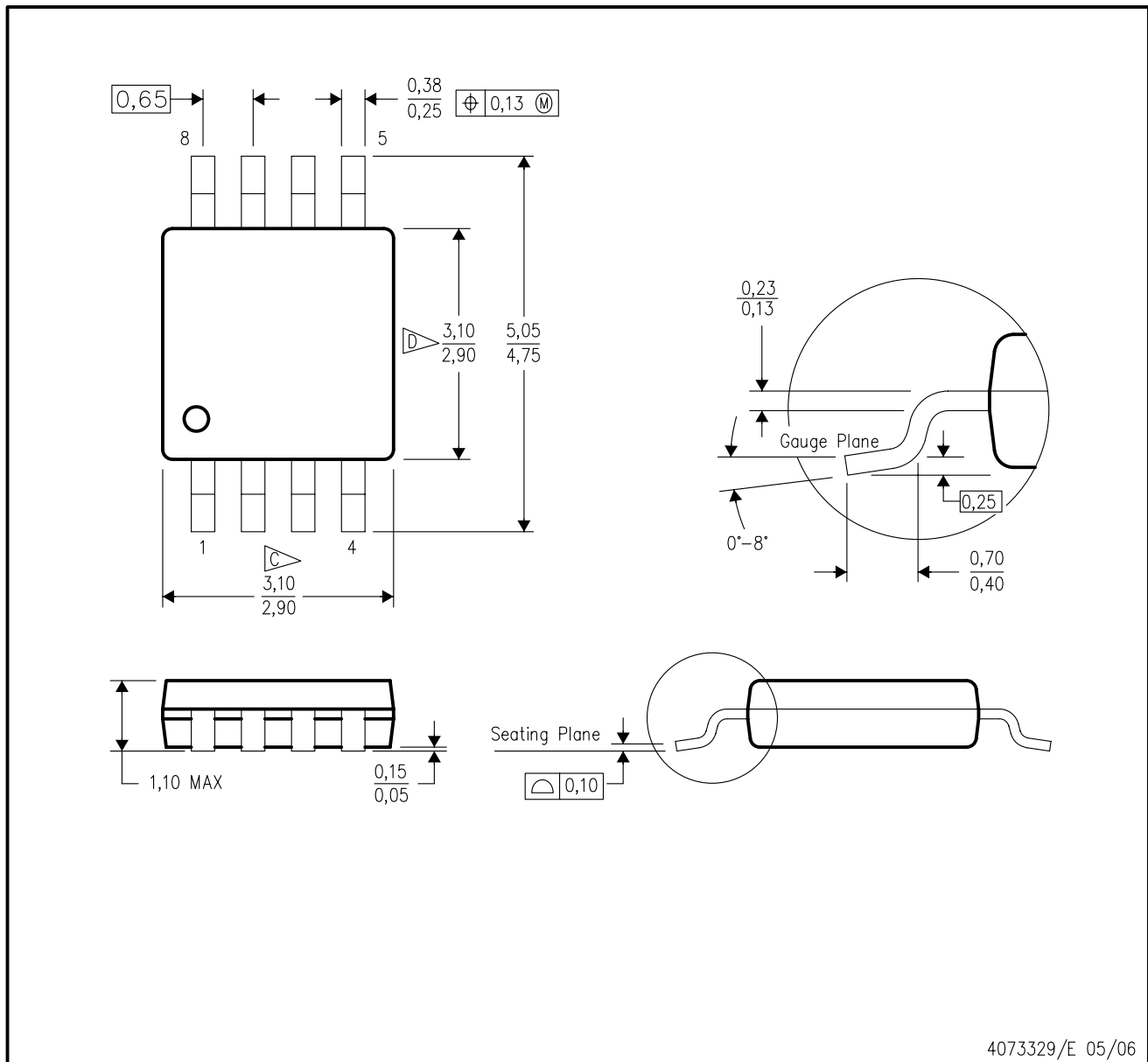
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

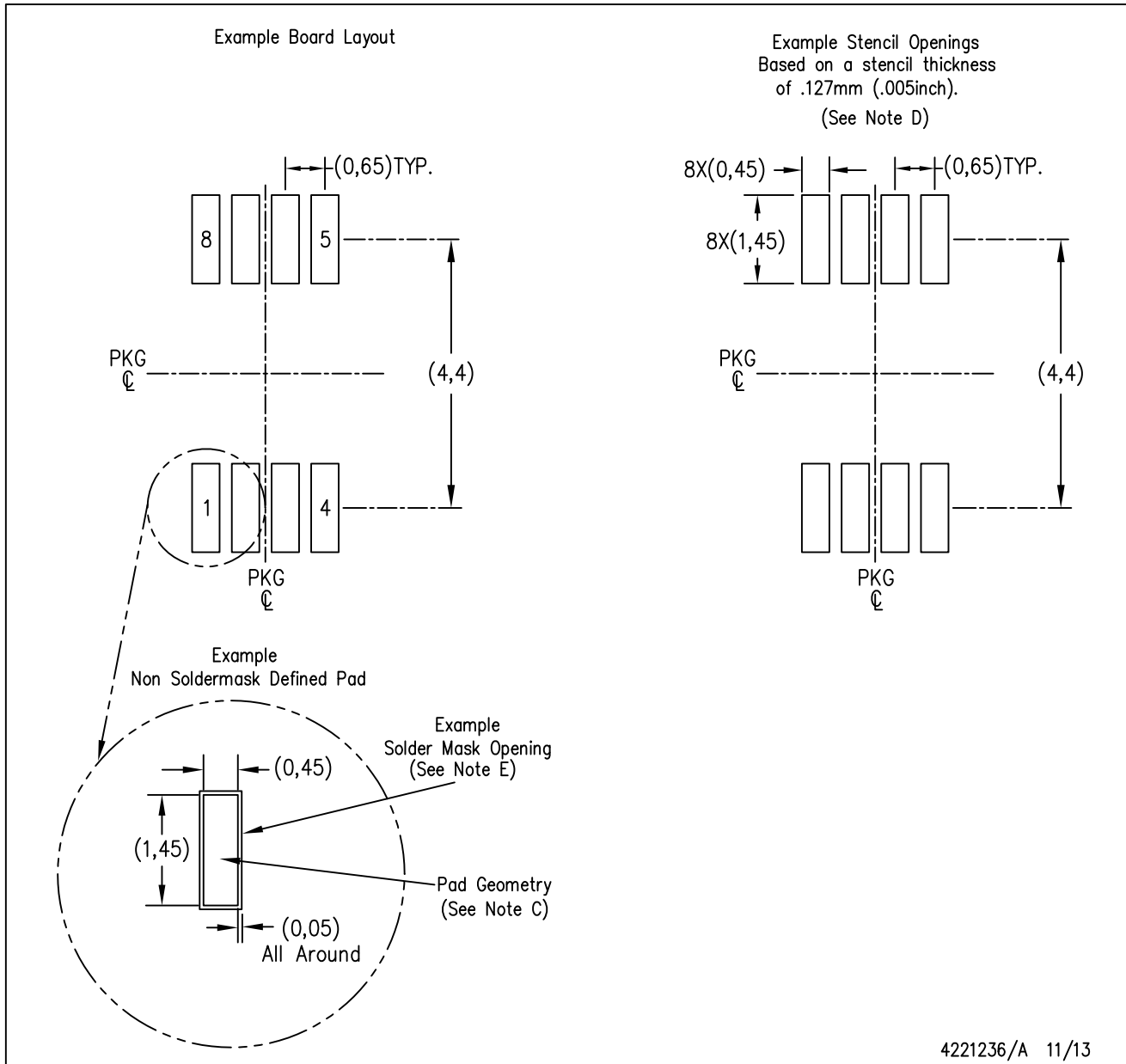


DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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