1A Variable Output

LDO Regulator with Power Good

BD00JC0MNUX-M

General Description

BD00JC0MNUX-M is a low-voltage output 1ch linear regulator IC that operates from a very low input supply and offers an ideal performance in low input voltage to low output voltage applications. It has built-in N-MOSFET power transistor that minimizes the input-to-output voltage differential producing very small ON resistance (RON=200mΩ) level. By lowering the dropout voltage in this way, the IC can operate even at high current (Iomax=1A) with very low power loss. As a result, this eliminates the need for switching regulator and its associated components. BD00JC0MNUX-M is designed for small packages that causes cost reduction. Its output voltage can be varied from 0.65V to 2.7V and it has a soft start (NRCS) function that enables an output voltage ramp-up which can be set to whatever power supply sequence is required.

Features

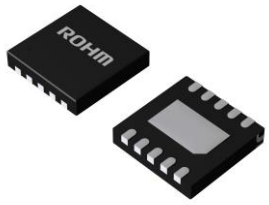
- High Output Voltage Accuracy : ±1%
- Built-in VCC Under Voltage Lock Out circuit
- With Soft Start Function (NRCS)
- Low ON Resistance
- Built-in Over-Current Protection Circuit
- Built-in Thermal Shut Down circuit (TSD)
- Variable Output
- With Tracking Function
- Small package VSON010X3030

Key Specifications

- Input Power Supply Voltage Range
  - Input Voltage 1 (V_{CC}): 3.0V to 5.5V
  - Input Voltage 2 (V_{IN}): 0.95V to 4.5V
- Output Voltage Range: 0.65V to 2.7V
- Output Current: 1.0A
- Operating Temperature Range: -40°C to +105°C

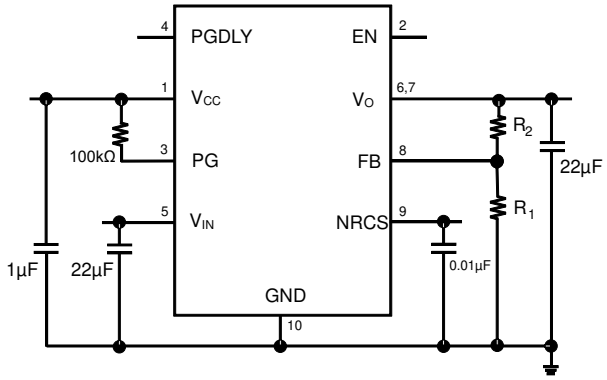
Package

W(Typ) x D(Typ) x H(Max)
3.0mm x 3.0mm x 0.6mm



VSON010X3030

Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

Block Diagram

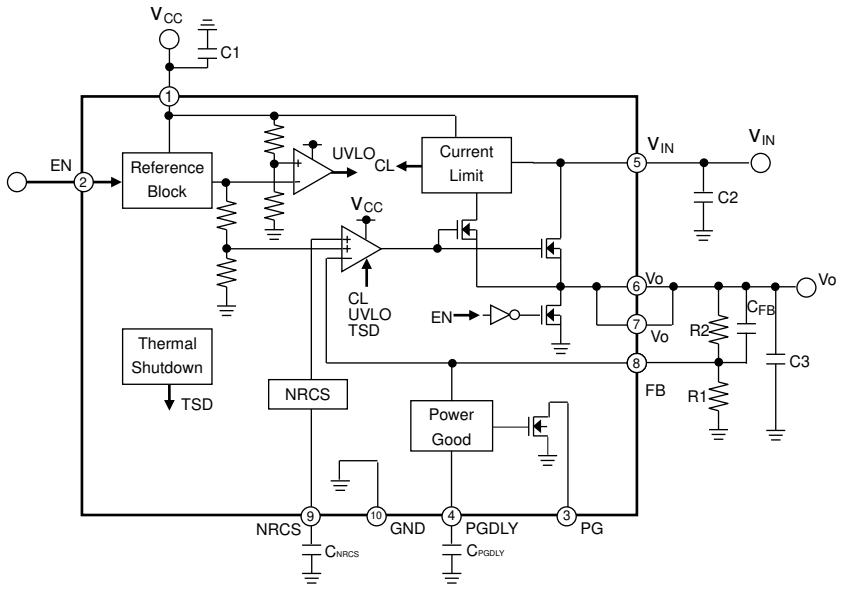


Figure 1. Block Diagram

Pin Description

Pin No.	Pin name	Pin Function
1	V_{CC}	Power supply pin
2	EN	Enable input pin
3	PG	Power Good pin
4	PGDLY	Power Good Delay capacitor connection pin
5	V_{IN}	Input voltage pin
6	V_O	Output voltage pin
7	V_O	Output voltage pin
8	FB	Reference voltage feedback pin
9	NRCS	In-rush current protection (NRCS) capacitor connection pin
10	GND	Ground pin

Description of Blocks

・AMP

This is an error amp that compares the reference voltage (0.65V) with Vo to drive the output Nch FET (Ron=200mΩ). Frequency optimization helps to adjusts on rapid transient response, and to support the use of ceramic capacitors on the output. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to V_{CC}. When EN is OFF, or when UVLO is active, output goes LOW and the output of the NchFET switches OFF.

・EN

The EN block controls the regulators ON/OFF state through the EN logic input pin. When OFF, circuit current is maintained at 0μA, thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin and Vo, thereby draining the excess charge and preventing the IC on the load side from malfunctioning. Since no electrical connection is required (e.g., between the V_{CC} pin and the ESD prevention Diode), operation is independent of the input sequence.

・UVLO

To prevent malfunctions that can occur during a momentary decrease in V_{CC}, the UVLO circuit switches the output to OFF, and (like the EN block) discharges NRCS and Vo. Once the UVLO threshold voltage (TYP2.5V) is reached, the power-on reset is triggered and output continues.

・CURRENT LIMIT

When output is ON, the current limit monitors the internal IC output current against the designed value (2.0A). When current exceeds this level, the current limit circuit lowers the output current to protect the IC. When the overcurrent state is eliminated, output voltage is restored.

・NRCS (Non Rush Current on Start-up)

The soft start function is enabled by connecting an external capacitor between the NRCS pin and GND pin. Output ramp-up can be set for any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a 20μA (TYP) constant current source to charge the external capacitor. Output start time is calculated via formula (1) below.

$$t = C\frac{0.65V}{20\mu A} \quad \cdot\cdot\cdot (1)$$

Tracking sequence is available by connecting the output voltage of external power supply instead of external capacitor. And then, ratio-metric sequence is also available by changing the resistor divider network of external power supply output voltage. (See next page)

・TSD (Thermal Shut Down)

The shutdown (TSD) circuit automatically switches the output OFF when the chip temperature gets too high, thus protecting the IC against “thermal runaway” and heat damage. Because the TSD circuit is provided to shut down the IC in the presence of extreme heat, in order to avoid potential problems with the TSD, it is crucial that the Tj (max) parameter not be exceeded in the thermal design.

・V_{IN}

The V_{IN} line acts as the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the V_{CC} pin and the ESD protection Diode) is necessary, V_{IN} operates independent of the input sequence. However, since an output NchFET body Diode exists between V_{IN} and Vo, a V_{IN}-Vo electric (Diode) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to V_{IN} from Vo.

・PGOOD

It outputs the output voltage (Vo). PGOOD pin (open drain) is used to pull up the 100kΩ resistor. PGOOD is HIGH when FB voltage is between 0.585V(TYP) to 0.715V(TYP), and LOW if the voltage is out of range.

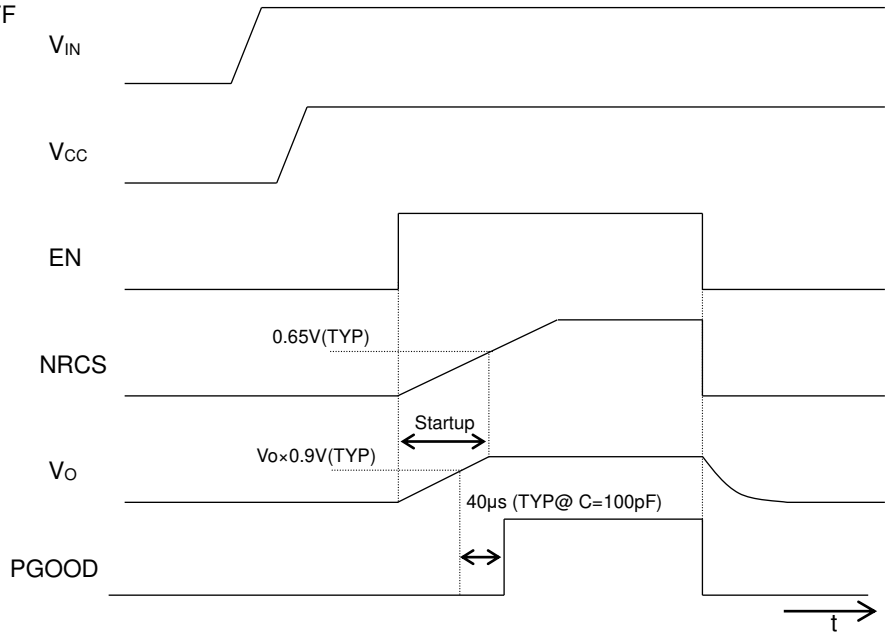
・PGDLY

It is available to set PGOOD output delay. PGDLY pin should be connected to 100pF capacitor.
PGOOD delay time is determined by the following formula.

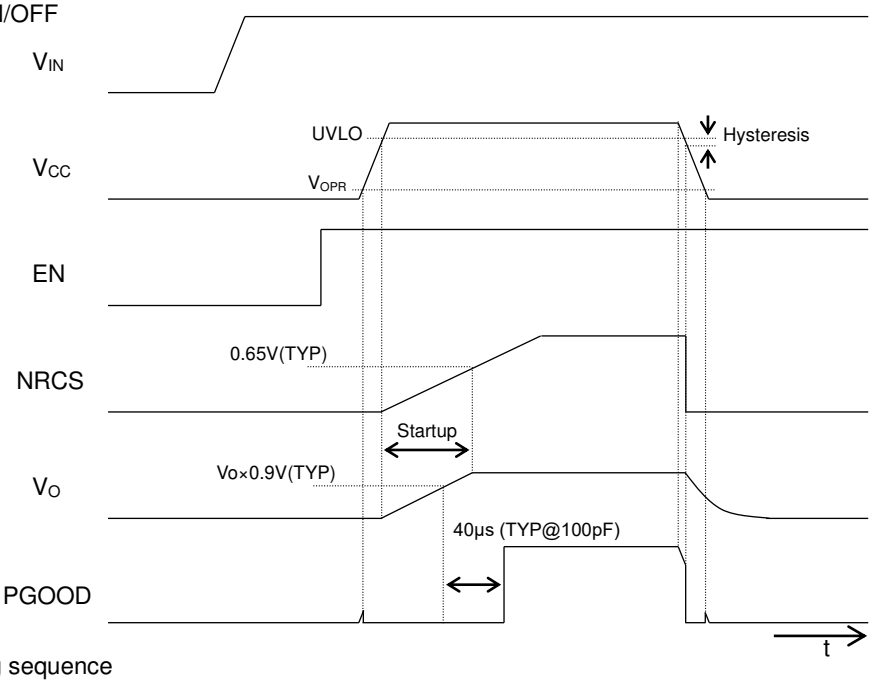
$$t_{PGDLY} = \frac{C(pF)\times 0.75}{I_{PGDLY}\ (\mu A)}\ (\mu sec)$$

Timing Chart

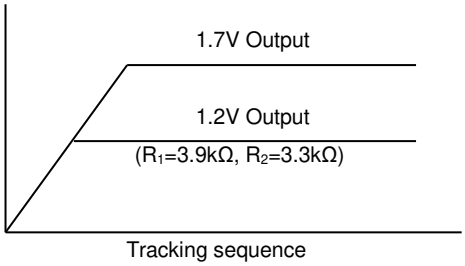
EN ON/OFF

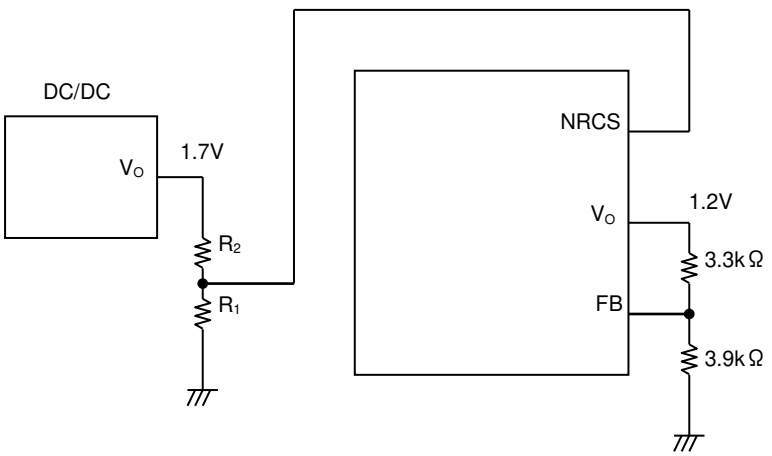


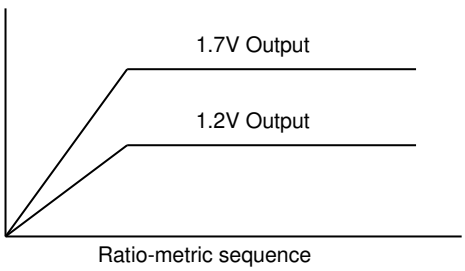
VCC ON/OFF



Tracking sequence







Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Input Voltage 1	V_{CC}	+6.0 (Note 1)	V
Input Voltage 2	V_{IN}	+6.0 (Note 1)	V
Enable Input Voltage	V_{EN}	-0.3 to +6.0	V
PGOOD Input Voltage	V_{PGOOD}	+6.0 (Note 1)	V
Power Dissipation 1	Pd1	0.575 (Note 2)	W
Power Dissipation 2	Pd2	1.8 (Note 3)	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) Not to exceed Power dissipation (Pd)
(Note 2) Reduced by 4.6mW/℃ for temperature above 25℃ (when mounted on a 1-layer glass epoxy board with 74.2mm×74.2mm×1.6mm dimension, and copper foil dimension = 6.28mm^2).
(Note 3) Reduced by 14.4mW/℃ for temperature above 25℃ (when mounted on a 4-layer glass epoxy board with 74.2mm×74.2mm×1.6mm dimension, and copper foil dimension = 6.28mm^2).

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Voltage 1	V_{CC}	3.0	5.5	V
Input Voltage 2	V_{IN}	0.95	VCC-1 (Note 4)	V
Output Current	I_O	-	1.0	A
PGOOD Input Voltage	V_{PGOOD}	-0.3	5.5	V
Output Voltage Setting Range	V_O	V_{FB}	V_{IN}-dVo (Note 5)	V
Enable Input Voltage	V_{EN}	-0.3	5.5	V

(Note 4) No power-ON sequence for VCC and VIN.
(Note 5) Minimum dropout voltage (Electrical Characteristics).

Electrical Characteristics

(Unless otherwise specified Ta=-40 to 105°C, V_{CC}=5V, V_{EN}=3V, V_{IN}=1.7V, R_1=3.9kΩ, R_2=3.3kΩ)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current	I_{CC}	-	0.7	1.0	mA	
VCC Shutdown Mode Current	I_{STB}	-	0	10	μA	V_{EN}=0V
Output Voltage	VOUT	-	1.200	-	V	
Output Voltage Temperature Coefficient	T_{CVO}	-	0.01	-	%/°C	
Feedback Voltage 1	V_{FB1}	0.643	0.650	0.657	V	Tj=25°C
Feedback Voltage 2	V_{FB2}	0.637	0.650	0.663	V	Tj=-40 to 105°C
Load Regulation	Reg.L	-	0.5	10	mV	I_O=0A to 1.0A
Line Regulation 1	Reg.l1	-	0.1	0.5	%/V	V_{CC}=3.0V to 5.5V
Line Regulation 2	Reg.l2	-	0.1	0.5	%/V	V_{IN}=1.5V to 3.3V
Standby Discharge Current	Id_{EN}	1	-	-	mA	V_{EN}=0V, V_O=1V
[ENABLE]						
Enable Pin Input Voltage High	EN_{HI}	2	-	-	V	
Enable Pin Input Voltage Low	EN_{LOW}	0	-	VCC×0.15	V	
Enable Input Bias Current	I_{EN}	-	7	10	μA	V_{EN}=3V
[NRCS]						
NRCS Charge Current	I_{NRCS}	14	20	26	μA	V_{NRCS}=0.5V
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	VCC_{UVLO}	2.3	2.5	2.7	V	V_{CC}:Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	VCC_{HYS}	50	100	150	mV	V_{CC}:Sweep-down
[PGOOD]						
Low-side Threshold Voltage	V_{THPGL}	V_O×0.87	V_O×0.9	V_O×0.93	V	
High-side Threshold Voltage	V_{THPGH}	V_O×1.07	V_O×1.1	V_O×1.13	V	
PGDLY charge current	I_{PGDLY}	1.4	2.0	2.6	μA	
Ron	R_{PG}	30	75	150	Ω	
[AMP]						
Minimum dropout voltage	dV_O	-	200	300	mV	I_O=1.0A, V_{IN}=1.2V

Typical Performance Curves

(Unless otherwise specified V_{CC}=5V, V_{EN}=3V, V_{IN}=1.7V, R_1=3.9kΩ, R_2=3.3kΩ)

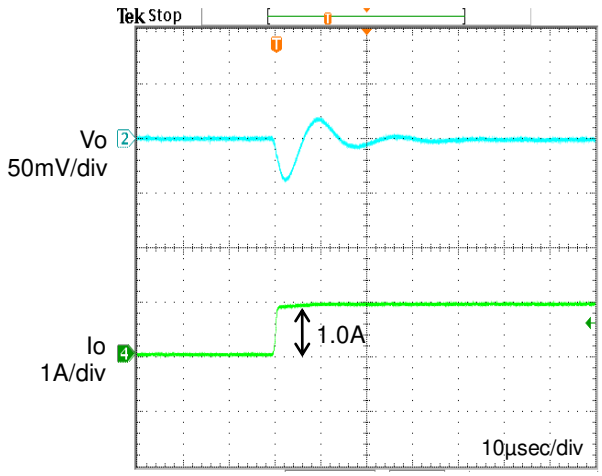


Figure.2 Transient Response
(Io=0 → 1.0A, Ta=-40°C)
C_O=100uF, C_{FB}=1000pF

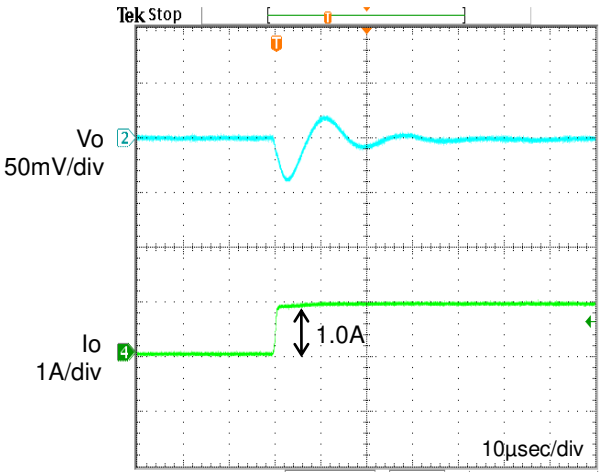


Figure.3 Transient Response
(Io=0 → 1.0A, Ta=25°C)
C_O=100uF, C_{FB}=1000pF

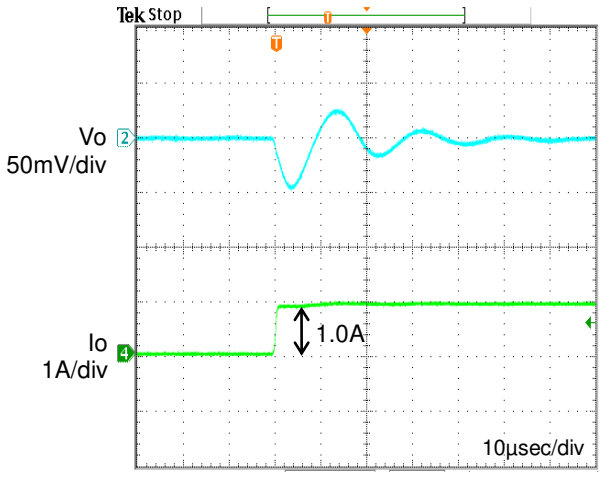


Figure.4 Transient Response
(Io=0 → 1.0A, Ta=105°C)
C_O=100uF, C_{FB}=1000pF

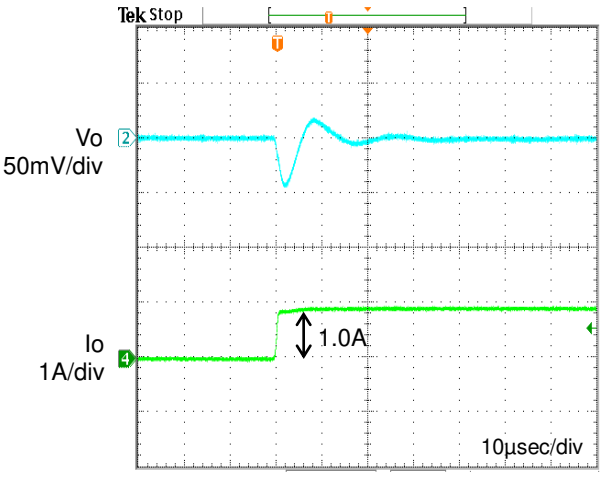


Figure.5 Transient Response
(Io=0 → 1.0A, Ta=-40°C)
C_O=47uF, C_{FB}=1000pF

Typical Performance Curves - continued

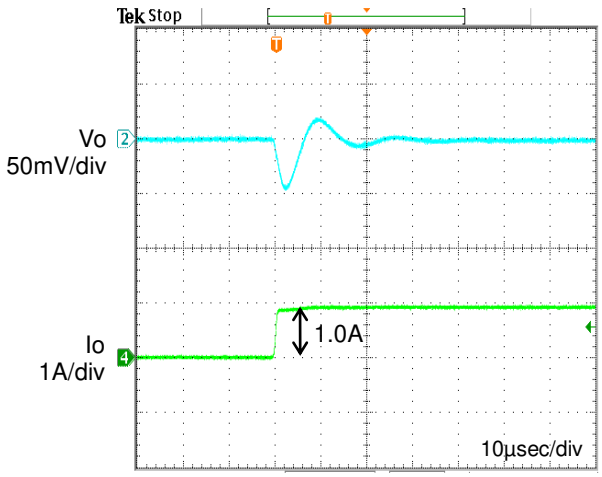


Figure.6 Transient Response
(Io=0 → 1.0A, Ta=25°C)
C_O=47uF, C_{FB}=1000pF

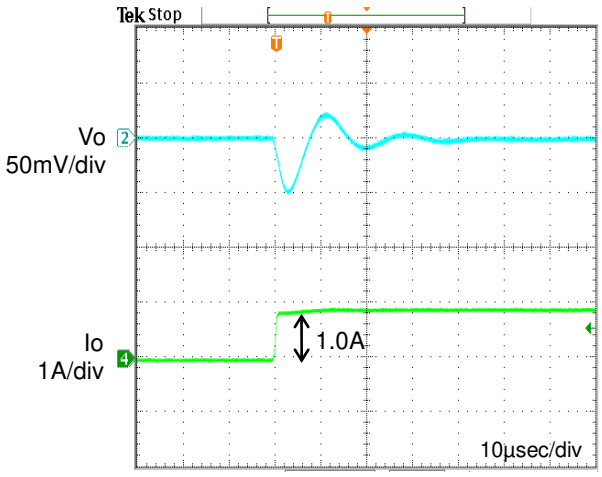


Figure.7 Transient Response
(Io=0 → 1.0A, Ta=105°C)
C_O=47uF, C_{FB}=1000pF

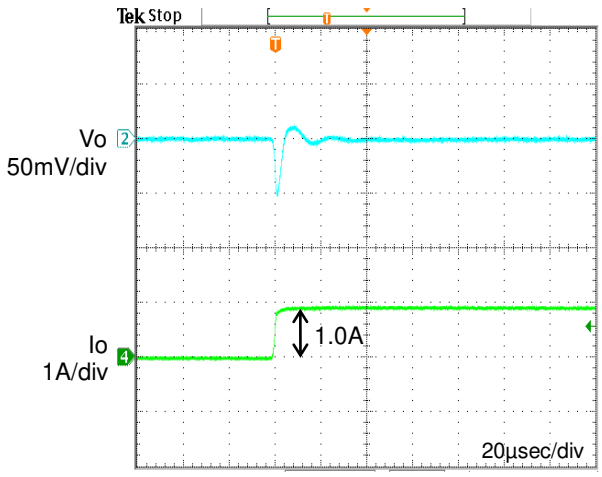


Figure.8 Transient Response
(Io=0 → 1.0A, Ta=-40°C)
C_O=22uF, C_{FB}=1000pF

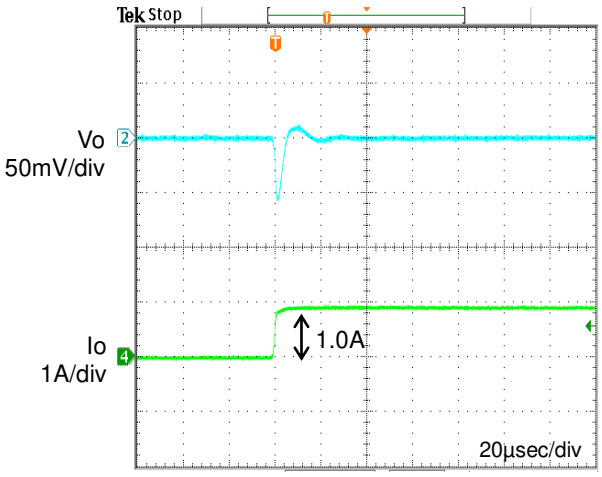


Figure.9 Transient Response
(Io=0 → 1.0A, Ta=25°C)
C_O=22uF, C_{FB}=1000pF

Typical Performance Curves - continued

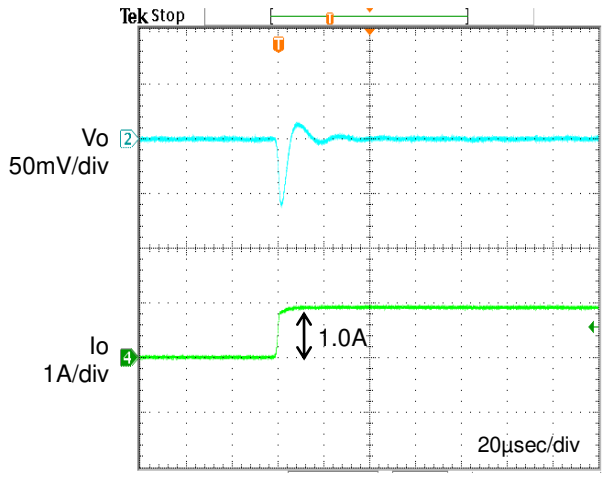


Figure.10 Transient Response
(Io=0 → 1.0A, Ta=105°C)
C_O=22uF, C_{FB}=1000pF

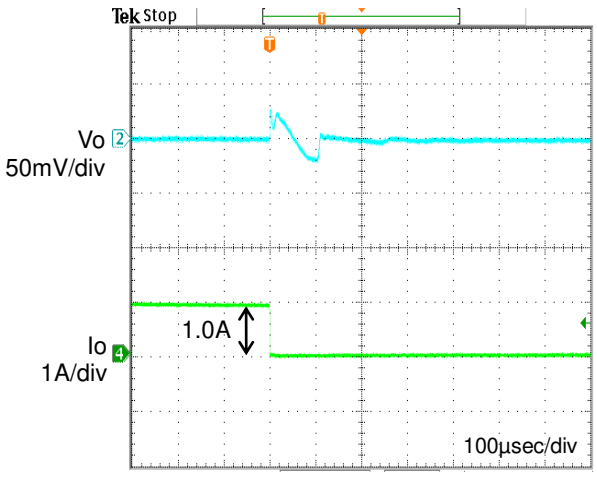


Figure.11 Transient Response
(Io=1.0A → 0, Ta=-40°C)
C_O=100uF, C_{FB}=1000pF

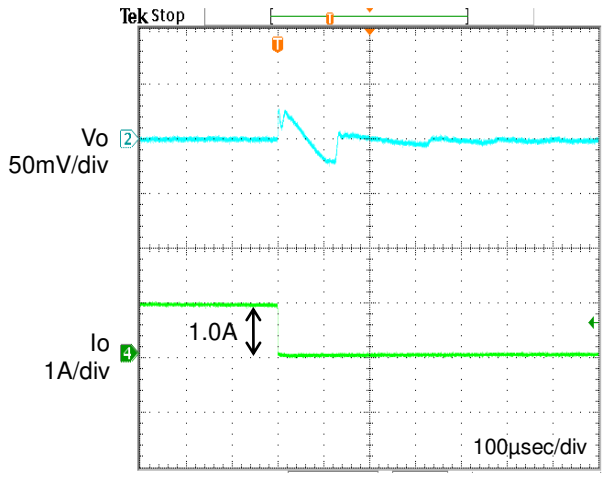


Figure.12 Transient Response
(Io=1.0A → 0, Ta=25°C)
C_O=100uF, C_{FB}=1000pF

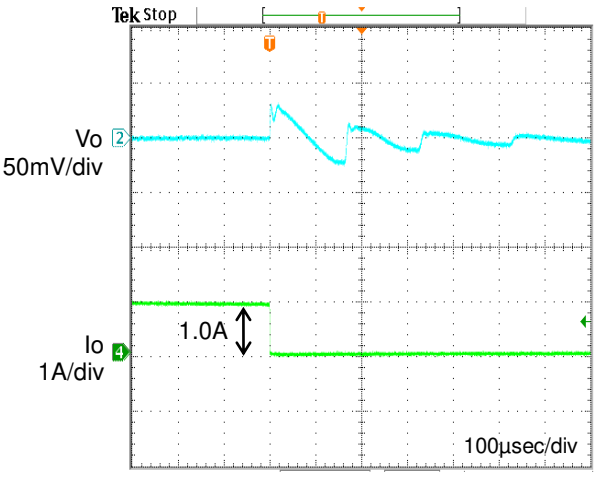


Figure.13 Transient Response
(Io=1.0A → 0, Ta=105°C)
C_O=100uF, C_{FB}=1000pF

Typical Performance Curves - continued

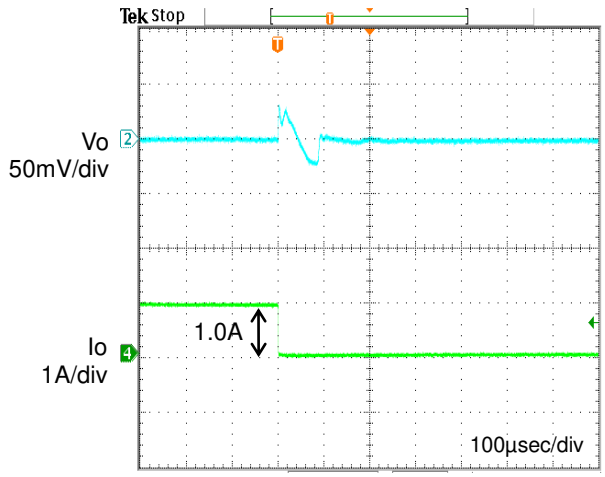


Figure.14 Transient Response
(Io=1.0A → 0, Ta=-40°C)
C_O=47uF, C_{FB}=1000pF

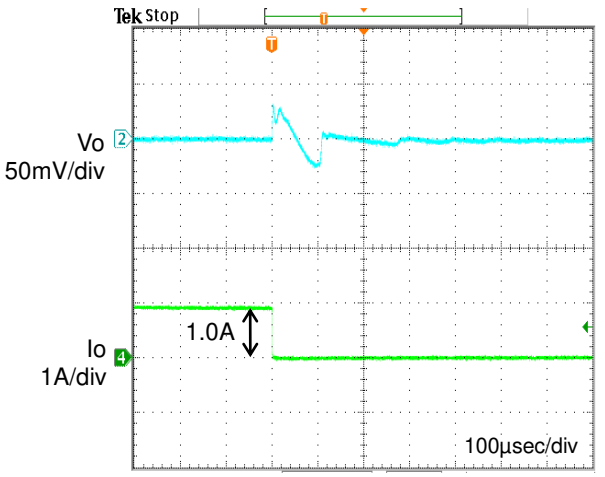


Figure.15 Transient Response
(Io=1.0A → 0, Ta=25°C)
C_O=47uF, C_{FB}=1000pF

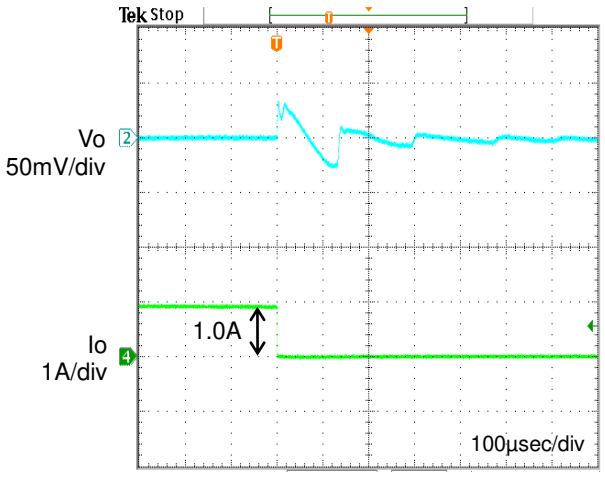


Figure.16 Transient Response
(Io=1.0A → 0, Ta=105°C)
C_O=47uF, C_{FB}=1000pF

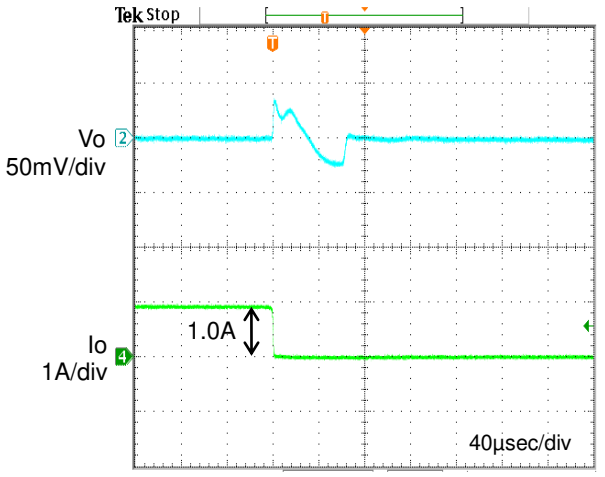


Figure.17 Transient Response
(Io=1.0A → 0, Ta=-40°C)
C_O=22uF, C_{FB}=1000pF

Typical Performance Curves - continued

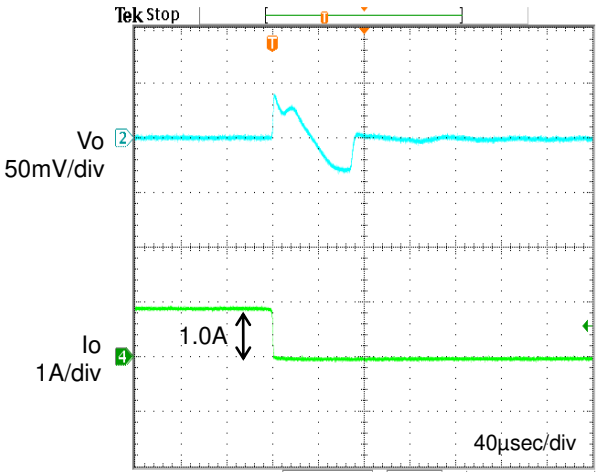


Figure.18 Transient Response
(Io=1.0A → 0, Ta=25°C)
C_O=22uF, C_{FB}=1000pF

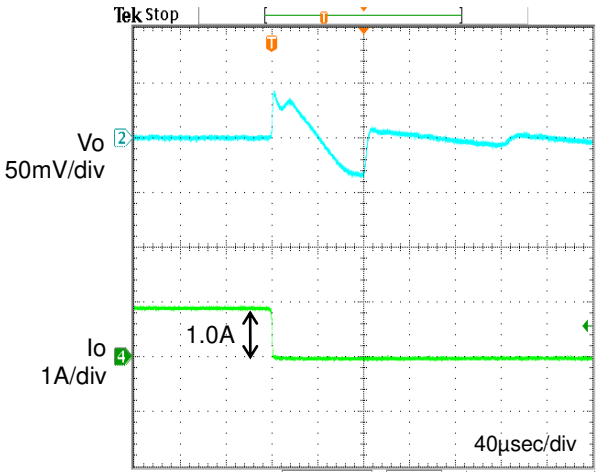


Figure.19 Transient Response
(Io=1.0A → 0, Ta=105°C)
C_O=22uF, C_{FB}=1000pF

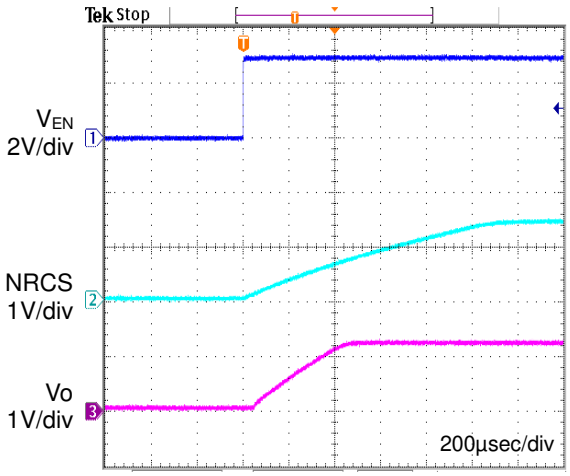


Figure.20 Start-up Sequence 1
(Ta=-40°C)

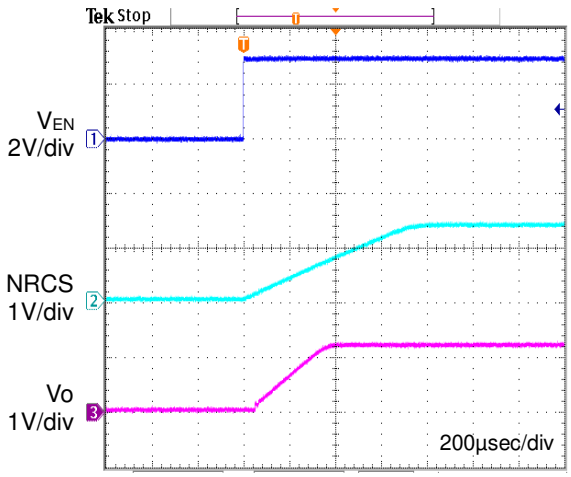


Figure.21 Start-up Sequence 1
(Ta=25°C)

Typical Performance Curves - continued

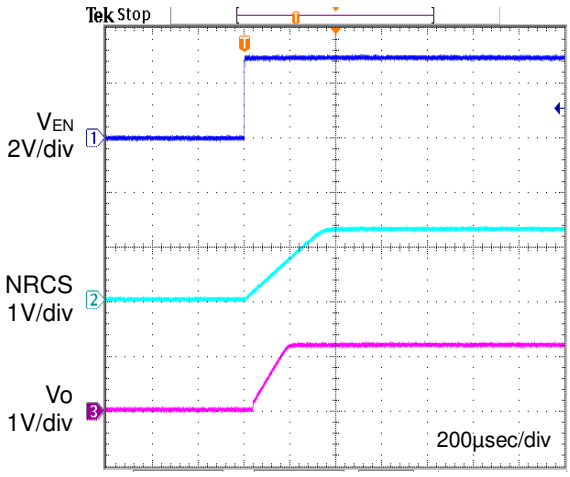


Figure.22 Start-up Sequence 1
(Ta=105°C)

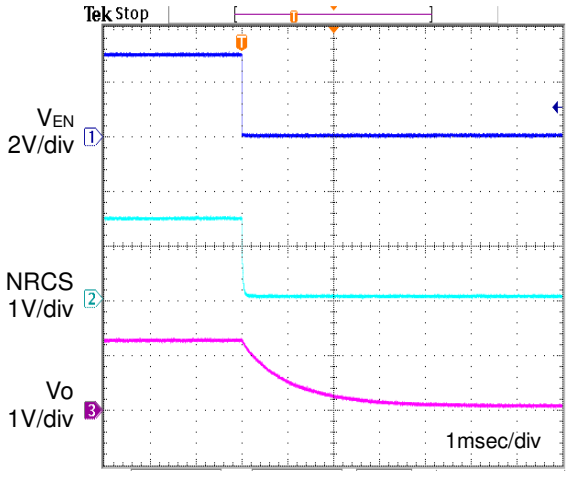


Figure.23 OFF Sequence
(Ta=-40°C)

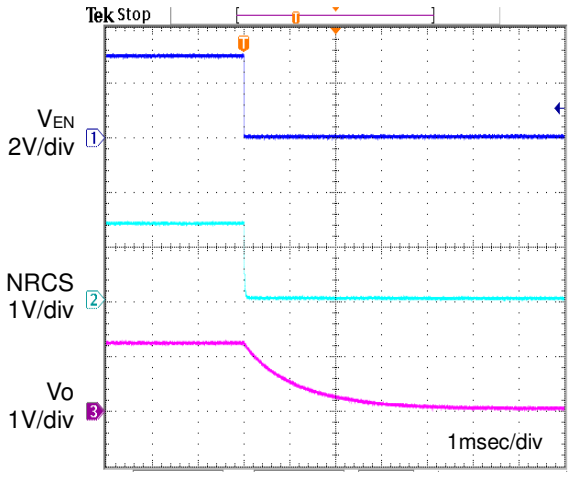


Figure.24 OFF Sequence
(Ta=25°C)

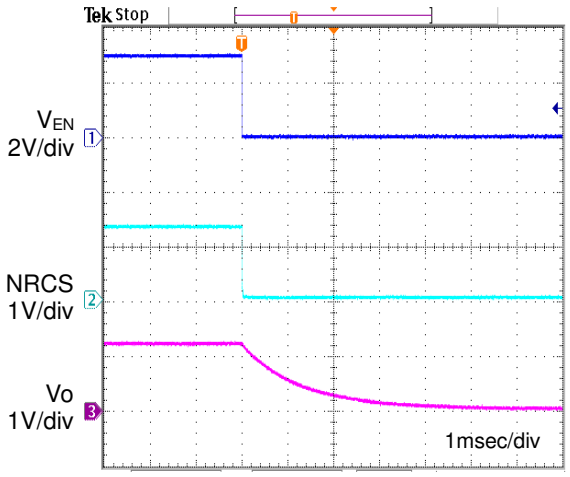


Figure.25 OFF Sequence
(Ta=105°C)

Typical Performance Curves - continued

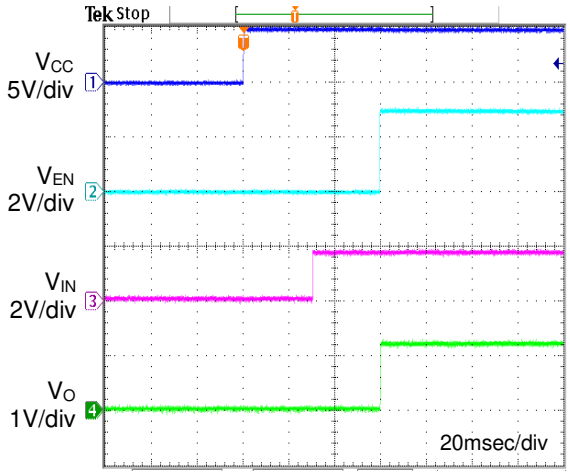


Figure.26 Start-up Sequence 2
(V_{CC} → V_{IN} → V_{EN})
Ta=-40°C

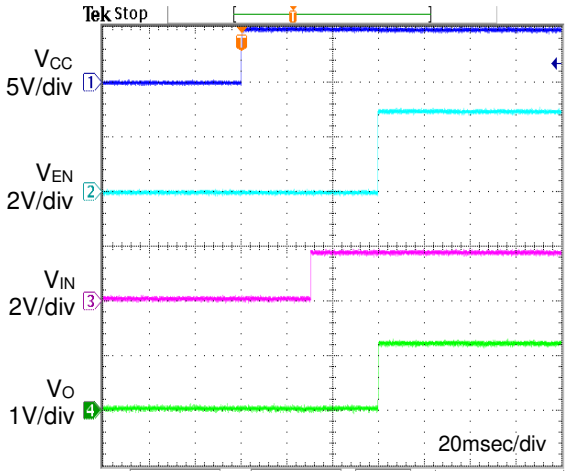


Figure.27 Start-up Sequence 2
(V_{CC} → V_{IN} → V_{EN})
Ta=25°C

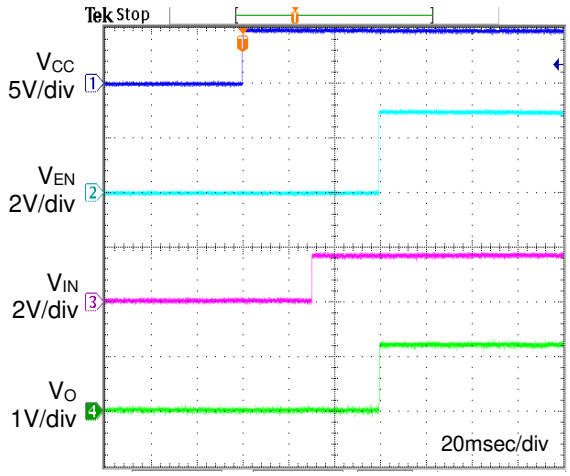


Figure.28 Start-up Sequence 2
(V_{CC} → V_{IN} → V_{EN})
Ta=105°C

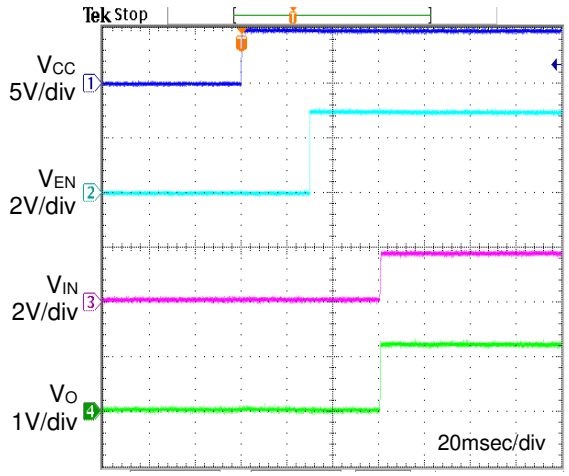


Figure.29 Start-up Sequence 3
(V_{CC} → V_{EN} → V_{IN})
Ta=-40°C

Typical Performance Curves - continued

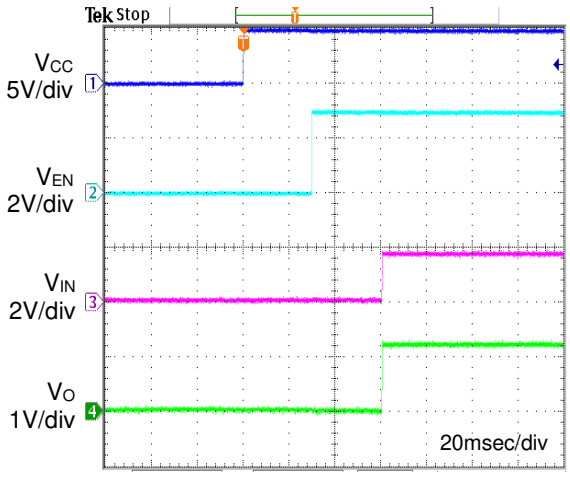


Figure.30 Start-up Sequence 3
(V_{CC} → V_{EN} → V_{IN})
Ta=25°C

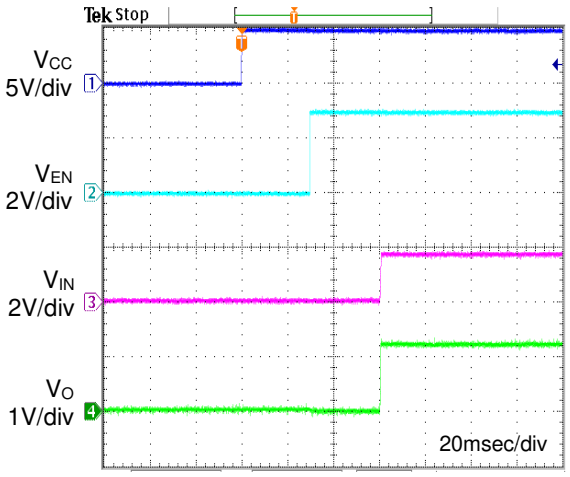


Figure.31 Start-up Sequence 3
(V_{CC} → V_{EN} → V_{IN})
Ta=105°C

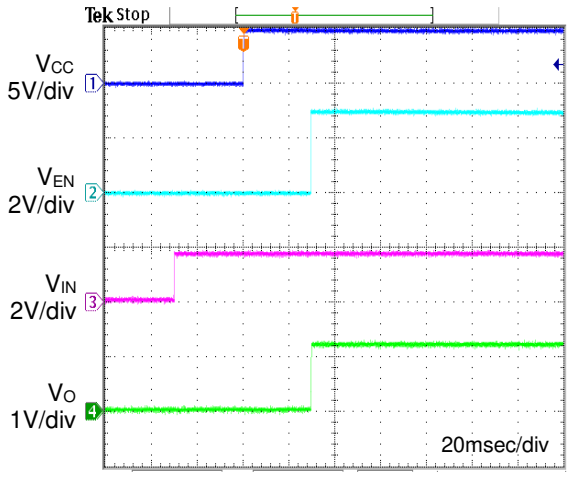


Figure.32 Start-up Sequence 4
(V_{IN} → V_{CC} → V_{EN})
Ta=-40°C

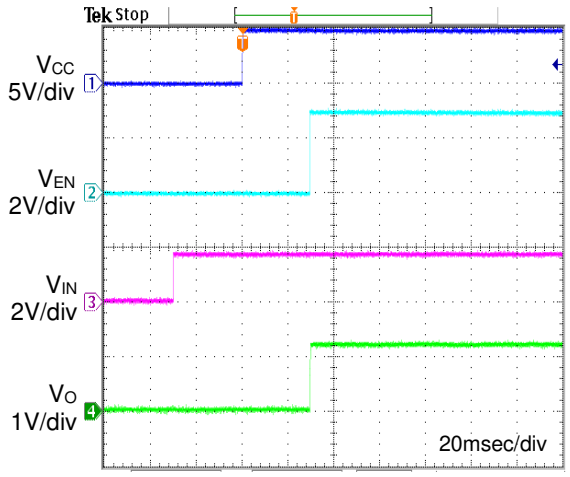


Figure.33 Start-up Sequence 4
(V_{IN} → V_{CC} → V_{EN})
Ta=25°C

Typical Performance Curves - continued

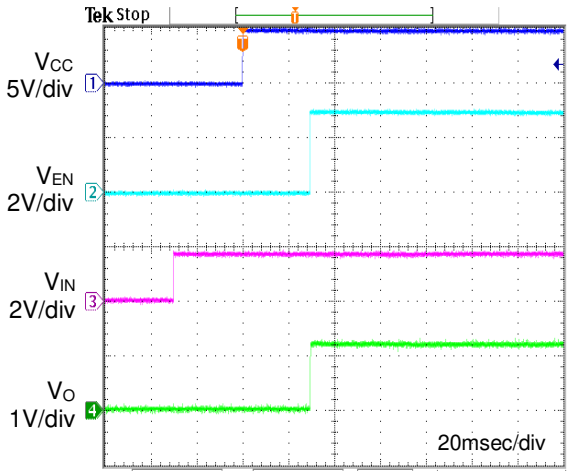


Figure.34 Start-up Sequence 4
(V_{IN} → V_{CC} → V_{EN})
Ta=105°C

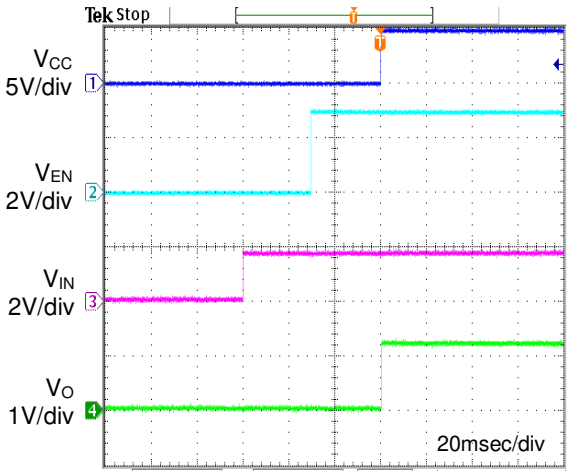


Figure.35 Start-up Sequence 5
(V_{IN} → V_{EN} → V_{CC})
Ta=-40°C

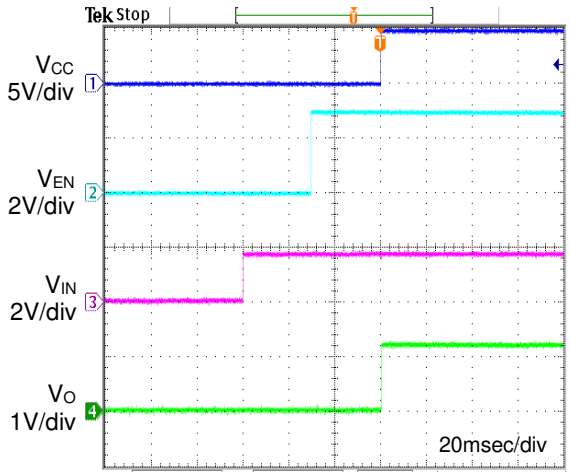


Figure.36 Start-up Sequence 5
(V_{IN} → V_{EN} → V_{CC})
Ta=25°C

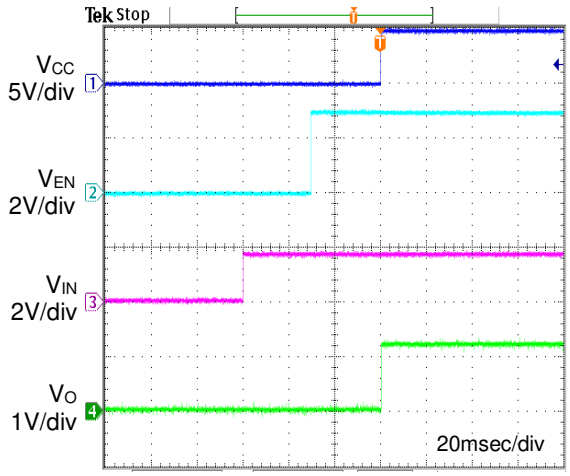


Figure.37 Start-up Sequence 5
(V_{IN} → V_{EN} → V_{CC})
Ta=105°C

Typical Performance Curves - continued

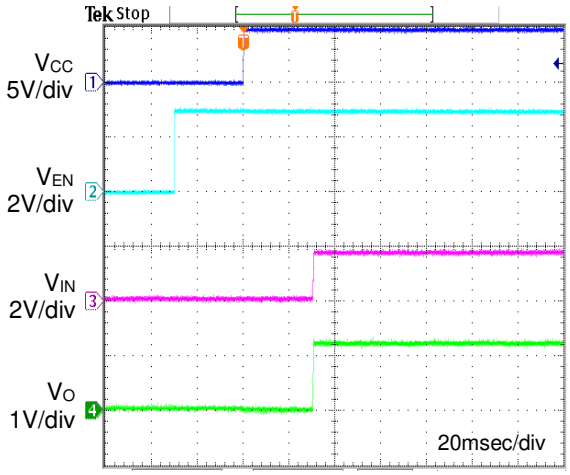


Figure.38 Start-up Sequence 6
(V_{EN} → V_{CC} → V_{IN})
Ta=-40°C

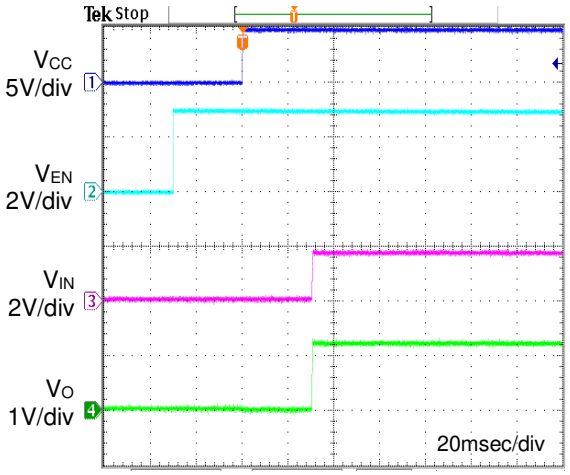


Figure.39 Start-up Sequence 6
(V_{EN}→ V_{CC} → V_{IN})
Ta=25°C

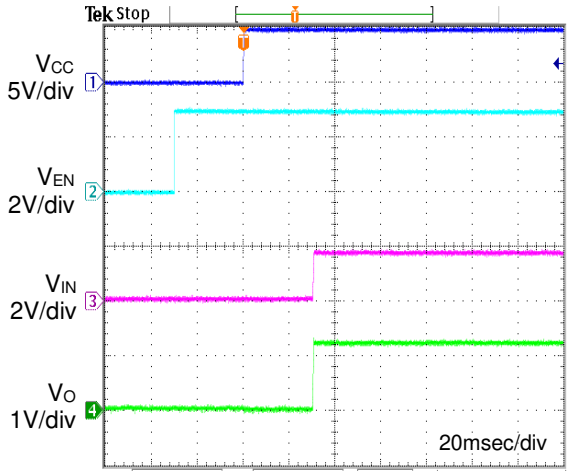


Figure.40 Start-up Sequence 6
(V_{EN} → V_{CC} → V_{IN})
Ta=105°C

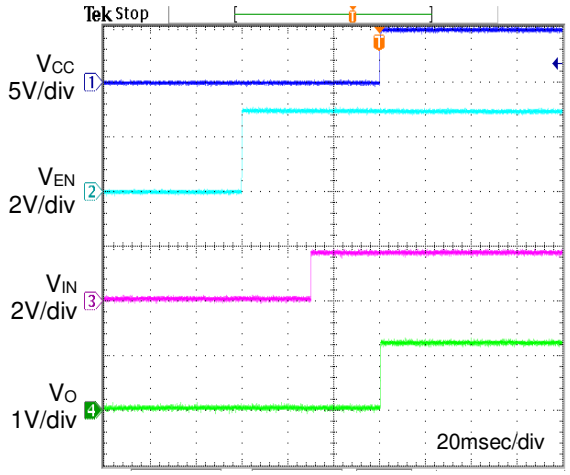


Figure.41 Start-up Sequence 7
(V_{EN} → V_{IN} → V_{CC})
Ta=-40°C

Typical Performance Curves - continued

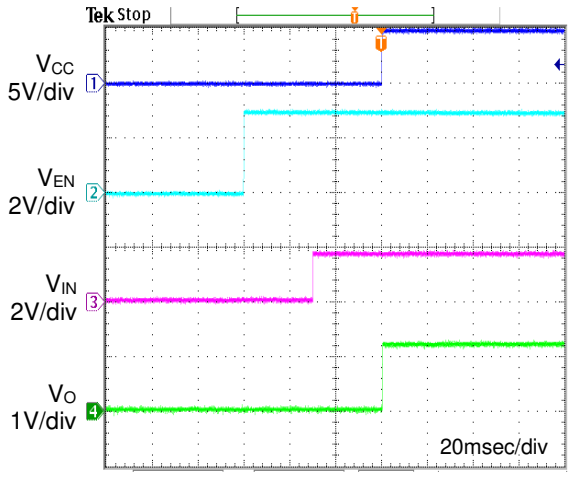


Figure.42 Start-up Sequence 7
(V_{EN} → V_{IN} → V_{CC})
Ta=25°C

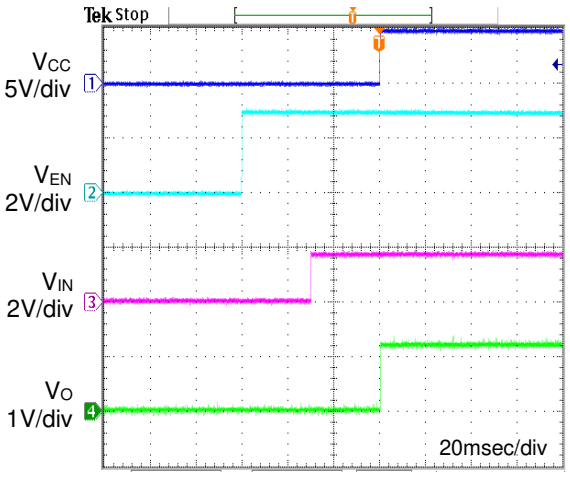


Figure.43 Start-up Sequence 7
(V_{EN} → V_{IN} → V_{CC})
Ta=105°C

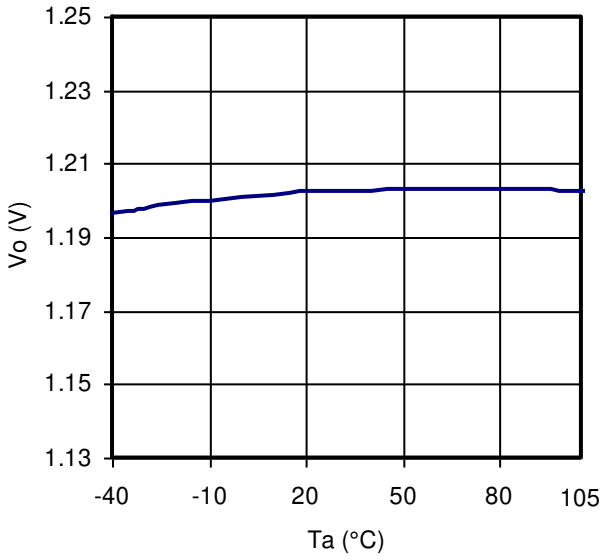


Figure.44 Ta-Vo
(I_O=0mA)

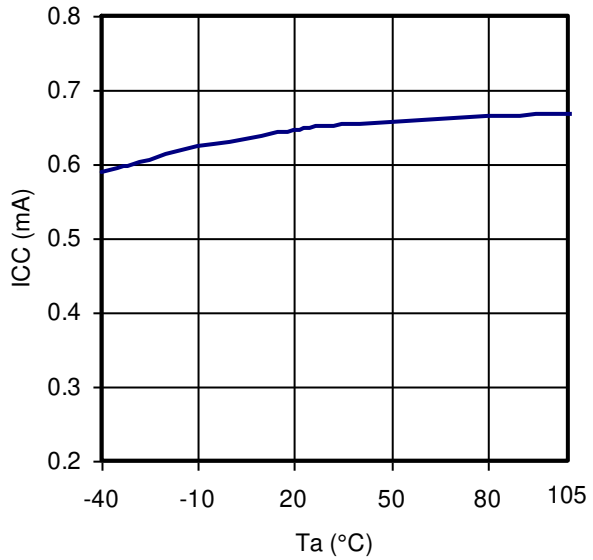


Figure.45 Ta-I_{CC}

Typical Performance Curves - continued

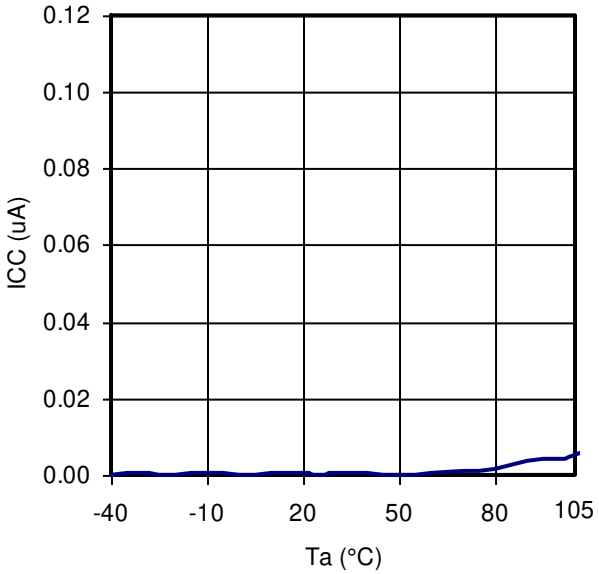


Figure.46 Ta-I_{STB}

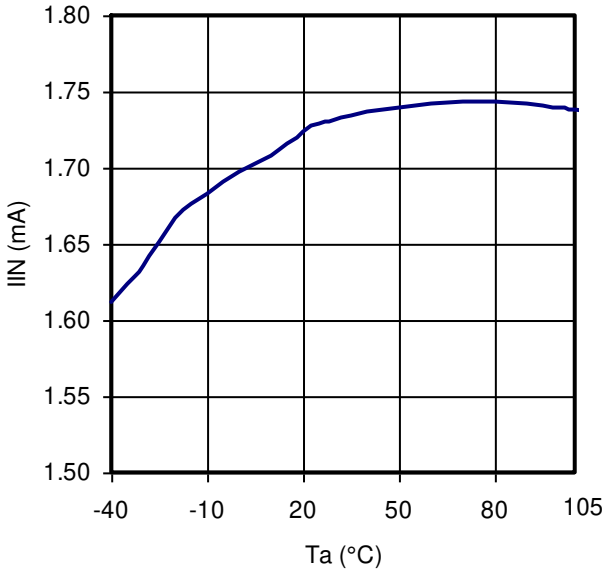


Figure.47 Ta-I_{IN}

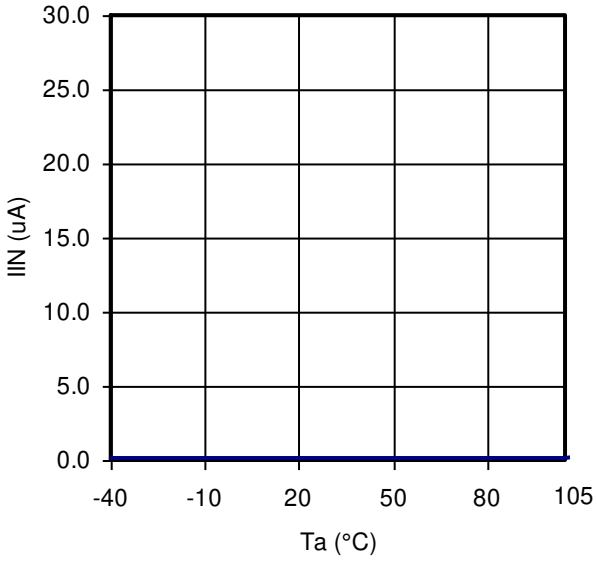


Figure.48 Ta-I_{INSTB}

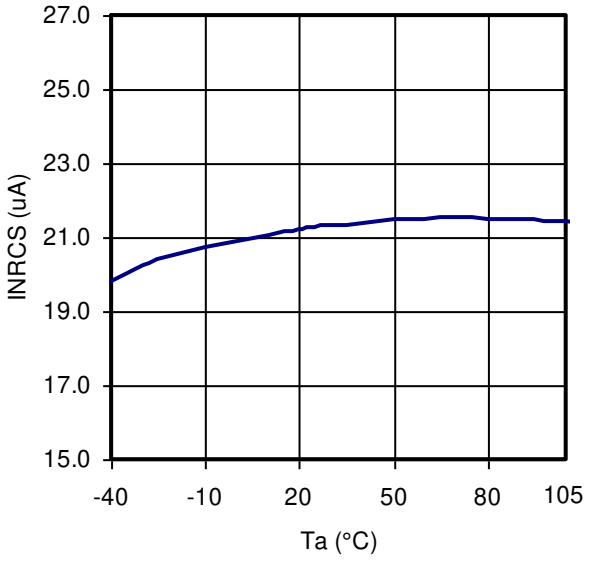


Figure.49 Ta-I_{INRCS}

Typical Performance Curves - continued

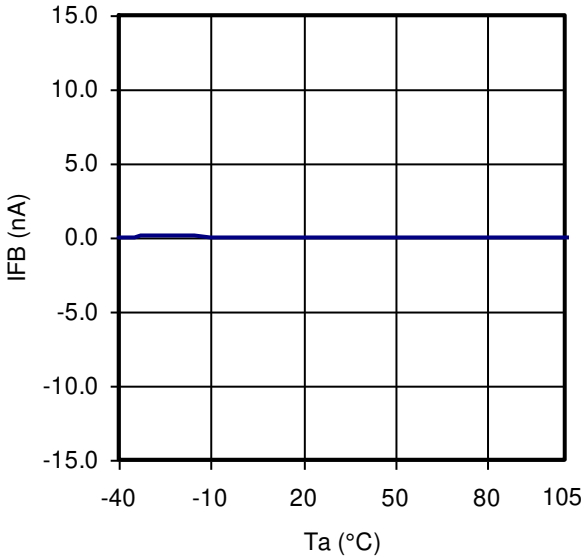


Figure.50 Ta-I_{FB}

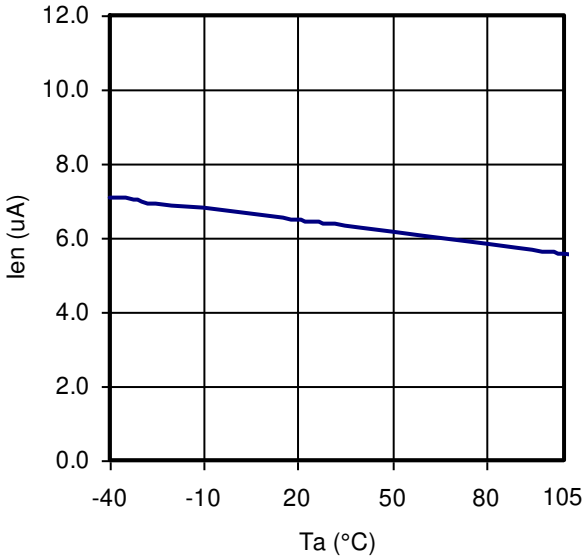


Figure.51 Ta-I_{EN}

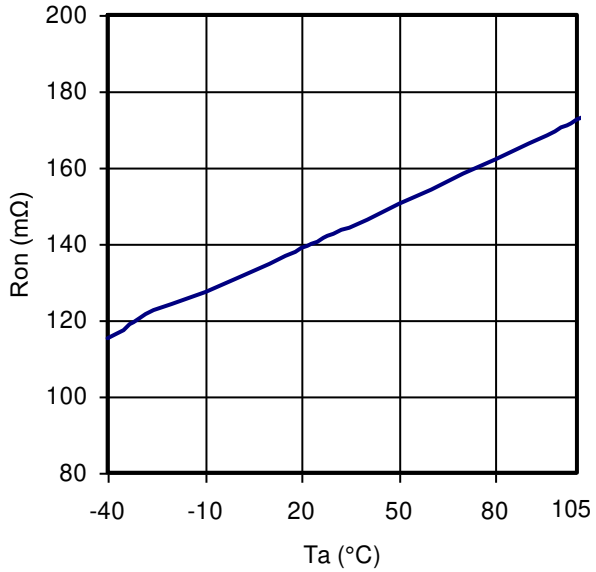


Figure.52 Ta-R_{ON}
(V_{CC}=5V, V_O=1.2V)

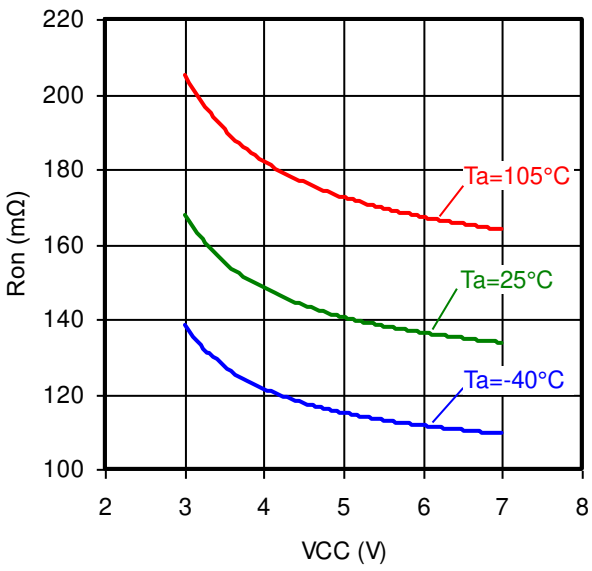
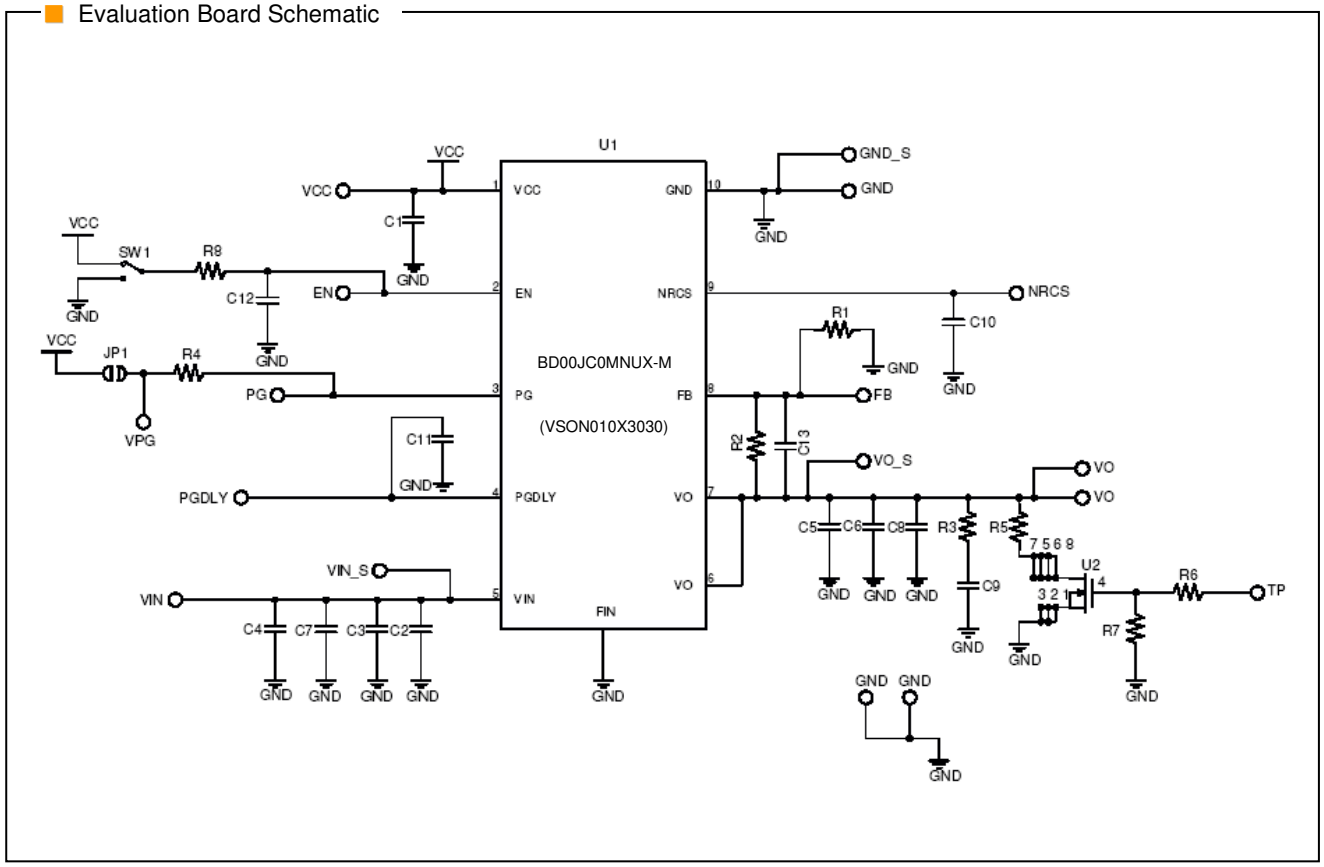


Figure.53 V_{CC}-R_{ON}

Evaluation Board

Evaluation Board Schematic



Evaluation Board Standard Component List

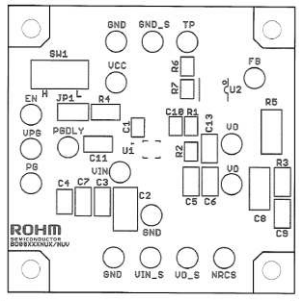
Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD00JC0MNUX-M
C1	1uF	MURATA	GRM188B11A105KD
C10	0.01uF	MURATA	GRM188B11H103KD
C11	100pF	MURATA	GRM188B11H101KD
R8	0Ω	-	Jumper
C5	22uF	KYOCERA	CM32X5R226M10A

Component	Rating	Manufacturer	Product Name
C2	22uF	KYOCERA	CM32X5R226M10A
C13	1000pF	MURATA	GRM188B11H102KD
R1	3.9kΩ	ROHM	MCR03EZPF3901
R2	3.3kΩ	ROHM	MCR03EZPF3301
R4	100kΩ	ROHM	MCR03EZPF

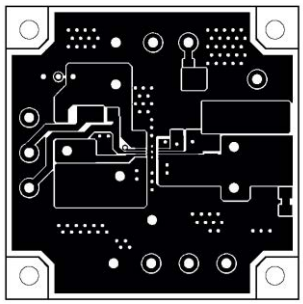
Evaluation Board Layout

(2nd layer and 3rd layer are GND Line)

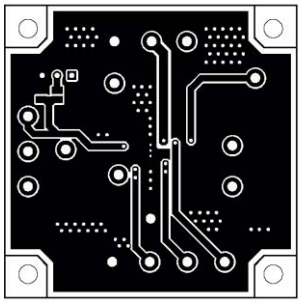
Silkscreen



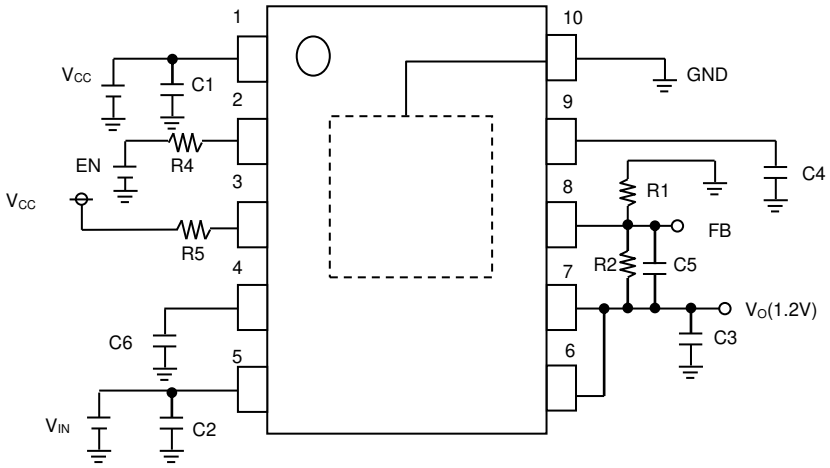
TOP Layer



Bottom Layer



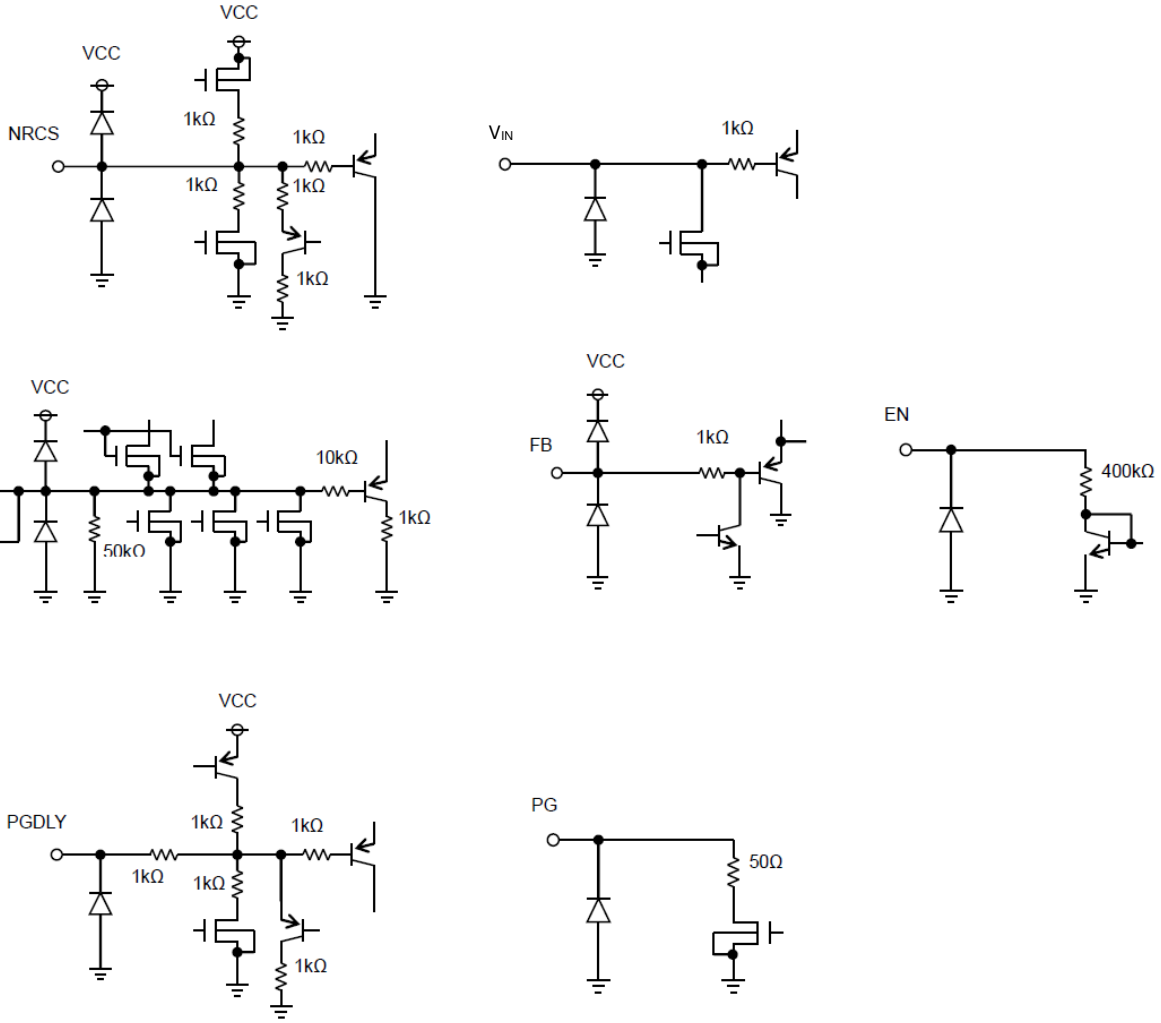
Recommended Circuit Example



Component	Recommended Value	Programming Notes and Precautions
R1/R2	3.9k/3.3k	IC output voltage can be set with a configuration formula using the values for the internal reference output voltage (V_{FB}) and the output voltage resistors (R1, R2). Select resistance values that will avoid the impact of the V_{REF} current (±100nA). The recommended total resistance value is 10KΩ.
C3	22µF	To assure output voltage stability, there should be capacitor connected across V_O pins and the GND pin. Output capacitor plays a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22µF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.
C1	1µF	Input capacitor reduce the output impedance of the voltage supply source connected to the (V_{CC}) input pin. If the impedance of this power supply increases, input voltage (V_{CC}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 1µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C2	22µF	Input capacitor reduce the output impedance of the voltage supply source connected to the (V_{IN}) input pin. If the impedance of this power supply increases, input voltage (V_{IN}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 22µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C4	0.01µF	The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (V_{IN} to V_O) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.
C5	-	This component is employed when the C3 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.
C6	100pF	Capacitor to set delay of power good. 100pF is recommended.
R5	100k	It is pull-up resistance of Open Drain pin. 100kΩ is recommended.
R4	Several kΩ ～several 10kΩ	It is recommended that a resistance (several kΩ to several 10kΩ) be place in R4, in case negative voltage is applied in EN pin.

I/O Equivalent Circuit Diagram

(Resistance value is Typical)



Notes for Use

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND Voltage
   The potential of GND pin must be minimum potential in all operating conditions.

3. Thermal design
   Use a thermal design that allows for a sufficient margin considering the power dissipation (Pd) in actual operating conditions.

4. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

5. ASO
   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

6. Thermal shutdown circuit
   The IC incorporates a built-in thermal shutdown circuit (TSD circuit: Latch type). The thermal shutdown circuit (TSD circuit: Latch type) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation.
   Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD ON temperature [℃] (typ.)	Hysteresis temperature [℃] (typ.)
175	15

7. Ground Wiring Pattern
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components.

8. Output voltage resistance setting (R1, R2)
   Output voltage is adjusted with resistor R1 and R2. Output voltage is calculated as $V_{FB} \times (R1+R2) / R1$. Total 10kΩ is recommended so that the output voltage is not affected by the V_{FB} bias current.

9. Output capacitor (C3)
   To assure output voltage stability, there should be capacitor connected across V_O pins and the GND pin. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 47uF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.

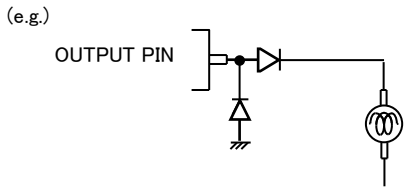
10. Input capacitors setting (C1, C2)
    Input capacitors reduce the impedance of the voltage supply source connected to the (V_{CC}, V_{IN}) input pins. If the impedance of this power supply increases, input voltage (V_{CC}, V_{IN}) could become unstable, leading to oscillation or lowered ripple rejection function. Stability highly depends on the input power supply characteristic and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

11. NRCS pin capacitors setting (CNRCS)
The Non Rush Current on Startup (NRCS) function is built in the IC to prevent rush current from going through the load (V_{IN} to V_O) and impacting output capacitors at power supply start-up. The constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. To obtain a stable NRCS delay time, capacitors with low susceptibility to temperature are recommended.

12. Input pins (V_{CC}, V_{IN}, EN)
This IC's EN pin, V_{IN} pin, and V_{CC} pin are isolated, and the UVLO function is built in the V_{CC} pin to prevent undervoltage lockout. It does not depend on the Input pin order. Output voltage starts up when V_{CC} and EN reach the threshold voltage. However, note that when putting in V_{IN} pin lastly, V_O may result in overshooting.

13. Heat sink (FIN)
Since the heat sink (FIN) is connected to with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to substrate. Please solder properly.

14. Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at start-up or in output OFF condition.



15. Short-circuits between pins and mounting errors
Please be sure to install the IC in correct position and orientation. Mounting errors, such as incorrect positioning or orientation, or connecting of the power supply in reverse polarity can also destroy the IC. Short-circuit between pins or pin and the power supply, or between ground may also damage to the IC.

Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 105°C.
2. Chip junction temperature (Tj) can be no higher than 150°C.

Chip junction temperature can be determined as follows:

①Calculation based on ambient temperature (Ta)

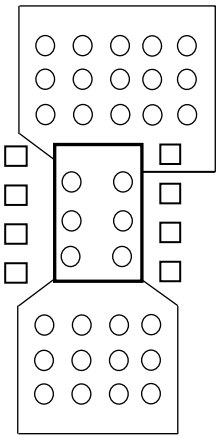
Tj=Ta+θj-a X W

< Reference values >

θ j-a:VSON010X3030	215°C/W	1-layer substrate (Bottom copper foil area: 6.28mm^2)
	69.4°C/W	4-layer substrate (Bottom copper foil area: 6.28mm^2)

PCB size: 74.2mm × 74.2mm × 1.6mm (substrate with thermal via)

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 3.0mm × 3.0mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below) enables to get the superior heat radiation characteristic. (The figure below shows the recommended VIA size and the number suitable for the actual situation.)



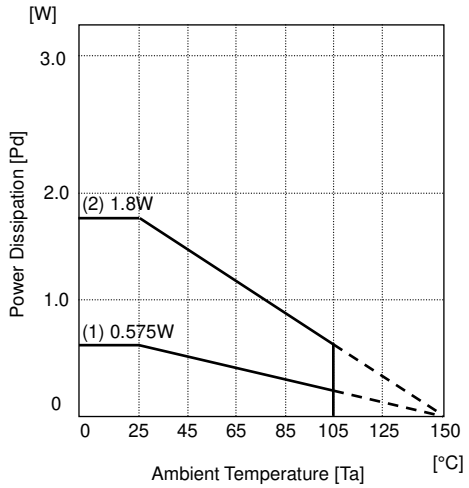
Most of the heat loss that occurs in the BD00JC0MNUX-M is generated from the output Nch FET. Power loss is determined by the total VIN-Vo voltage and output current. Be sure to confirm the system's input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the VIN and Vo in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD00JC0MNUX-M) considering other factor such as substrate size into the thermal design.

Power consumption (W) = { Input voltage (V_{IN})- Output voltage (Vo) (Vo≒VREF) } x Io(Ave)

Example: When V_{IN}=1.7V, V_O=1.2V, Io(Ave) = 1A,
Power consumption (W) = { 1.7(V)-1.2(V) } x 1.0(A)
= 0.5(W)

Power Dissipation

VSON010X3030



(1) Mounted on 1-layer board
Bottom copper foil area: 6.28mm^2
θj-a=215.5°C/W

(2) Mounted on 4-layer board
Bottom copper foil area: 6.28mm^2
θj-a=69.4°C/W

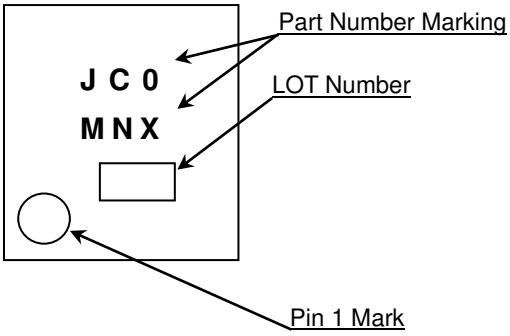
Ordering Information

B D 0 0 J C 0 M N U X	-	M E 2

Part Number	Output voltage	Input Voltage	Output Current	Automotive	Package	Packaging and forming specification
	00:Variable	J:6V	C0:1A	“M”:M-series	NUX:VSON010X3030	E2:Emboss tape reel

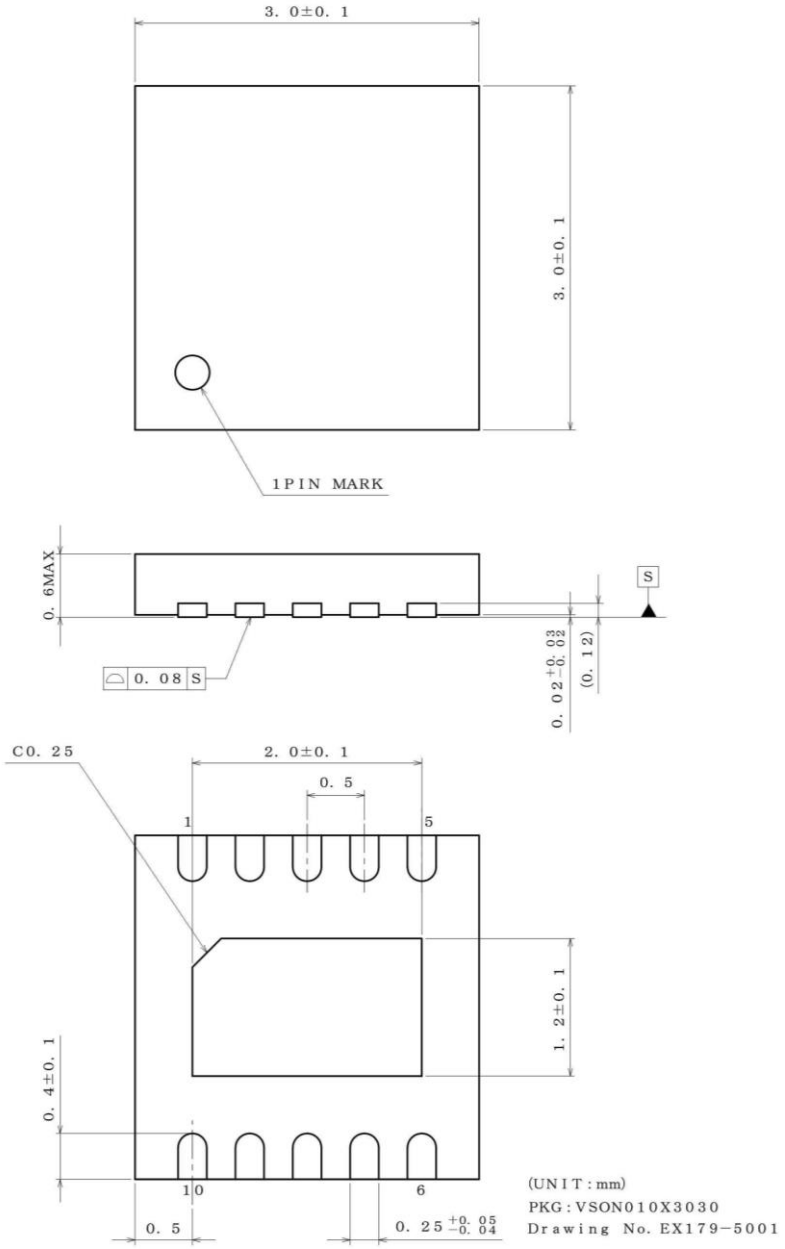
Marking Diagram

VSON010X3030 (TOP VIEW)



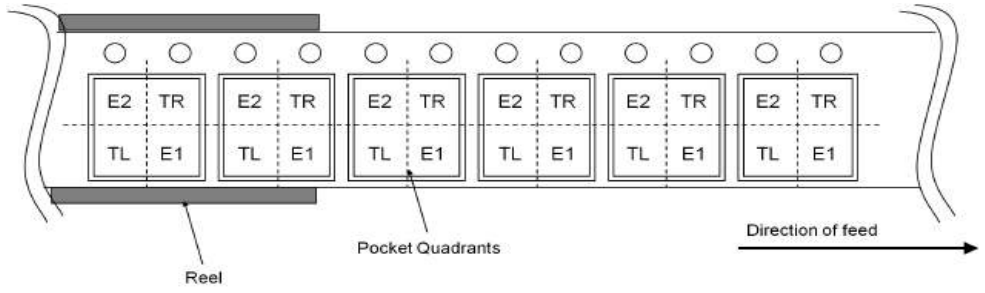
Physical Dimension and Packing Information

Package Name	VSON010X3030



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
2.Dec.2013	001	New Release
19.Apr.2022	002	P4: A writing errors of Timing Chart was corrected. P11 and P12: A writing errors of Figure.20 to Figure.25 was corrected. P22: I/O Equivalent Circuit Diagram was fixed. P22: Reference landing pattern was removed. P25: A writing errors of Heat Loss was corrected. P25: A writing errors of Power Dissipation was corrected. P26: Add Marking Diagram. P27: Add Physical Dimension and Packing Information.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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