

November 1994

CMOS 8-Bit Microprocessor

Hardware Features

- Typical Full Speed Operating Power @ 5V 35mW
- Typical WAIT Mode Power 5mW
- Typical STOP Mode Power 25 μ W
- 112 Bytes of On-Chip RAM
- 16 Bidirectional I/O Lines on CDP 6805E2
- 13 Bidirectional I/O Lines on CDP6805E3
- Internal 8-Bit Timer with Software Programmable 7-Bit Prescaler
- External Timer Input
- Full External and Timer Interrupts
- Multiplexed Address/Data Bus
- Master Reset and Power-On Reset
- CDP6805E2 is Capable of Addressing up to 8K Bytes of External Memory
- CDP6805E3 is Capable of Addressing up to 64K Bytes of External Memory
- Single 3V to 6V Supply
- On-Chip Oscillator
- 40 Pin Dual-in-Line Package (E Suffix)
- 44 Lead Plastic Chip Carrier Package (Q Suffix)
- -40°C to +85°C Operation With CDP6805E2C and CDP6805E3C

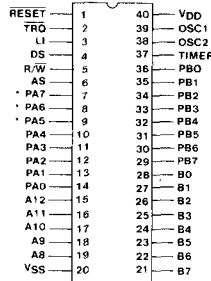
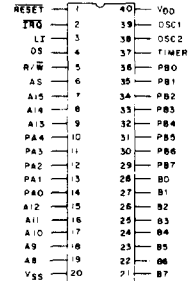
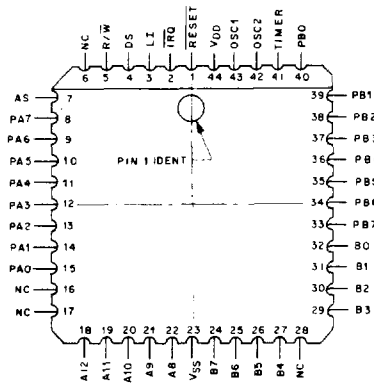
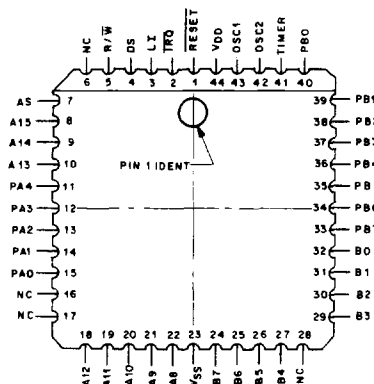
Software Features

- Efficient Use of Program Space
- Versatile Interrupt Handling
- True Bit Manipulation
- Addressing Modes With Indexed Addressing for Tables
- Efficient Instruction Set
- Memory Mapped I/O
- Two Power Saving Standby Modes

Description

The CDP6805E2 and CDP6805E3 Microprocessors Unit (MPUs) belong to the CDP6805 Family of CMOS Microcomputers. These 8-bit fully static and expandable microprocessors contain a CPU, on-chip RAM, I/O and Timer. They are low power, low cost processors designed for mid-range applications in the consumer, automotive, industrial and communications markets where very low power consumption constitutes an important factor. The major features of the CDP6805E2 and CDP6805E3 MPUs are listed under "Hardware Features" and "Software Features".

Pinouts

**CDP6805E2 40 LEAD DIP
TOP VIEW**

**CDP6805E3 40 LEAD DIP
TOP VIEW**

**CDP6805E2 44 PLCC
TOP VIEW**

**CDP6805E3 44 PLCC
TOP VIEW**


CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

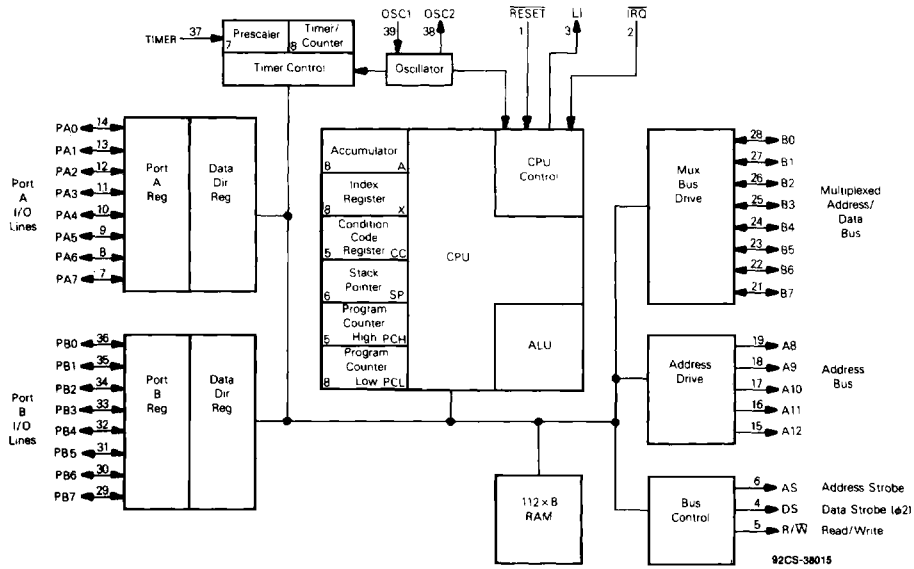


Fig. 1a - CDP6805E2 block diagram.

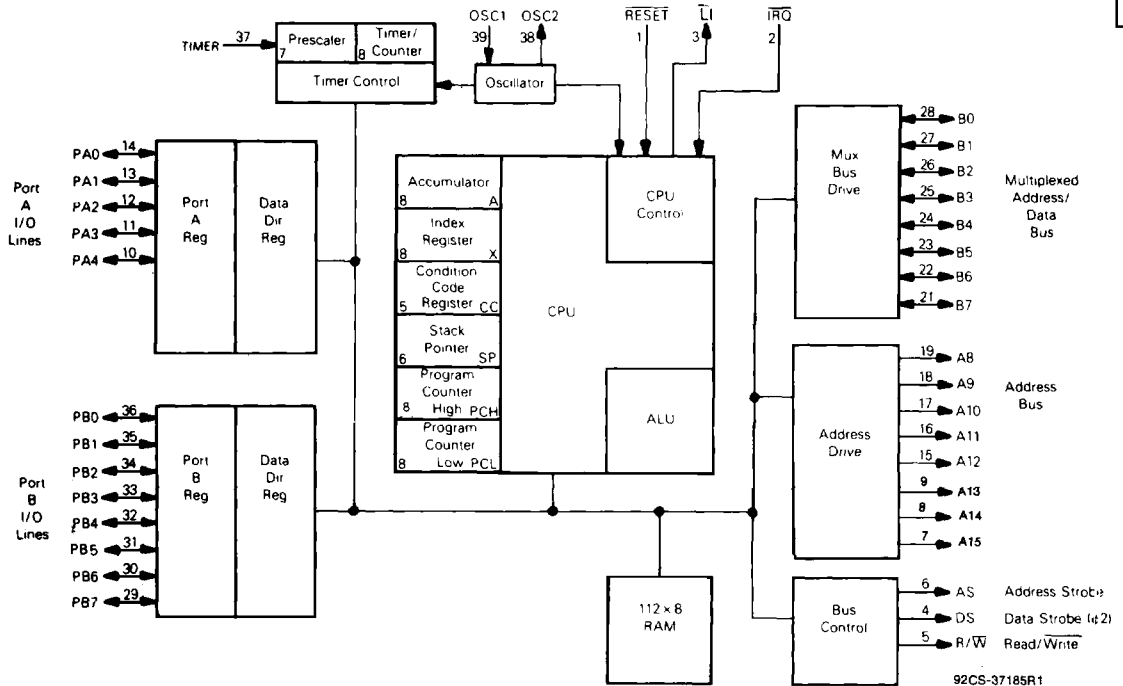


Fig. 1b - CDP6805E3 block diagram.

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MICRO-PROCESSORS

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

MAXIMUM RATINGS (voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V _{DD}	-0.3 to +8.0	V
All Input Voltages Except OSC1	V _{in}	V _{SS} - 0.5 to V _{DD} + 0.5	V
Current Drain Per Pin Excluding V _{DD} and V _{SS}	I	10	mA
Operating Temperature Range CDP6805E2, CDP6805E3 CDP6805E2C, CDP6805E3C	T _A	T _L to T _H 0 to 70 -40 to 85	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS 3.0 V (V_{DD}=3 Vdc, V_{SS}=0, T_A=T_L to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage I _{LOAD} ≤ 10.0 μA	V _{OL} V _{OH}	- V _{DD} - 0.1	0.1 -	V
Total Supply Current (C _L = 50 pF -- no DC loads) t _{cyc} = 5 μs				
Run (V _{IL} = 0.2 V, V _{IH} = V _{DD} - 0.2 V)	I _{DD}	-	1.3	mA
Wait (Test Conditions -- See Note Below)	I _{DD}	-	200	μA
Stop (Test Conditions -- See Note Below)	I _{DD}	-	100	μA
Output High Voltage				
(I _{LOAD} = 0.25 mA) A8-A15, B0-B7	V _{OH}	2.7	-	V
(I _{LOAD} = 0.1 mA) PA0-PA7, PB0-PB7	V _{OH}	2.7	-	V
(I _{LOAD} = 0.25 mA) DS, AS, R/W	V _{OH}	2.7	-	V
Output Low Voltage				
(I _{LOAD} = 0.25 mA) A8-A15, B0-B7	V _{OL}	-	0.3	V
(I _{LOAD} = 0.25 mA) PA0-PA7, PB0-PB7	V _{OL}	-	0.3	V
(I _{LOAD} = 0.25 mA) DS, AS, R/W	V _{OL}	-	0.3	V
Input High Voltage				
PA0-PA7, PB0-PB7, B0-B7	V _{IH}	2.1	-	V
TIMER, I _{RQ} , RESET	V _{IH}	2.5	-	V
OSC1	V _{IH}	2.1	-	V
Input Low Voltage (All inputs)	V _{IL}	-	0.5	V
Frequency of Operation				
Crystal	f _{OSC}	0.032	1.0	MHz
External Clock	f _{OSC}	DC	1.0	MHz
Input Current				
RESET, I _{RQ} , Timer, OSC1	I _{in}	-	±1	μA
Three-State Output Leakage				
PA0-PA7, PB0-PB7, B0-B7	I _{TSL}	-	±10	μA
Capacitance				
RESET, I _{RQ} , Timer	C _{in}	-	8.0	pF
Capacitance				
DS, AS, R/W, A8-A15, PA0-PA7, PB0-PB7, B0-B7	C _{out}	-	12.0	pF

NOTE: Test conditions for Quiescent Current Values are:

Port A and B programmed as inputs.

V_{IL} = 0.2 V for PA0-PA7, PB0-PB7, and B0-B7.

V_{IH} = V_{DD} - 0.2 V for RESET, I_{RQ}, and Timer.

OSC1 input is a squarewave from V_{SS} + 0.2 V to V_{DD} - 0.2 V.

OSC2 output load (including tester) is 35 pF maximum.

Wait mode I_{DD} is affected linearly by this capacitance.

NOTE: References to PA5-7 pertain to CDP6805E2 and references to A13-15 pertain to CDP6805E3.

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

DC ELECTRICAL CHARACTERISTICS 5.0 V ($V_{DD}=5\text{ Vdc} \pm 10\%$, $V_{SS}=0$, $T_A=T_L$ to T_H , unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10.0\ \mu\text{A}$	V_{OL}	–	0.1	V
	V_{OH}	$V_{DD}-0.1$	–	V
Total Supply Current ($C_L = 130\ \text{pF}$ – On Bus, $C_L = 50\ \text{pF}$ – On Ports, No DC Loads, $t_{CYC} = 1.0\ \mu\text{s}$)	I_{DD}	–	10	mA
Run ($V_{IL} = 0.2\ \text{V}$, $V_{IH} = V_{DD} - 0.2\ \text{V}$)				
Wait (Test Conditions – See Note Below)	I_{DD}	–	1.5	mA
Stop (Test Conditions – See Note Below)	I_{DD}	–	200	μA
Output High Voltage				
($I_{LOAD} = 1.6\ \text{mA}$) A8–A15, B0–B7	V_{OH}	4.1	–	V
($I_{LOAD} = 0.36\ \text{mA}$) PA0–PA7, PB0–PB7	V_{OH}	4.1	–	V
($I_{LOAD} = 1.6\ \text{mA}$) DS, AS, R/W	V_{OH}	4.1	–	V
Output Low Voltage				
($I_{LOAD} = 1.6\ \text{mA}$) A8–A15, B0–B7	V_{OL}	–	0.4	V
($I_{LOAD} = 1.6\ \text{mA}$) PA0–PA7, PB0–PB7	V_{OL}	–	0.4	V
($I_{LOAD} = 1.6\ \text{mA}$) DS, AS, R/W	V_{OL}	–	0.4	V
Input High Voltage				
PA0–PA7, PB0–PB7, B0–B7	V_{IH}	$V_{DD}-2.0$	–	V
TIMER, $\overline{\text{IRQ}}$, RESET	V_{IH}	$V_{DD}-0.8$	–	V
OSC1	V_{IH}	$V_{DD}-1.5$	–	V
Input Low Voltage (All Inputs)	V_{IL}	–	0.8	V
Frequency of Operation				
Crystal	f_{OSC}	0.032	5.0	MHz
External Clock	f_{OSC}	DC	5.0	MHz
Input Current				
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, Timer, OSC1	I_{in}	–	± 1	μA
Three-State Output Leakage				
PA0–PA7, PB0–PB7, B0–B7	I_{TSI}	–	± 10	μA
Capacitance				
RESET, $\overline{\text{IRQ}}$, Timer	C_{in}	–	8.0	pF
Capacitance				
DS, AS, R/W, A8–A15, PA0–PA7, PB0–PB7, B0–B7	C_{out}	–	12.0	pF

NOTE: Test conditions for Quiescent Current Values are:
 Port A and B programmed as inputs
 $V_{IL} = 0.2\ \text{V}$ for PA0–PA7, PB0–PB7, and B0–B7
 $V_{IH} = V_{DD} - 0.2\ \text{V}$ for RESET, $\overline{\text{IRQ}}$, and Timer.

OSC1 input is a squarewave from $V_{SS} + 0.2\ \text{V}$ to $V_{DD} - 0.2\ \text{V}$.
 OSC2 output load (including tester) is 35 pF maximum.
 Wait mode (I_{DD}) is affected linearly by this capacitance.

NOTE: References to PA5–7 pertain to CDP6805E2 and references to A13–15 pertain to CDP6805E3.

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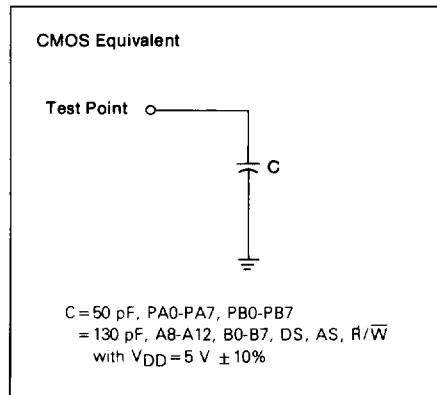
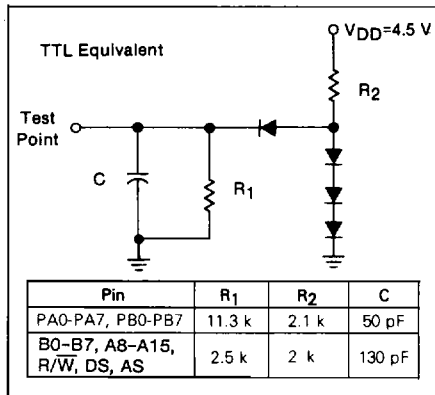
MICRO-PROCESSORS

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

TABLE 1 — CONTROL TIMING ($V_{SS}=0$, $T_A=T_L$ to T_H)

Characteristics	Symbol	$V_{DD}=3\text{ V}$ $f_{OSC}=1\text{ MHz}$			$V_{DD}=5\text{ V} \pm 10\%$ $f_{OSC}=5\text{ MHz}$			Unit
		Min	Typ	Max	Min	Typ	Max	
I/O Port Timing — Input Setup Time (Figure 3)	t_{PVASL}	500	—	—	250	—	—	ns
Input Hold Time (Figure 3)	t_{ASLPX}	100	—	—	100	—	—	ns
Output Delay Time (Figure 3)	t_{ASLPV}	—	—	0	—	—	0	ns
Interrupt Setup Time (Figure 6)	t_{ILASL}	2	—	—	0.4	—	—	μs
Crystal Oscillator Startup Time (Figure 5)	t_{OXOV}	—	30	300	—	15	100	ms
Wait Recovery Startup Time (Figure 7)	t_{IVASH}	—	—	10	—	—	2	μs
Stop Recovery Startup Time (Crystal Oscillator) (Figure 8)	t_{ILASH}	—	30	300	—	15	100	ms
Required Interrupt Release (Figure 6)	t_{DSLH}	—	—	5	—	—	1.0	μs
Timer Pulse Width (Figure 7)	t_{TH}, t_{TL}	0.5	—	—	0.5	—	—	t_{cyc}
Reset Pulse Width (Figure 5)	t_{RL}	5.2	—	—	1.05	—	—	μs
Timer Period (Figure 7)	t_{TLTL}	1.0	—	—	1.0	—	—	t_{cyc}
Interrupt Pulse Width Low (Figure 16)	t_{ILIH}	1.0	—	—	1.0	—	—	t_{cyc}
Interrupt Pulse Period (Figure 16)	t_{ILIL}	*	—	—	*	—	—	t_{cyc}
Oscillator Cycle Period (1/5 of t_{cyc})	t_{OLOL}	1000	—	—	200	—	—	ms
OSC1 Pulse Width High	t_{OH}	350	—	—	75	—	—	ns
OSC1 Pulse Width Low	t_{OL}	350	—	—	75	—	—	ns

* The minimum period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.

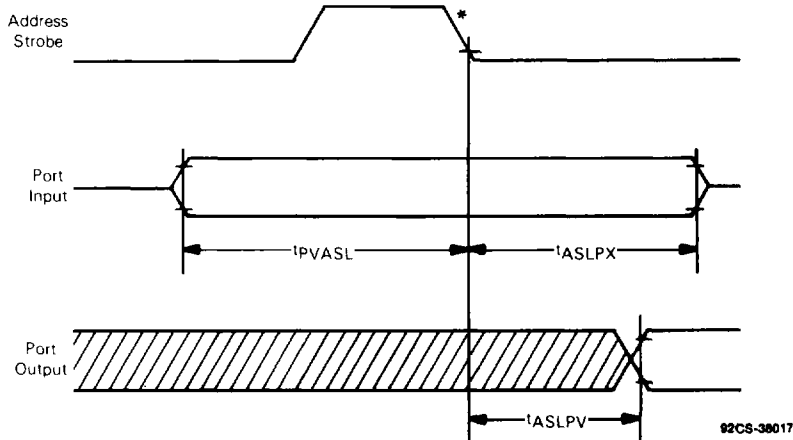


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Fig. 2 - Equivalent test-load circuits.

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

($V_{LOW} = 0.8 \text{ V}$, $V_{HIGH} = V_{DD} - 2 \text{ V}$, $V_{DD} = 5 \pm 10\%$
 Temp = 0° to 70°C , C_L on Port = 50 pF , $f_{OSC} = 5 \text{ MHz}$)

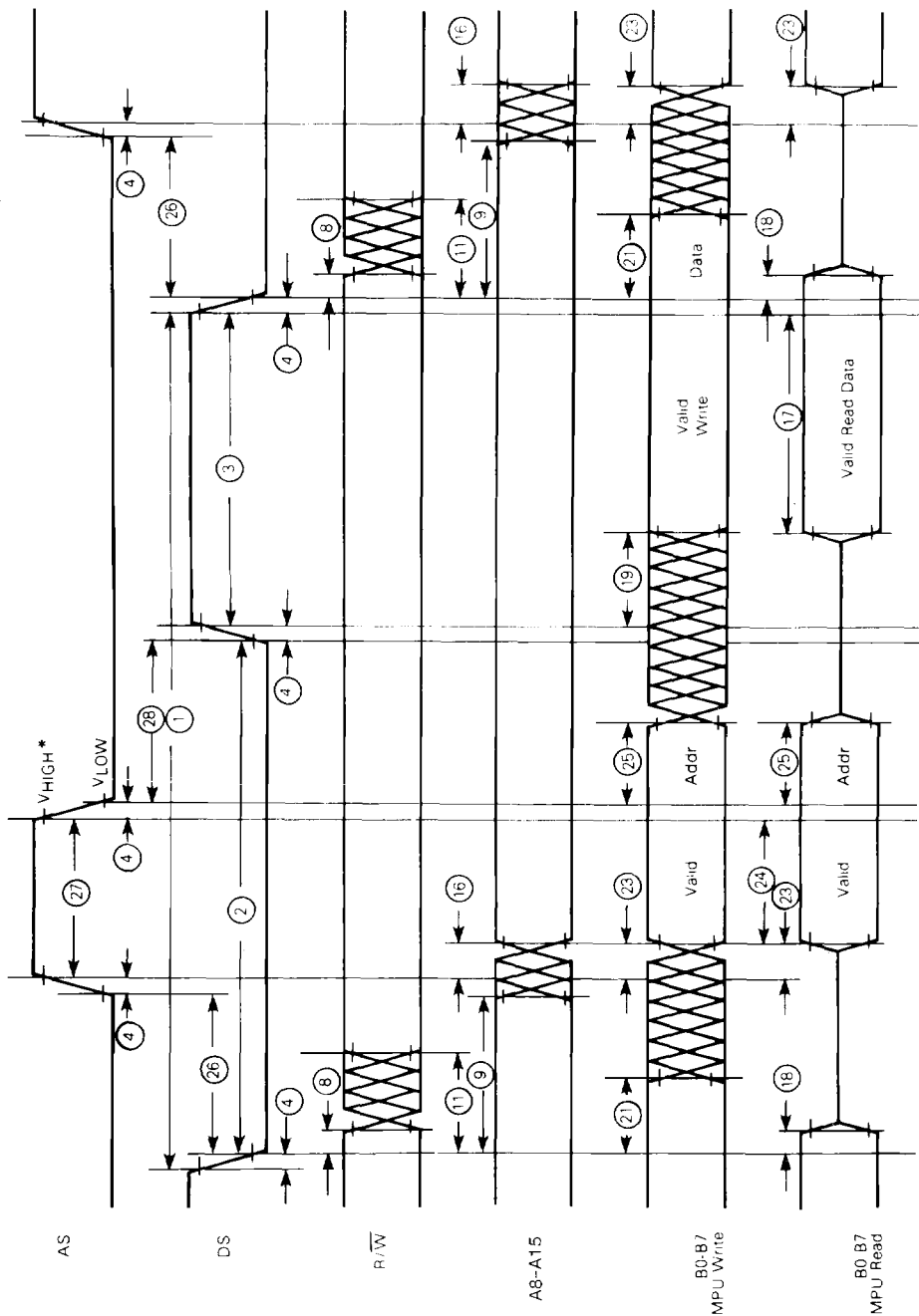


*The address strobe of the first cycle of the next instruction as shown in Table 11.

Fig. 3 - I/O port timing waveforms.

TABLE 2 - BUS TIMING ($T_A = T_L$ to T_H , $V_{SS} = 0 \text{ V}$) See Figure 4

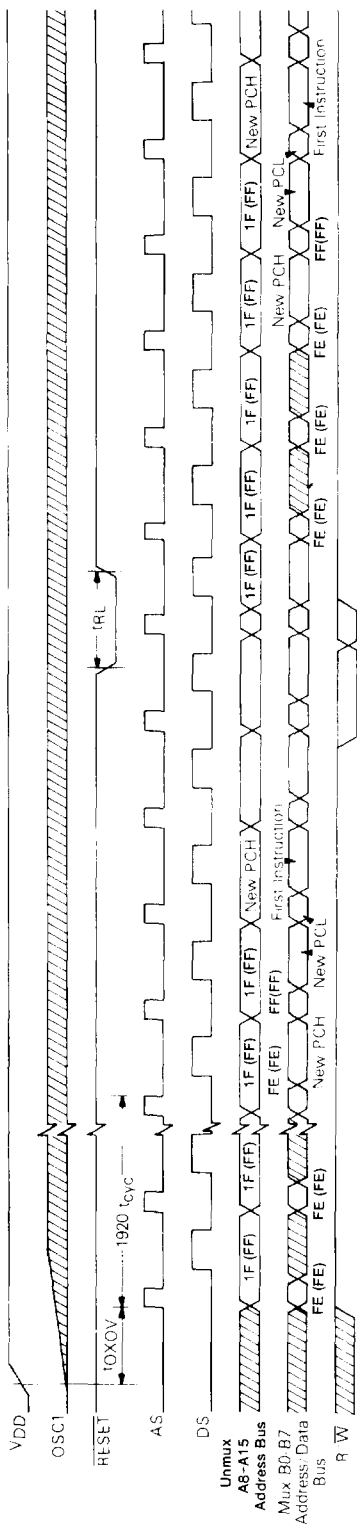
Num	Characteristics	Symbol	$f_{OSC} = 1 \text{ MHz}$, $V_{DD} = 3 \text{ V}$ 50 pF Load		$f_{OSC} = 5 \text{ MHz}$, $V_{DD} = 5 \text{ V} \pm 10\%$, 1 TTL and 130 pF Load		Unit
			Min	Max	Min	Max *	
1	Cycle Time	t_{cyc}	5000	DC	1000	DC	ns
2	Pulse Width, DS Low	PW_{EL}	2800	—	560	—	ns
3	Pulse Width, DS High or RD, WR, Low	PW_{EH}	1800	—	375	—	ns
4	Clock Transition	t_r, t_f	—	100	—	30	ns
8	R/W Hold	t_{RWH}	10	—	10	—	ns
9	Non-Muxed Address Hold	t_{AH}	800	—	100	—	ns
11	R/W Delay from DS Fall	t_{AD}	—	500	—	300	ns
16	Non-Muxed Address Delay from AS Rise	t_{ADH}	0	200	0	100	ns
17	MPU Read Data Setup	t_{DSR}	200	—	115	—	ns
18	Read Data Hold	t_{DHR}	0	1000	0	160	ns
19	MPU Data Delay, Write	t_{DDW}	—	0	—	120	ns
21	Write Data Hold	t_{DHW}	800	—	55	—	ns
23	Muxed Address Delay from AS Rise	t_{BHD}	0	250	0	120	ns
24	Muxed Address Valid to AS Fall	t_{ASL}	600	—	55	—	ns
25	Muxed Address Hold	t_{AHL}	250	750	60	180	ns
26	Delay DS Fall to AS Rise	t_{ASD}	800	—	160	—	ns
27	Pulse Width, AS High	PW_{ASH}	850	—	175	—	ns
28	Delay, AS Fall to DS Rise	t_{ASED}	800	—	160	—	ns



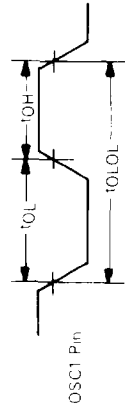
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* V_{HIGH} = -2 V, V_{LOW} = 0.5 V for V_{DD} = 3 V
 V_{HIGH} = V_{DD} - 2 V, V_{LOW} = 0.8 V for V_{DD} = 5 V ± 10 %

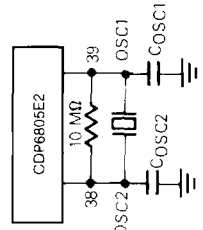
Fig. 4 - Bus timing waveforms.



Oscillator Waveform

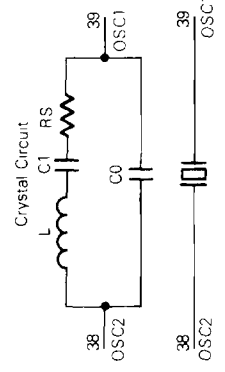


Crystal Oscillator Connections



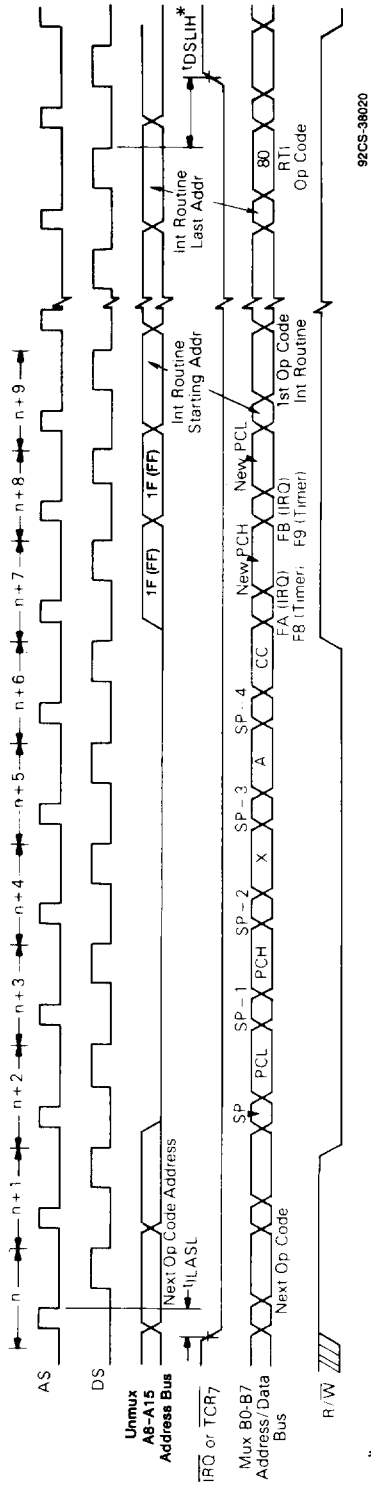
Crystal Parameters Representative Frequencies

	5 MHz	4 MHz	1 MHz
RS max	500	750	4000
C0	8 pF	7 pF	5 pF
C1	0.02 pF	0.012 pF	0.008 pF
Q	50 k	40 k	30 k
C0SC1	15-30 pF	15-30 pF	15-40 pF
C0SC2	15-25 pF	15-25 pF	15-30 pF



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Fig. 5 - Power-on reset and reset timing waveforms.



* tDSUH - The interrupting device must release the IRQ line within this time to prevent subsequent recognition of the same interrupt

Fig. 6 - \overline{IRQ} and \overline{TCR}_7 interrupt timing waveforms.

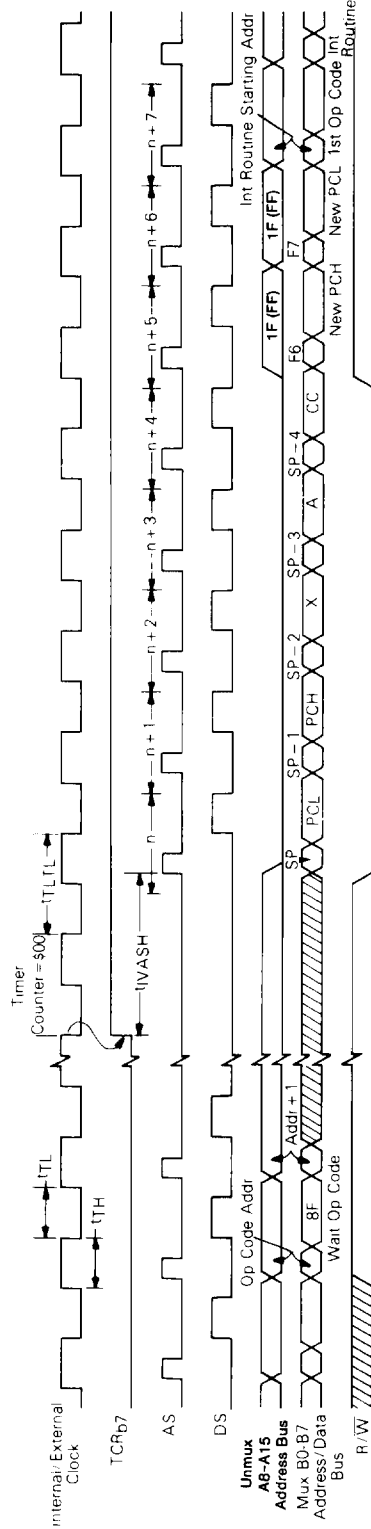
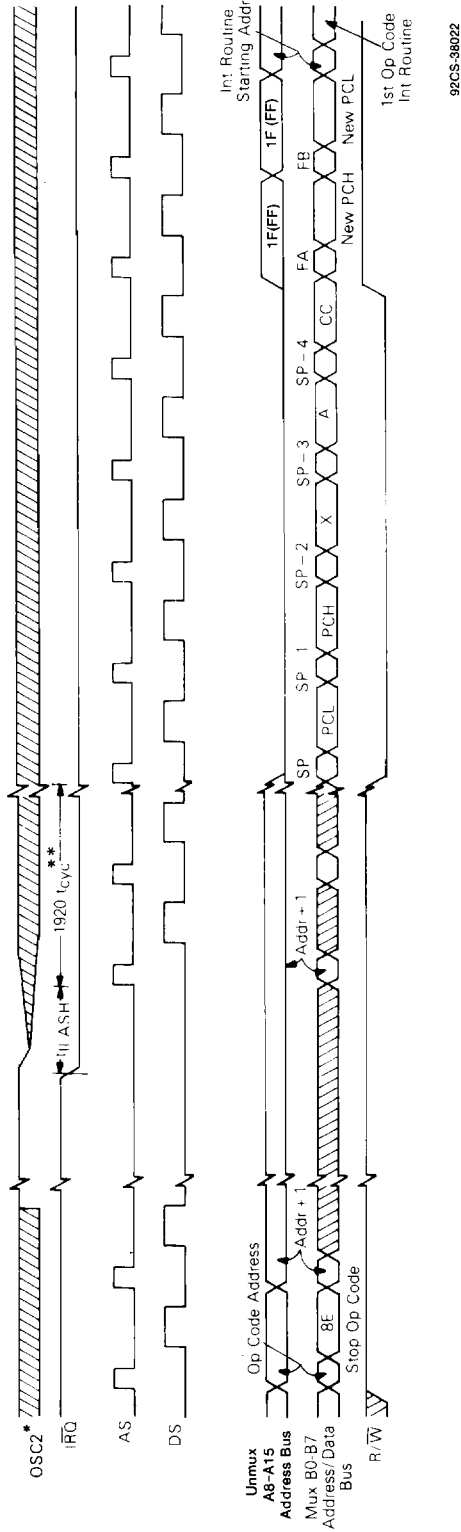


Fig. 7 - Timer interrupt after WAIT instruction timing waveforms.



* Represents the internal gating of the OSC1 input pin.
 ** t_{cyc} is one instruction cycle (for $f_{OSC} = 5 \text{ MHz}$, $t_{cyc} = 1 \mu\text{s}$)

Fig. 8 - Interrupt recovery from STOP instruction timing waveforms.

Functional Pin Description

VDD and VSS - VDD and VSS provide power to the chip. VDD provides power and VSS is ground.

IRQ (Maskable Interrupt Request) - $\overline{\text{IRQ}}$ is a level sensitive and edge sensitive input which can be used to request an interrupt sequence. The MPU completes the current instruction before it responds to the request. If $\overline{\text{IRQ}}$ is low and the interrupt mask bit (I-bit) in the Condition Code Register is clear, the MPU begins an interrupt sequence at the end of the current instruction. The interrupt circuit recognizes both a "Wire ORed" level as well as pulses on the IRQ line (see Interrupt Section for more details). $\overline{\text{IRQ}}$ requires an external resistor to VDD for "Wire OR" operation.

RESET - The $\overline{\text{RESET}}$ input is not required for start up but can be used to reset the MPU's internal state and provide an orderly software start up procedure. Refer to the RESET section for a detailed description.

TIMER - The TIMER input is used for clocking the on chip timer. Refer to TIMER section for a detailed description.

AS (Address Strobe) - Address Strobe (AS) is an output strobe used to indicate the presence of an address on the 8-bit multiplexed bus. The AS line is used to demultiplex the eight least significant address bits from the data bus. A latch controlled by Address Strobe should capture addresses on the negative edge. This output is capable of driving one standard TTL load and 130pF and is available at $f_{\text{OSC}} \div 5$ when the MPU is not in the WAIT or STOP states.

DS (Data Strobe) - This output is used to transfer data to or from a peripheral or memory. DS occurs anytime the MPU does a data read or write. DS also occurs when the MPU does a data transfer to or from the MPU's internal memory. Refer to Table 2 and Figure 4 for timing characteristics. This output is capable of driving one standard TTL

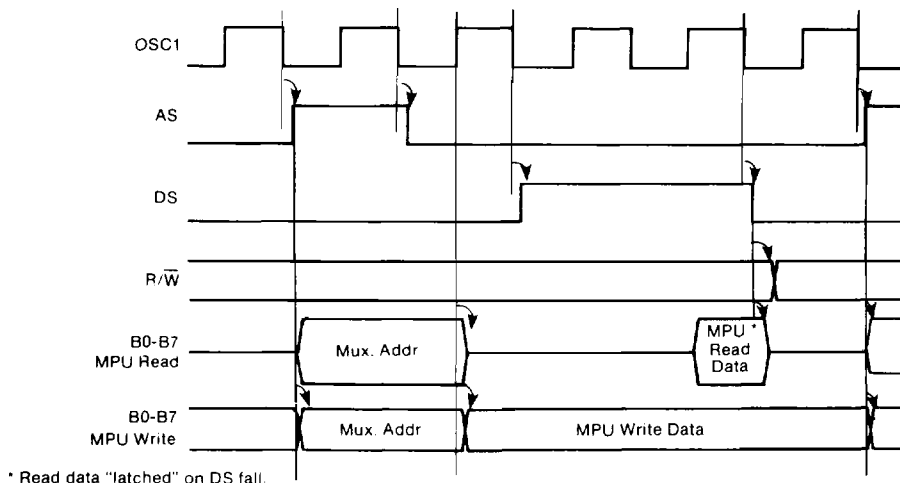
load and 130pF. DS is a continuous signal at $f_{\text{OSC}} \div 5$ when the MPU is not in WAIT or STOP state. Some bus cycles are redundant reads of op code bytes.

R/W (Read/Write) - The R/W output is used to indicate the direction of data transfer for both internal memory and I/O registers, and external peripheral devices and memories. This output is used to indicate to a selected peripheral whether the MPU is going to read or write data on the next Data Strobe (R/W low = processor write; R/W high = processor read). The R/W output is capable of driving one standard TTL load and 130pF. The normal standby state is Read (high).

A8-A15 (High Order Address Lines) - The A8-A15 output lines constitute the higher order non-multiplexed addresses. Each output line is capable of driving one standard TTL load and 130pF.

B0-B7 (Address/Data Bus) - The B0-B7 bidirectional lines constitute the lower order addresses and data. These lines are multiplexed, with address present at Address Strobe time and data present at Data Strobe time. When in the data mode, these lines are bidirectional, transferring data to and from memory and peripheral devices as indicated by the R/W pin. As outputs in either the data or address modes, these lines are capable of driving one standard TTL load and 130pF.

OSC1, OSC2 - The CDP6805E2/3 provides for two types of oscillator inputs — crystal circuit or external clock. The two oscillator pins are used to interface to a crystal circuit, as shown in Figure 5. If an external clock is used, it must be connected to OSC1. The input at these pins is divided by five to form the cycle rate seen on the AS and DS pins. The frequency range is specified by f_{OSC} . The OSC1 to bus transitions relationships are provided in Figure 9 for system designs using oscillators slower than 5 MHz.



* Read data "latched" on DS fall.

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Fig. 9 - OSC1 to bus transitions timing waveforms

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

Crystal — The circuit shown in Figure 5 is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. An external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time.

External Clock — An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 10.

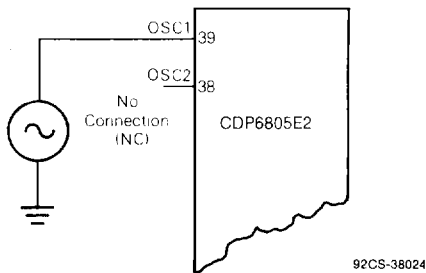
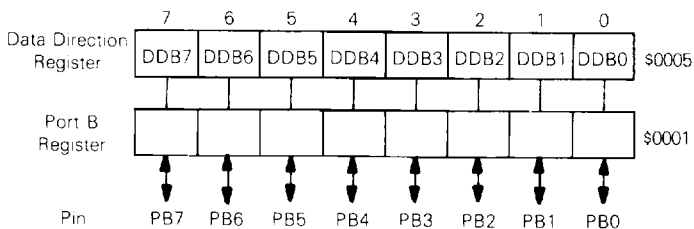
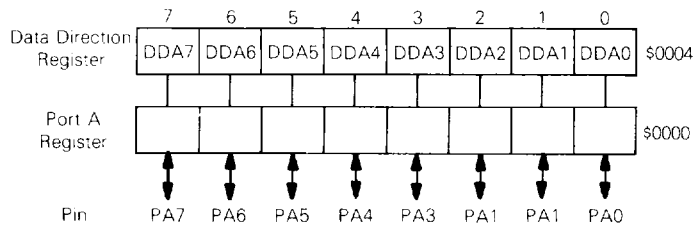


Fig. 10 — External clock connection.

LI (Load Instruction) — This output is used to indicate that a fetch of the next opcode is in progress. LI remains low during an External or Timer interrupt. The LI output is only used for certain debugging and test systems. For normal operations this pin is not connected. The LI output is capable of driving one standard TTL load and 50 pF. This signal overlaps Data Strobe.

PA0-PA7 — These eight pins constitute Input/Output Port A. Each line is individually programmed to be either an input or output under software control via its Data Direction Register as shown below. An I/O pin is programmed as an output when the corresponding DDR bit is set to a "1," and as an input when it is set to a "0". In the output mode the bits are latched and appear on the corresponding output pins. An MPU read of the port bits programmed as outputs reflect the last value written to that location. When programmed as an input, the input data bit(s) are not latched. An MPU read of the port bits programmed as inputs reflects the current status of the corresponding input pins. The Read/Write port timing is shown in Figure 3. See typical I/O Port Circuitry in Figure 11. During a Power-On Reset or external RESET all lines are configured as inputs (zero in Data Direction Register). The output port register is not initialized by reset. The TTL compatible three-state output buffers are capable of driving one standard TTL load and 50 pF. The DDR is a read/write register.

PB0-PB7 — These eight pins interface to Input/Output Port B. Refer to PA0-PA7 description for details of operation.



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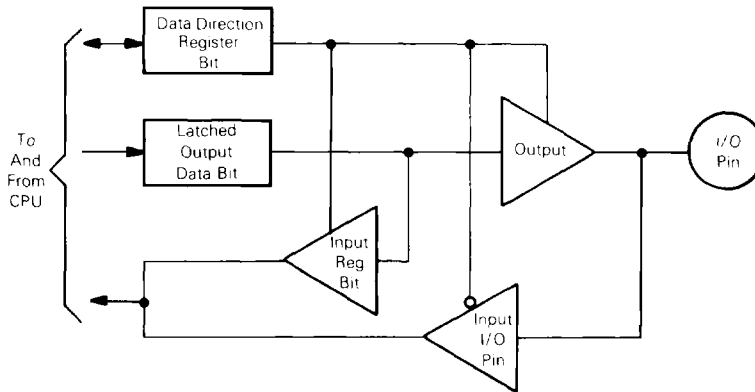


Fig. 11 - Typical I/O port circuitry

TABLE 3 I/O PIN FUNCTIONS

R/W	DDR	I/O PIN FUNCTIONS
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read
1	1	The I/O pin is in an output mode. The output data latch is read.

Functional Description

Throughout the following sections references to CDP6805E2 imply both the CDP6805E2 and the CDP6805E3. Values in parenthesis refer to the CDP6805E3.

Memory Addressing

The CDP6805E2 is capable of addressing 8192 (65,536) bytes of memory and I/O registers. The address space is divided into internal memory space and external memory space, as shown in Figure 12.

The internal memory space is located within the first 128 bytes of memory (first half of page zero) and is comprised of the I/O port locations, timer locations, and 112 bytes of RAM. The MPU can read from or write to any of these locations. A program write to on chip locations is repeated on the external bus to permit off chip memory to duplicate the content of on chip memory. Program reads to on chip locations also appear on the external bus, but the MPU accepts data only from the addressed on chip location. Any read data appearing on the input bus is ignored.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and

subroutine calls. At power up, the stack pointer is set to \$7F and it is decremented as data is pushed onto the stack. When data is removed from the stack, the stack pointer is incremented. A maximum of 64 bytes of RAM is available for stack usage. Since most programs use only a small part of the allotted stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.

All memory locations above location \$007F are part of the external memory map. In addition, ten locations in the I/O portion of the lower 128 bytes of memory space, as shown in Figure 12, are part of the external memory map. All of the external memory space is user definable except the highest 10 locations. Locations \$1FF6 to \$1FFF (\$FFF6 to \$FFFF) of the external address space are reserved for interrupt and reset vectors (see Figure 12).

Registers

The CDP6805E2 contains five registers as shown in the programming model in Figure 13. The interrupt stacking order is shown in Figure 14.

Accumulator (A) - This Accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations.

Index Register (X) - The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit operand which is used to create an effective address. The index register is also used for data manipulations with the Read/Modify/Write type of instructions and as a temporary storage register when not performing addressing operations.

Program Counter (PC) - The program counter is a 13-bit (16-bit) register that contains the address of the next instruction to be executed by the processor.

CDP6805E2, CDP6805E3, CDP6805E2C, CDP6805E3C

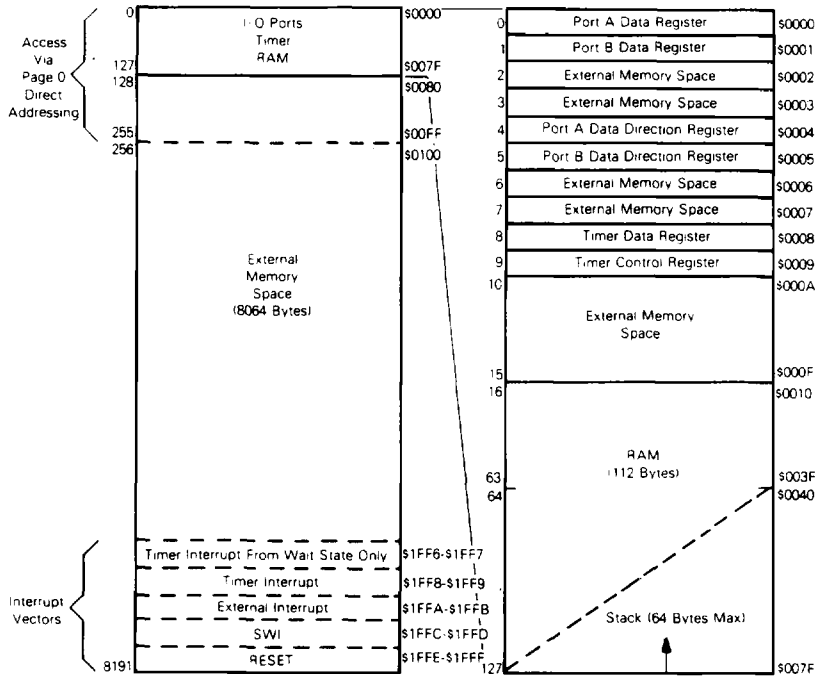


Fig. 12a - CDP6805E2 address map.

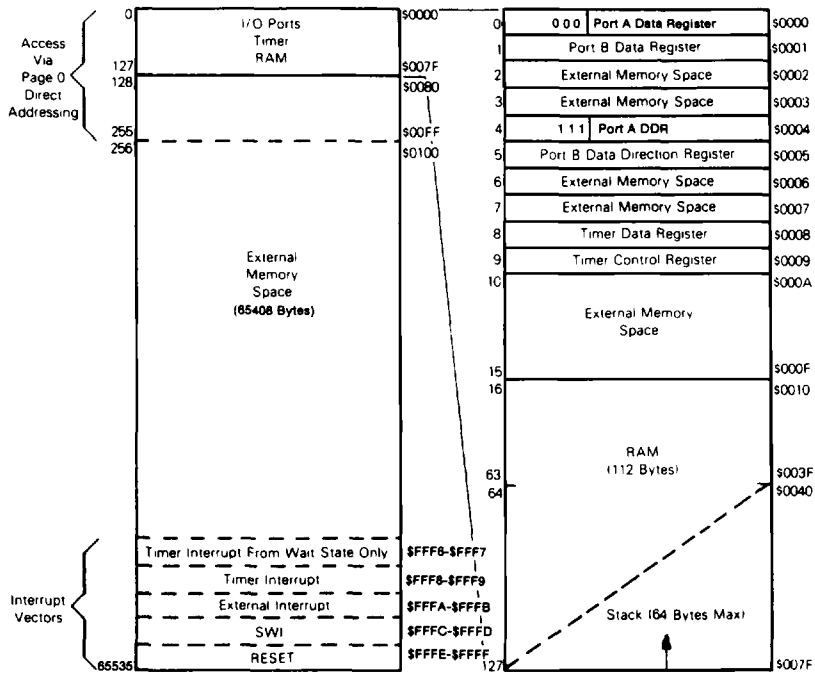


Fig. 12b - CDP6805E3 address map.

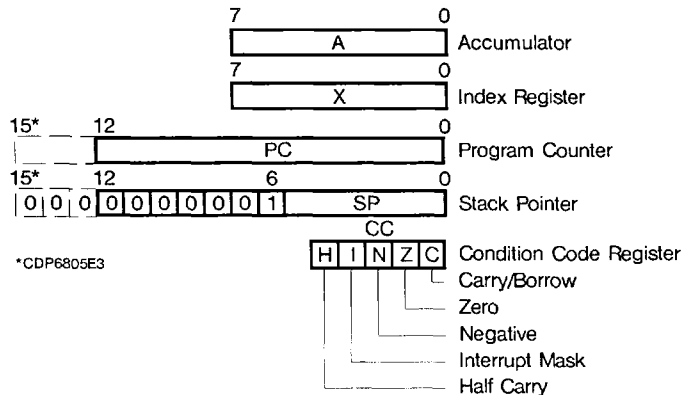
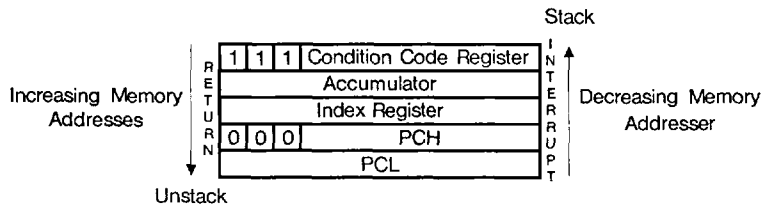


Fig. 13 - Programming model.



NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Fig. 14 - Stacking order.

STACK POINTER (SP) - The stack pointer is a 13-bit (16-bit) register containing the address of the next free location on the stack. When accessing memory, the seven most significant bits are permanently set to 0000001 (0000000001). They are appended to the six least-significant register bits to produce an address within the range of \$007F to \$0040. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit (\$007F). Nested interrupts and/or subroutines may use up to 64 (decimal) locations, beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes.

CONDITION CODE REGISTER (CC) - The condition code register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed. These

bits can be individually tested by a program and specific action taken as a result of their state. Each of the five bits is explained below.

Half Carry Bit (H) - The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H-bit is useful in Binary Coded Decimal addition subroutines.

Interrupt Mask Bit (I) - When the I-bit is set, both the external interrupt and the timer interrupt are disabled. Clearing this bit enables the above interrupts. If an interrupt occurs while the I-bit is set, the interrupt is latched and will be processed when the I-bit is next cleared.

Negative Bit (N) - When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical one).

Zero Bit (Z) - When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry Bit (C) – The C-bit is set when a carry or a borrow out of the ALU occurs during an arithmetic instruction. The C-bit is also modified during bit test, shift, rotate, and branch types of instruction.

Resets

The CDP6805E2 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a Power On Reset function; refer to Figure 5.

RESET (Pin #1) – The $\overline{\text{RESET}}$ input pin is used to reset the MPU and provide an orderly software start up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{Cyc} . The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger to improve its noise immunity capability.

Power On Reset – The Power On Reset occurs when a positive transition is detected on V_{DD} . The Power On Reset is used strictly for power turn on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power down reset. The power on circuitry provides for a $1920 t_{\text{Cyc}}$ delay from the time of the first oscillator operation. If the external reset pin is low at the end of the $1920 t_{\text{Cyc}}$ time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit (bit 7) is cleared to a "0".
- Timer control register interrupt mask bit (bit 6) is set to a "1".
- All data direction register bits are cleared to a "0" (inputs).
- Stack pointer is set to \$007F
- The address bus is forced to the reset vector (\$1FFE, \$1FFF (\$FFE, \$FFF)).
- Condition code register interrupt mask bit (I) is set to a "1"
- STOP and WAIT latches are reset.
- External interrupt latch is reset.

All other functions, such as other registers (including output ports) the timer, etc., are not cleared by the reset conditions.

Interrupts

The CDP6805E2 is capable of operation with three different interrupts, two hardware (timer interrupt and external interrupt) and one software (SWI). When any of these interrupts occur, normal processing is suspended at the end of the current instruction execution. All of the program registers (the machine state) are pushed onto the stack; refer to Figure 14 for stacking order. The appropriate vector pointing to the starting address of the interrupt service routine is then fetched; refer to Figure 15 for the interrupt sequence.

The priority of the various interrupts from highest to lowest is as follows:

RESET → * → External Interrupt → Timer Interrupt

Timer Interrupt – If the timer mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions

from \$01 to \$00) an interrupt request is generated. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I-bit in the condition code register is set. This masks further interrupts until the present one is serviced. The processor now vectors to the timer interrupts service routine. The address for this service routine is specified by the contents of \$1FF8 and \$1FF9 (\$FF8 and \$FF9). The contents of \$1FF6 and \$1FF7 (\$FF6 and \$FF7) specify the service routine. Also, software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

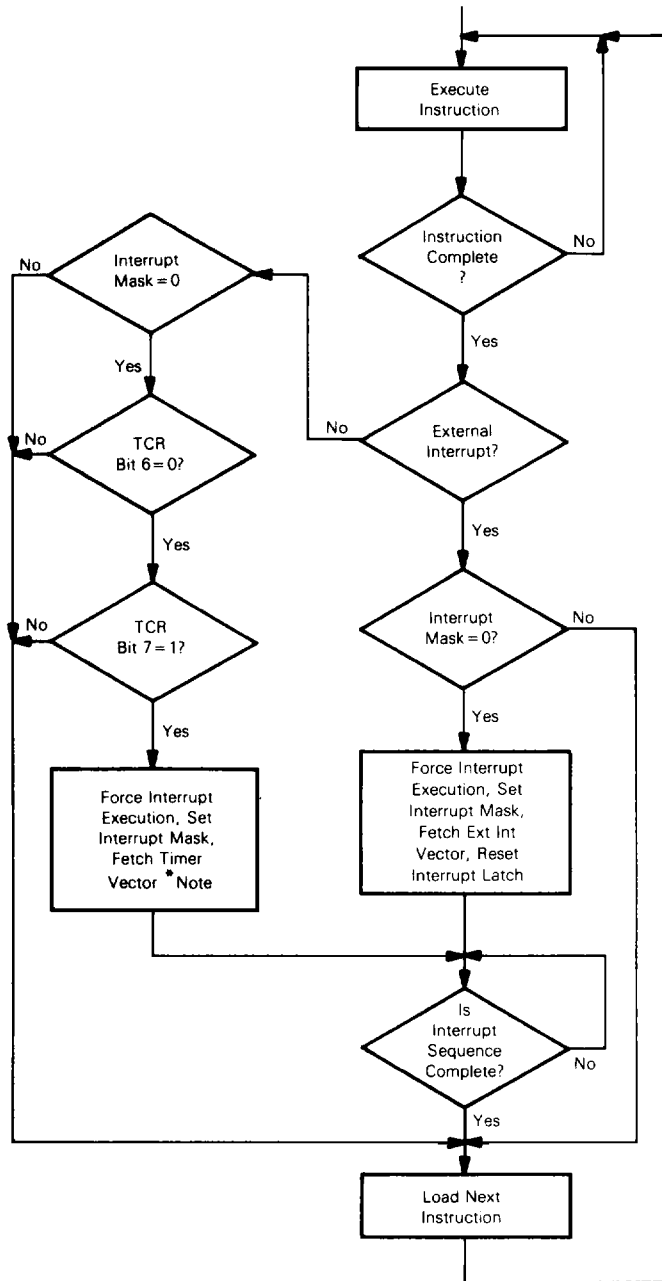
External Interrupt – If the interrupt mask bit of the condition code register is cleared and the external interrupt pin $\overline{\text{IRQ}}$ is "low", then the external interrupt occurs. The action of the external interrupt is identical to the timer interrupt with the exception that the service routine address is specified by the contents of \$1FFA and \$1FFB (\$FFA and \$FFB). The interrupt logic recognizes both a "wire ORed" level and pulses on the external interrupt line. Figure 16 shows both a functional diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the $\overline{\text{IRQ}}$ remains low, then the next interrupt is recognized. The second method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{ILIL}) is obtained by adding 20 instruction cycles (one cycle $t_{\text{Cyc}} = 5/f_{\text{OSC}}$) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 6.

Software Interrupt (SWI) – The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations \$1FFC and \$1FFD (\$FFC and \$FFD). See Figure 15 for interrupt and instruction Processing Flowchart.

The following three functions are not strictly interrupts; however, they are tied very closely to the interrupts. These functions are RESET, STOP, WAIT.

RESET – The $\overline{\text{RESET}}$ input pin and the internal Power On Reset function each cause the program to vector to an initialization program. This vector is specified by the contents of memory locations \$1FFE and \$1FFF (\$FFE and \$FFF). The interrupt mask of the condition code register is also set. Refer to RESET section for details.

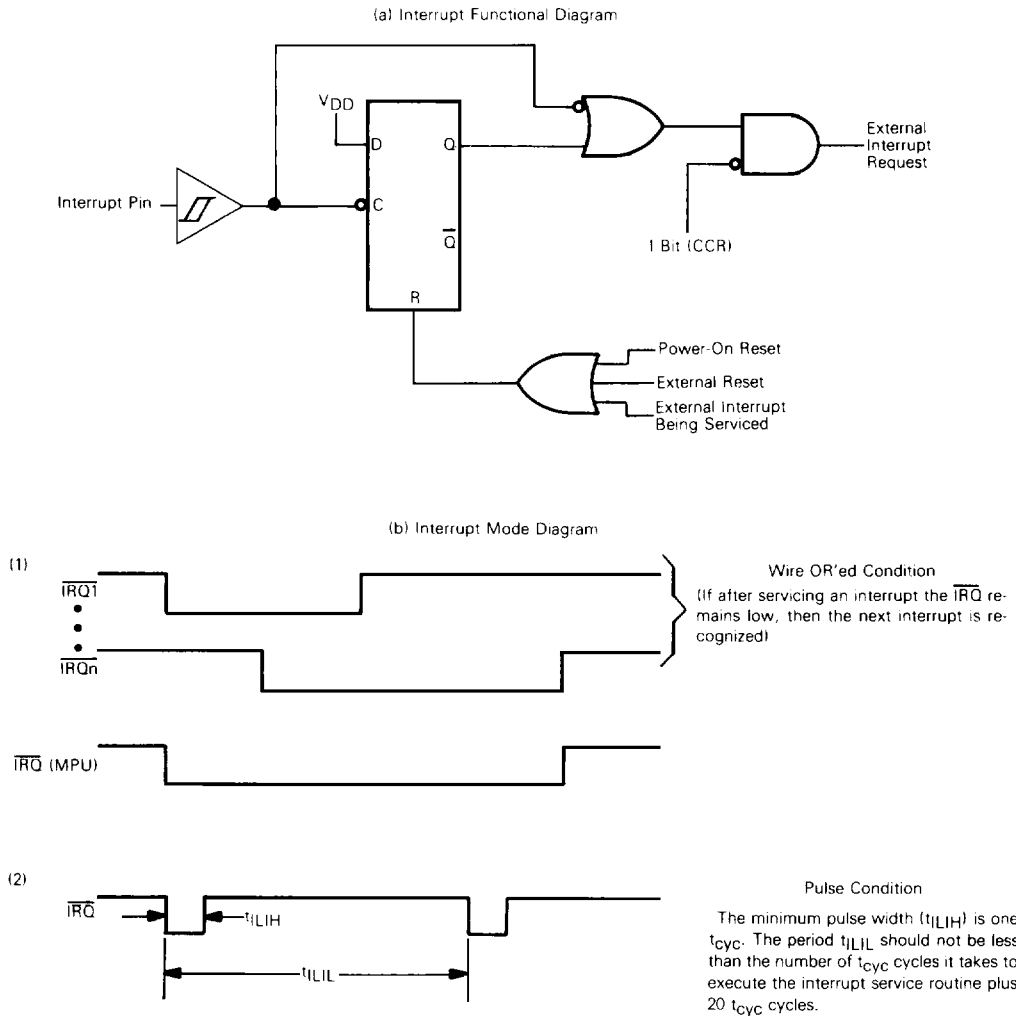
*Any current instruction including SWI



*NOTE: The clear of TCR bit 7 must be accomplished with software.

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Fig. 15 - Interrupt and instruction processing flowchart.



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Fig. 16 - External interrupt.

STOP - The STOP instruction places the CDP6805E2 in a low power consumption mode. In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted; refer to Figure 17. The DS and AS lines go to a low state and the R/W line goes to a high state. The multiplexed address/data bus goes to the data input state. The high order address lines remain at the address of the next instruction. The MPU remains in the STOP mode until an external interrupt or reset occurs; refer to Figure 8 and 17.

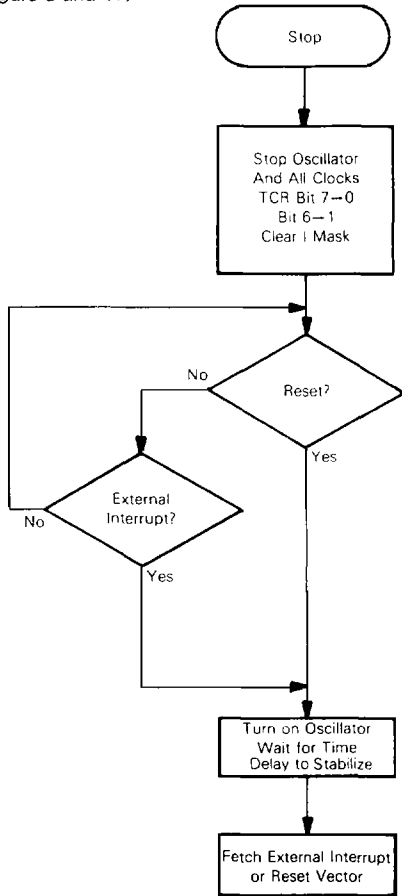


Fig. 17 - Stop function flowchart

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered. All I/O lines remain unchanged.

WAIT - The WAIT instruction places the CDP6805E2 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode; refer to Table 1. In the WAIT function, the internal clock is disabled from all internal circuitry except the Timer circuit, refer to Figure 18. Thus, all internal processing is halted

except the Timer, which is allowed to count in a normal sequence. The R/W line goes to a high state, the multiplexed address/data bus goes to the data input state, and the DS and AS lines go to the low state. The high order address lines remain at the address of the next instruction. The MPU remains in this state until an external interrupt, timer interrupt, or a reset occurs; refer to Figures 7 and 18.

During the WAIT mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled to allow a periodic exit from the WAIT mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode.

Timer

The MPU timer contains a single 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the Timer Control Register (TCR) is set. Then if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I-bit in the Condition Code Register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer vector address from locations \$1FF8 and \$1FF9 (\$FFF8 and \$FFF9) in order to begin servicing the interrupt, unless it was in locations \$1FF6 and \$1FF7 (\$FFF6 and \$FFF7) the WAIT mode.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read. The timer interrupt request bit remains set until cleared by the software. If this happens before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR = 1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler; however, its contents are cleared to all "0's" by the write operation into TCR when bit 3 of the written data equals 1, which allows for truncation free counting.

The Timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the Timer Control Register section.

Timer Input Mode 1 - If TCR4 and TCR5 are both programmed to a "0", the input to the Timer is from an internal clock and the Timer input is disabled. The internal clock mode can be used for periodic interrupt generation, as well

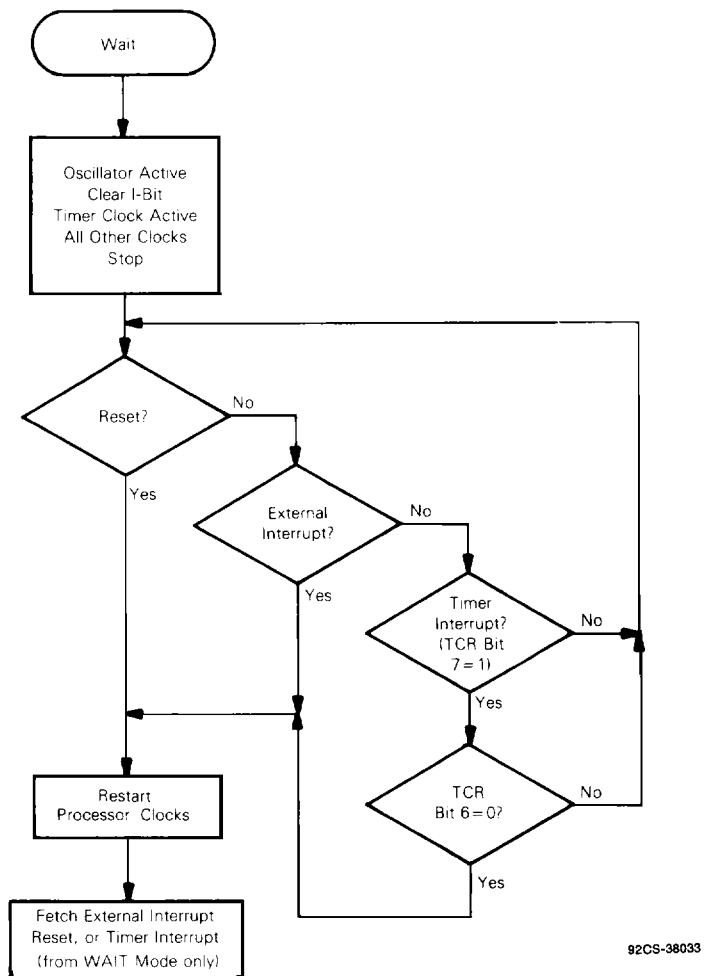


Fig. 18 - Wait function flowchart.

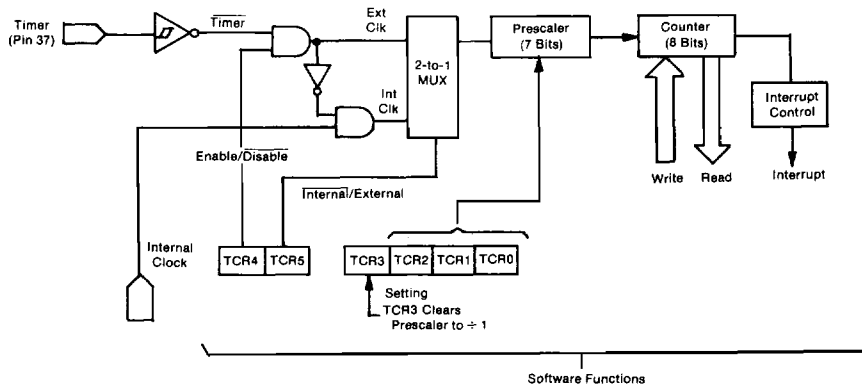
as a reference in frequency and event measurement. The internal clock is the instruction cycle clock and is coincident with Address Strobe (AS) except during a WAIT instruction. During a WAIT instruction the AS pin goes to a low state but the internal clock to the Timer continues to run at its normal rate.

Timer Input Mode 2 – With TCR4=1 and TCR5=0, the internal clock and the TIMER input pin are ANDed together to form the Timer input signal. This mode can be used to measure external pulse widths. The external pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is ± 1 clock and therefore accuracy improves with longer input pulse widths.

Timer Input Mode 3 – If TCR4=0 and TCR5=1, then all inputs to the Timer are disabled.

Timer Input Mode 4 – If TCR4=1 and TCR5=1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The external Timer pin can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts.

Figure 19 shows a block diagram of the Timer subsystem. Power-on Reset and the STOP instruction cause the counter to be set to \$F0.



- NOTES:
1. Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input.
 2. Counter is written to during Data Strobe (DS) and counts down continuously.

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Fig. 19 - Timer block diagram.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits.

TCR7 - Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic "1".

- 1 - Set whenever the counter decrements to zero, or under program control.
- 0 - Cleared on external reset, power-on reset, STOP instruction, or program control.

TCR6 - Timer interrupt mask bit: when this bit is a logic "1" it inhibits the timer interrupt to the processor.

- 1 - Set on external reset, power-on reset, STOP instruction, or program control.
- 0 - Cleared under program control.

TCR5 - External or internal bit: selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by RESET.)

- 1 - Select external clock source.
- 0 - Select internal clock source (AS).

TCR4 - External enable bit: control bit used to enable the external timer pin. (Unaffected by RESET.)

- 1 - Enable external timer pin.
- 0 - Disable external timer pin.

TCR5	TCR4	
0	0	Internal clock (AS) to Timer
0	1	AND of internal clock (AS) and TIMER pin to Timer
1	0	Inputs to Timer disabled
1	1	TIMER pin to Timer

Refer to Figure 19 for Logic Representation.

TCR3 - Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates a "0." (Unaffected by RESET.)

TCR2, TCR1, TCR0 - Prescaler address bits: decoded to select one of eight taps on the prescaler. (Unaffected by RESET.)

Prescaler			
TCR2	TCR1	TCR0	Result
0	0	0	+1
0	0	1	+2
0	1	0	+4
0	1	1	+8
1	0	0	+16
1	0	1	+32
1	1	0	+64
1	1	1	+128

SYSTEM CONFIGURATION

Figures 20 through 24 show in general terms how the CDP6805E2 bus structure may be utilized. Specified interface details vary with the various peripheral and memory devices employed.

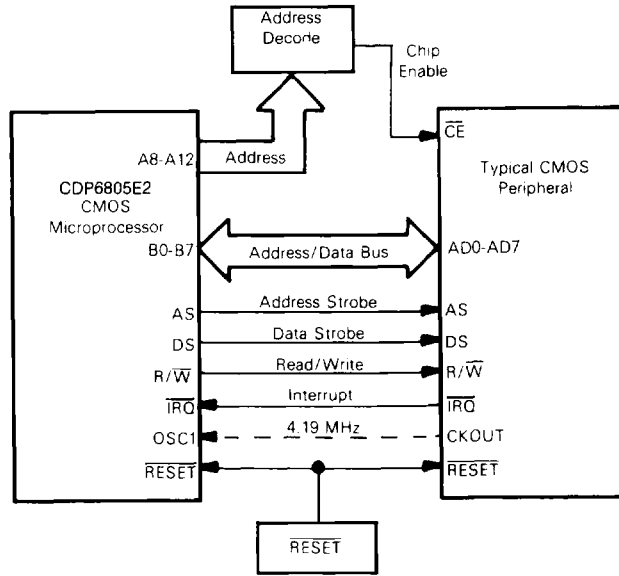


Fig. 20 - Connection to CMOS peripherals.

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

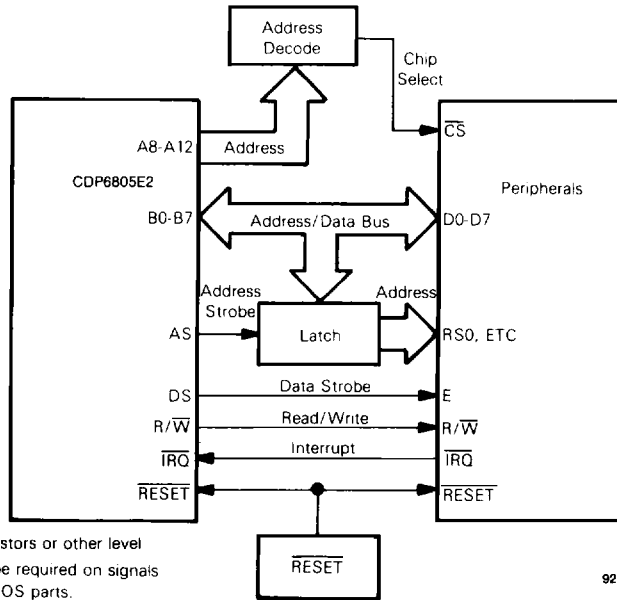


Fig. 21 - Connection to peripherals.

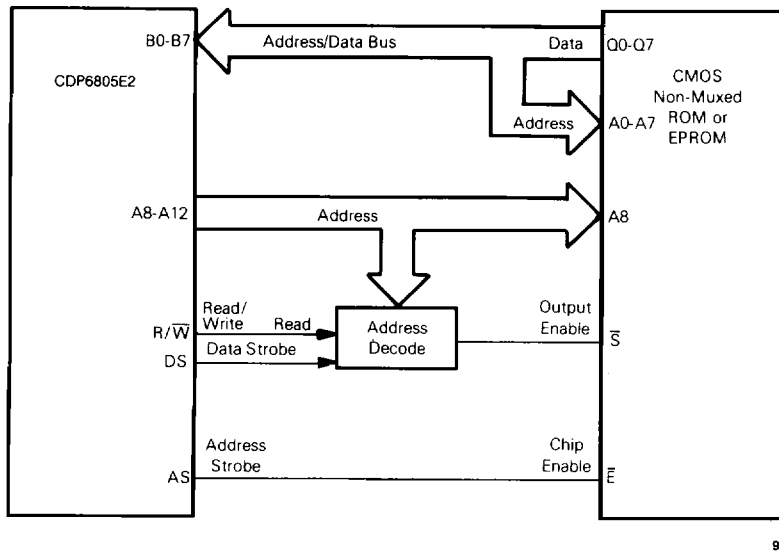
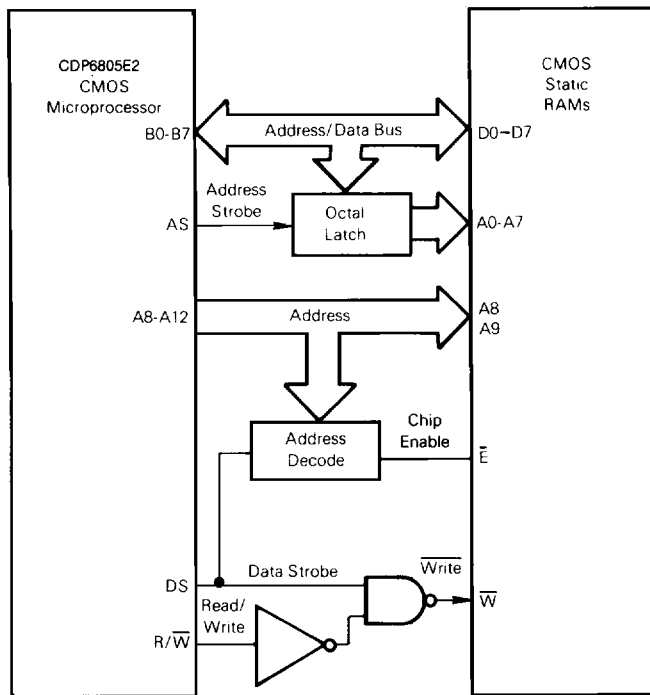
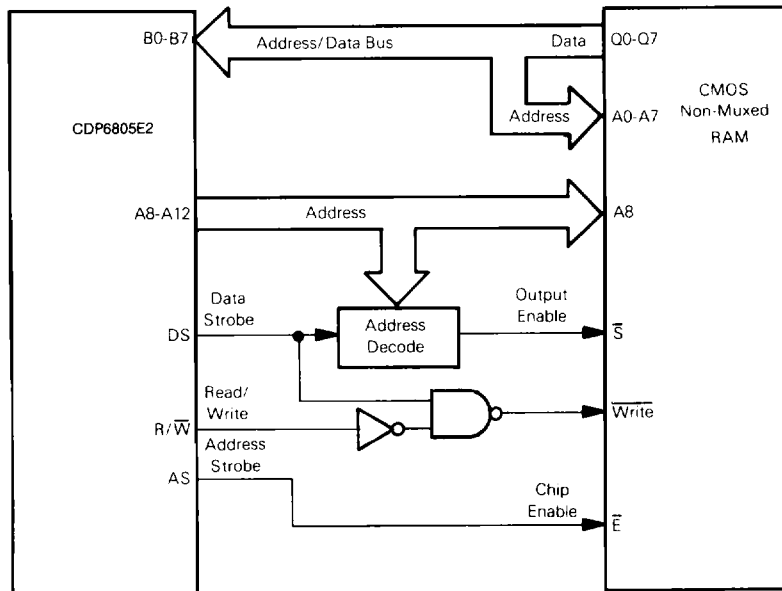


Fig. 22 - Connection to latch non-multiplexed CMOS ROM or EPROM.



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Fig. 23 - Connection to static CMOS RAMs.



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Fig. 24 - Connection to latched non-multiplexed CMOS RAM.

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

Table 4 provides a detailed description of the information present on the Bus, the Read/Write (R/W) pin and the Load Instruction (LI) pin during each cycle for each instruction. This information is useful in comparing actual with ex-

pected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction.

TABLE 4 – SUMMARY OF CYCLE BY CYCLE OPERATION

Address Mode Instructions	Cycles	Cycle #	Address Bus	R/W Pin	LI Pin	Data Bus
Inherent						
LSR LSL ASR NEG CLR ROL COM ROR DEC INC TST	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next instruction
		3	Op Code Address + 1	1	0	Op Code Next instruction
TAX CLC SEC STOP CLI SEI RSP WAIT NOP TXA	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next instruction
RTS	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Stack Pointer	1	0	Irrelevant Data
		4	Stack Pointer + 1	1	0	Irrelevant Data
		5	Stack Pointer + 2	1	0	Irrelevant Data
		6	New Op Code Address	1	0	New Op Code
SWI	10	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Stack Pointer	0	0	Return Address (LO Byte)
		4	Stack Pointer - 1	0	0	Return Address (HI Byte)
		5	Stack Pointer - 2	0	0	Contents of Index Register
		6	Stack Pointer - 3	0	0	Contents of Accumulator
		7	Stack Pointer - 4	0	0	Contents of CC Register
		8	Vector Address 1FFC (FFFC) (Hex)	1	0	Address of Int. Routine (HI Byte)
		9	Vector Address 1FFD (FFFD) (Hex)	1	0	Address of Int. Routine (LO Byte)
		10	Interrupt Routine Starting Address	1	0	Interrupt Routine First Opcode
RTI	9	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Stack Pointer	1	0	Irrelevant Data
		4	Stack Pointer + 1	1	0	Irrelevant Data
		5	Stack Pointer + 2	1	0	Irrelevant Data
		6	Stack Pointer + 3	1	0	Irrelevant Data
		7	Stack Pointer + 4	1	0	Irrelevant Data
		8	Stack Pointer + 5	1	0	Irrelevant Data
		9	New Op Code Address	1	0	New Op Code
Immediate						
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMB SUB	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Operand Data
Bit Set/Clear						
BSET n BCLR n	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Address of Operand	1	0	Operand Data
		5	Address of Operand	0	0	Manipulated Data
Bit Test and Branch						
BRSET n BRCLR n	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Op Code Address + 2	1	0	Branch Offset
		5	Op Code Address + 2	1	0	Branch Offset
Relative						
BCC BHI BNE BEQ BCS BPL BHCC BLS BIL BMC BRN BHCS BIH BMI BMS BRA	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Branch Offset
		3	Op Code Address + 1	1	0	Branch Offset
BSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Branch Offset
		3	Op Code Address + 1	1	0	Branch Offset
		4	Subroutine Starting Address	1	0	First Subroutine Op Code
		5	Stack Pointer	0	0	Return Address (LO Byte)
		6	Stack Pointer - 1	0	0	Return Address (HI Byte)

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

TABLE 4 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/W Pin	LI Pin	Data Bus
Direct						
JMP	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Jump Address
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
TST	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Op Code Address + 2	1	0	Op Code Next Instruction
STA STX	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Op Code Address + 1	1	0	Address of Operand
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	4	Address of Operand	0	0	Operand Data
		1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Operand Address	1	0	Current Operand Data
		4	Operand Address	1	0	Current Operand Data
JSR	5	5	Operand Address	0	0	New Operand Data
		1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Subroutine Address (LO Byte)
		3	Subroutine Starting Address	1	0	1st Subroutine Op Code
		4	Stack Pointer	0	0	Return Address (LO Byte)
5	Stack Pointer - 1	0	0	Return Address (HI Byte)		
Extended						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Jump Address (HI Byte)
		3	Op Code Address + 2	1	0	Jump Address (LO Byte)
ADC BIT ORA ADD CMP LDX AND EOR SBC CPX LDA SUB	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address Operand (HI Byte)
		3	Op Code Address + 2	1	0	Address Operand (LO Byte)
		4	Address of Operand	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand (HI Byte)
		3	Op Code Address + 2	1	0	Address of Operand (LO Byte)
		4	Op Code Address + 2	1	0	Address of Operand (LO Byte)
		5	Address of Operand	0	0	Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Subroutine (HI Byte)
		3	Op Code Address + 2	1	0	Address of Subroutine (LO Byte)
		4	Subroutine Starting Address	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address (LO Byte)
		6	Stack Pointer - 1	0	0	Return Address (HI Byte)
Indexed, No-Offset						
JMP	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Operand Data
TST	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Operand Data
		4	Op Code Address + 1	1	0	Op Code Next Instruction
STA STX	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Op Code Address + 1	1	0	Op Code Next Instruction
		4	Index Register	0	0	Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Current Operand Data
		4	Index Register	1	0	Current Operand Data
		5	Index Register	0	0	New Operand Data
JSR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	1st Subroutine Op Code
		4	Stack Pointer	0	0	Return Address (LO Byte)
		5	Stack Pointer - 1	0	0	Return Address (HI Byte)

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**MICRO-
PROCESSORS**

CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

TABLE 4 – SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/W Pin	LI Pin	Data Bus
Indexed 8-Bit Offset						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
ADC EOR CPX ADD LDA LDX AND ORA CMP SUB BIT SBC	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Op Code Address + 1	1	0	Offset
		5	Index Register + Offset	0	0	Operand Data
TST	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
		5	Op Code Address + 2	1	0	Op Code Next Instruction
LSL LSR ASR NEG CLR ROL COM ROR DEC INC	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Current Operand Data
		5	Index Register + Offset	1	0	Current Operand Data
		6	Index Register + Offset	0	0	New Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address LO Byte
		6	Stack Pointer - 1	0	0	Return Address HI Byte
Indexed, 16-Bit Offset						
JMP	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
ADC CMP SUB ADD EOR SBC AND ORA CPX LDA BIT LDX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	Operand Data
STA STX	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Op Code Address + 2	1	0	Offset (LO Byte)
		6	Index Register + Offset	0	0	Operand Data
JSR	7	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	1st Subroutine Op Code
		6	Stack Pointer	0	0	Return Address (LO Byte)
		7	Stack Pointer - 1	0	0	Return Address (HI Byte)

TABLE 4 – SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Instructions	Cycles	Cycles #	Address Bus	RESET Pin	R/W Pin	LI Pin	Data Bus
Other Functions							
Hardware $\overline{\text{RESET}}$	5	1	\$1FFE (\$FFFE)	0	1	0	Irrelevant Data
		2	\$1FFE (\$FFFE)	0	1	0	Irrelevant Data
		3	\$1FFE (\$FFFE)	1	1	0	Irrelevant Data
		4	\$1FFE (\$FFFE)	1	1	0	Vector High
		5	\$1FFF (\$FFFF)	1	1	0	Vector Low
		5	Reset Vector	1	1	0	Op Code
Power on Reset	1922	1	\$1FFE (\$FFFE)	1	1	0	Irrelevant Data
		•	•	•	•	•	•
		•	•	•	•	•	•
		•	•	•	•	•	•
		1919	\$1FFE (\$FFFE)	1	1	0	Irrelevant Data
		1920	\$1FFE (\$FFFE)	1	1	0	Vector High
1921	\$1FFF (\$FFFF)	1	1	0	Vector Low		
1922	Reset Vector	1	1	0	Op Code		
Instruction							
Instruction	Cycles	Cycles #	Address Bus	$\overline{\text{IRQ}}$ Pin	R/W Pin	LI Pin	Data Bus
$\overline{\text{IRQ}}$ Interrupt (Timer Vector \$1FFB, \$1FF9)	10		Last Cycle of Previous Instruction	0	X	0	X
		1	Next Op Code Address	0	1	0	Irrelevant Data
		2	Next Op Code Address	X	1	0	Irrelevant Data
		3	SP	X	0	0	Return Address (LO Byte)
		4	SP - 1	X	0	0	Return Address (HI Byte)
		5	SP - 2	X	0	0	Contents Index Reg
		6	SP - 3	X	0	0	Contents Accumulator
		7	SP - 4	X	0	0	Contents CC Register
		8	\$1FFA (\$FFFA)	X	1	0	Vector High
		9	\$1FFB (\$FFFB)	X	1	0	Vector Low
		10	$\overline{\text{IRQ}}$ Vector	X	1	0	Int Routine First

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MICRO-PROCESSORS