Bitec

DSP Solutions For Industry & Research

Product Brief : DisplayPort IP Core for Lattice

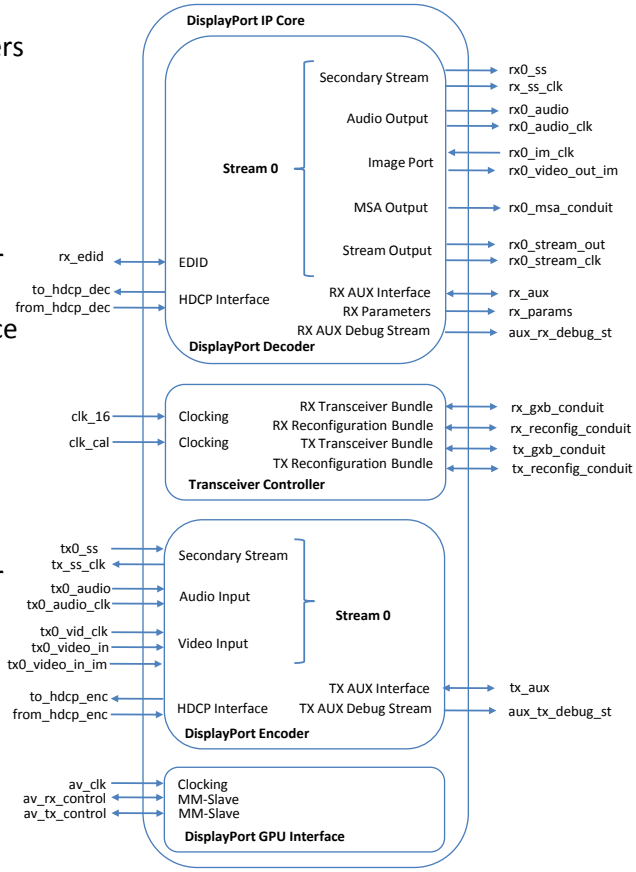
DisplayPort heralds a new alternative in video connectivity. Designed to enable low cost direct drive monitors and backed by industry leaders (DELL, Apple etc) DisplayPort is not hindered by license and royalty fees.

The Bitec DisplayPort IP core for Lattice FPGA devices offers a cost-efficient alternative to ASICs and enables DTV manufacturers to rapidly develop and deliver displays offering a superior viewing experience within ever-shrinking product lifecycles.

The Bitec DP IP core accepts 1,2 or 4 lane at either 1.62 or 2.7GB/s link rate. In accordance with the DP specification 1.4, the core will adapt and train to the transmitting source capability via a firmware driven policy maker API.

The source and sink cores accept v/h/d-sync and parallel RGB data. Audio data and raw Auxiliary data ports to the cores provide flexible side-band messaging.

Bitec also offer a tailoring service for bespoke designs. For more information contact Bitec.



Features

- Support for 1,2 & 4-lane
- Support DisplayPort 1.4
- Support 1.62 or 2.7Gbps link rate
- Dual/quad symbol modes
- Single/dual/quad pixel modes
- 4,8,10,12 & 16 bit color support
- Supports RGB, YCbCr Colorimetric Formats
- Autonomous AUX channel or GPU driven
- AUX debug channel
- Optional HDCP Support
- 8-Channel Audio
- eDP Features supported

Contact info@bitec-dsp.com for more information

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