19-6052; Rev 1; 8/12

EVALUATION KIT AVAILABLE

MAX14760/MAX14762/MAX14764

Above- and Below-the-Rails Low-Leakage Analog Switches

General Description

The MAX14760/MAX14762/MAX14764 analog switches are capable of passing bipolar signals that are beyond their supply rails. These devices operate from a single +3.0V to +5.5V supply, and support signals in the -25V to +25V range.

The MAX14760 is a single-pole/single-throw (SPST) analog switch, while the MAX14762 is a dual-SPST analog switch. The MAX14764 is a single-pole/double-throw (SPDT) analog switch.

The MAX14760/MAX14762/MAX14764 feature 20Ω (max) on-resistance with a ±10nA (max) on-leakage current for MAX14760/MAX14762.

The MAX14760/MAX14764 are available in 8-pin (3mm x 3mm) TDFN packages. The MAX14762 is available in a 10-pin (3mm x 3mm) TDFN package. These devices are specified over the -40°C to +85°C extended operating temperature range.

***Ordering Information/Selector Guide* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX14760.related.

Benefits and Features

- **Simplify Power-Supply Requirements**
  - **3.0V to 5.5V Supply Range**
  - **-25V to +25V Signal Range**
- **High Performance**
  - **±10nA (max) On-Leakage Current (MAX14760/MAX14762)**
  - **20Ω (max) On-Resistance**
  - **Low On-Resistance Flatness, 58mΩ (typ)**
  - **Thermal Shutdown Protection**
  - **-40°C to +85°C Operating Temperature Range**
  - **High Bandwidth:115MHz (typ)**
- **Save Space on Board**
  - **Small 8-Pin and 10-Pin TDFN Packages**

Applications

Industrial Measurement Systems

Instrumentation Systems

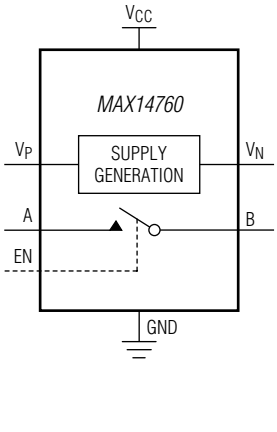
Opto-Relay Replacement

Medical Systems

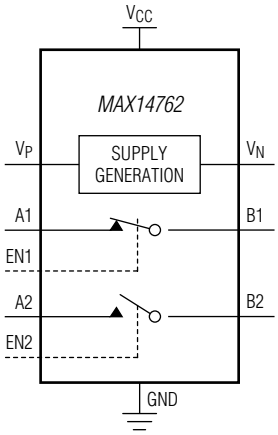
ATE Systems

Audio Signal Routing and Switching

Functional Diagrams/Truth Tables

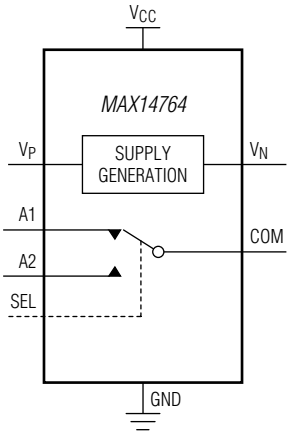


EN	A
0	OPEN
1	CLOSED



EN1	A1
0	CLOSED
1	OPEN

EN2	A2
0	OPEN
1	CLOSED



SEL	A1	A2
0	CLOSED	OPEN
1	OPEN	CLOSED

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

V_{CC} ..... -0.3V to +6V
EN, EN1, EN2, SEL ..... -0.3V to +(V_{CC} + 0.3V)
A, A1, A2, B, B1, B2, COM ..... (V_N - 0.3V) to Lesser of (V_P + 0.3V) or (V_N + 52V)
V_P ..... -0.3V to Lesser of (+52V) or (V_N + 70V)
V_N ..... Greater of (V_{CC} - 40V) or (V_P - 70V) to +0.3V
V_P to V_N ..... -0.3V to 70V
Continuous Current ..... ±25mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN Package (derate 24.4mW/°C above +70°C) 1951.2mW
10-Pin TDFN Package (derate 24.4mW/°C above +70°C) 1951.2mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

8 TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 8°C/W

10 TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 9°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Power Supply Range	V_{CC}			3.0		5.5	V
Continuous Current Through Switch	I_A			-25		+25	mA
Supply Current	I_{CC}	$V_{CC} \le 4.7V$	$V_{EN\_} = V_{CC}$		4.1	10	mA
			$V_{EN\_} = V_{CC}/2$		4.1	10	
		$V_{CC} > 4.7V$	$V_{EN\_} = V_{CC}$		2.5	6	
			$V_{EN\_} = V_{CC}/2$		2.5	6	
Analog Signal Range	V_{COM}, $V_{A\_}$, $V_{B\_}$	Switch open or closed		-25		+25	V
On-Resistance	R_{ON}	I_{COM} or $I_{B\_}$ = ±25mA, $V_{A\_}$ = ±25V			8	20	Ω
On-Resistance Flatness	ΔR_{ON}	-25V < $V_{A\_}$ < +25V, I_{COM} or $I_{B\_}$ = ±25mA			58		mΩ
A, A1, A2 Off-Leakage Current	$I_{A\_(OFF)}$	$V_{A\_}$ = +25V, V_{COM} or $V_{B\_}$ = 0V, Figure 1		-30		+30	nA
COM, B, B1, B2 Off-Leakage Current	$I_{COM(OFF)}$, $I_{B\_(OFF)}$	V_{COM} or $V_{B\_}$ = 15V, $V_{A\_}$ = 0V, Figure 1 (MAX14764)		-10		+10	nA
		$V_{B\_}$ = 15V, $V_{A\_}$ = 0V, Figure 1 (MAX14760/MAX14762)		-10		+10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Leakage Current	I_{ON}	$V_{A\_}$ = ±25V, B/COM is unconnected, Figure 1 (MAX14760/MAX14762)	-10		+10	nA
		$V_{A\_}$ = ±25V, B/COM is unconnected, Figure 1 (MAX14764)	-30		+30	
DIGITAL LOGIC						
Input-Voltage Logic-Low	V_{IL}	V_{CC} = 3.0V			0.7	V
		V_{CC} = 3.6V			0.7	
		V_{CC} = 4.5V			0.8	
		V_{CC} = 5.5V			0.8	
Input-Voltage Logic-High	V_{IH}	V_{CC} = 3.0V	1.7			V
		V_{CC} = 3.6V	1.9			
		V_{CC} = 4.5V	2.0			
		V_{CC} = 5.5V	2.1			
Input Current	I_L		-1		+1	µA
AC CHARACTERISTICS						
Power-On Time	t_{PWRON}	C_{VP} = C_{VN} = 100nF (Note 3)		50		ms
Enable Turn-On Time	t_{ON}	$V_{A\_}$ = ±10V, R_L = 10kΩ, Figure 2 (MAX14760/MAX14762)		100	200	µs
		$V_{A\_}$ = ±10V, R_L = 10kΩ, Figure 2 (MAX14764)		1.04	1.6	ms
Enable Turn-Off Time	t_{OFF}	(Figure 2)		110	400	µs
Break-Before-Make Interval	t_{BBM}	$V_{A\_}$ = $1V_{RMS}$, R_L = 10kΩ, Figure 3 (MAX14764)		740		µs
Off-Isolation	V_{ISO}	$V_{A\_}$ = $1V_{RMS}$, f = 100kHz, R_L = 50Ω, C_L = 15pF, Figure 4		-77		dB
Crosstalk	V_{CT}	R_S = R_L = 50Ω, f = 100kHz, V_{COM} = $1V_{RMS}$, Figure 5 (MAX14764)		-92		dB
-3dB Bandwidth	BW	R_S = 50Ω, R_L = 1kΩ , $V_{A\_}$ = $1V_{P-P}$, Figure 6		115		MHz
Total Harmonic Distortion	THD+N	R_S = R_L = 1kΩ, f = 20Hz to 20kHz		0.005		%
Charge Injection	Q	$V_{A\_}$ = GND, C_L = 1nF, Figure 7		19		pC
Input Capacitance	C_{IN}	At A, A1, A2, B, B1, B2, and COM pins		32		pF
THERMAL PROTECTION						
Thermal Shutdown Temperature	t_{HYST}			+154		°C
Shutdown Temperature Hysteresis	t_{SHUT}			24		°C
ESD PROTECTION						
All Pins		Human Body Model		±2		kV

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over operating temperature range are guaranteed by design.

Note 3: The power-on time is defined as the settling time for the charge pump's output to reach steady-state value within 1%.

Test Circuits/Timing Diagrams

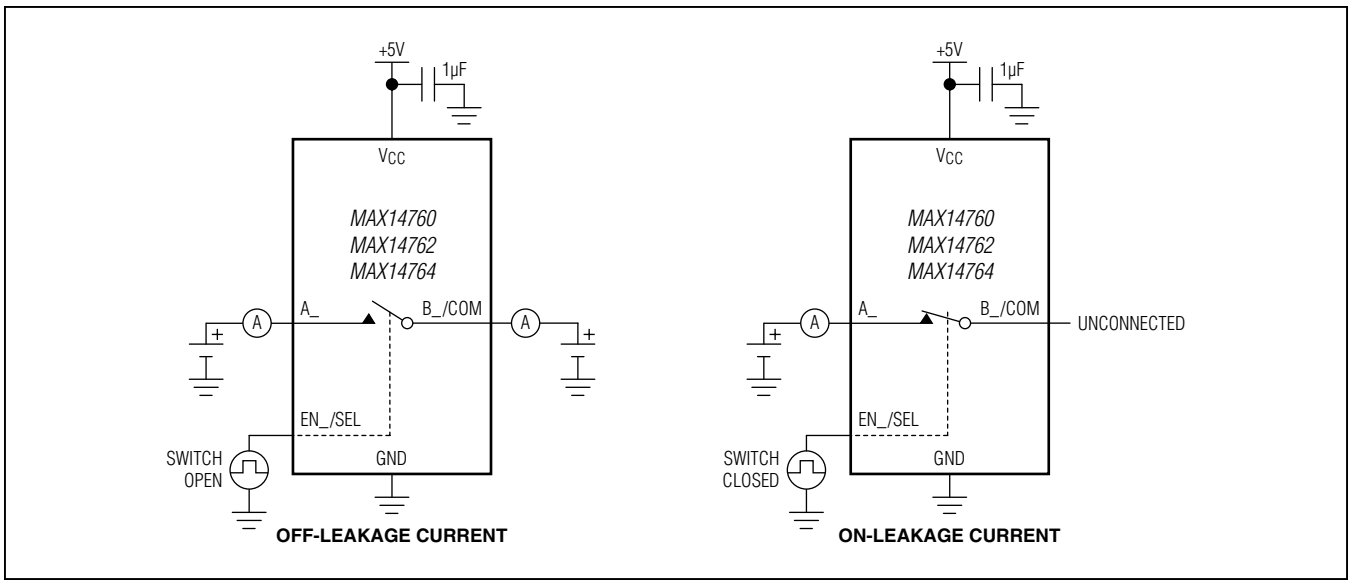


Figure 1. Leakage Current Measurement

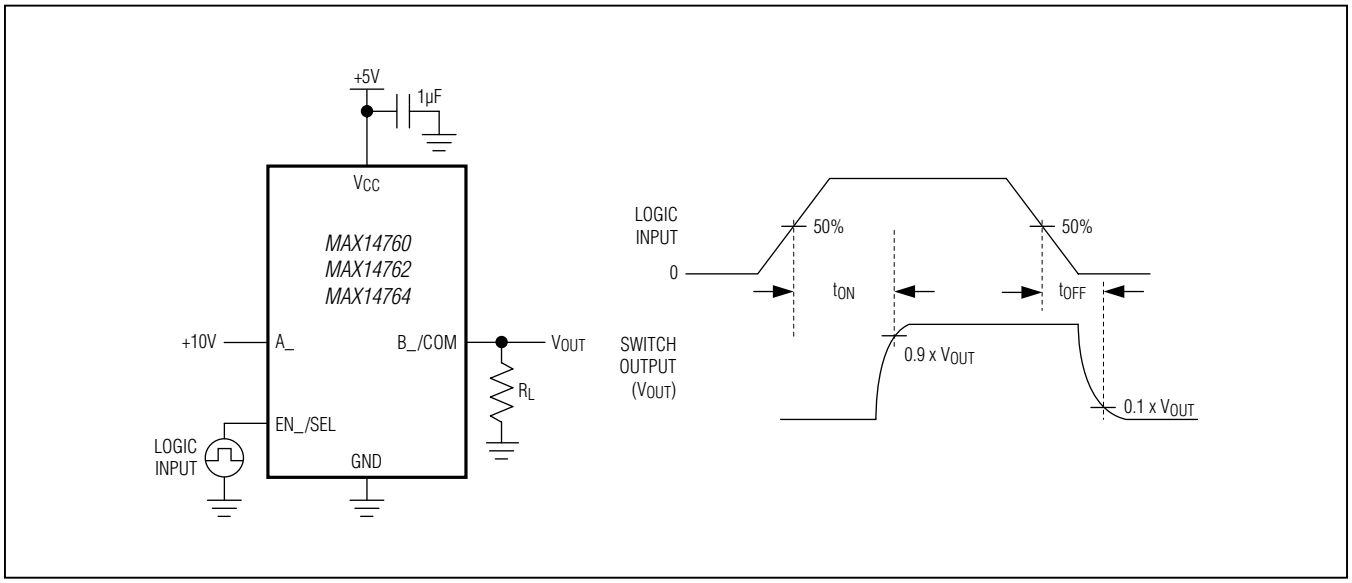


Figure 2. Switching Time

Test Circuits/Timing Diagrams (continued)

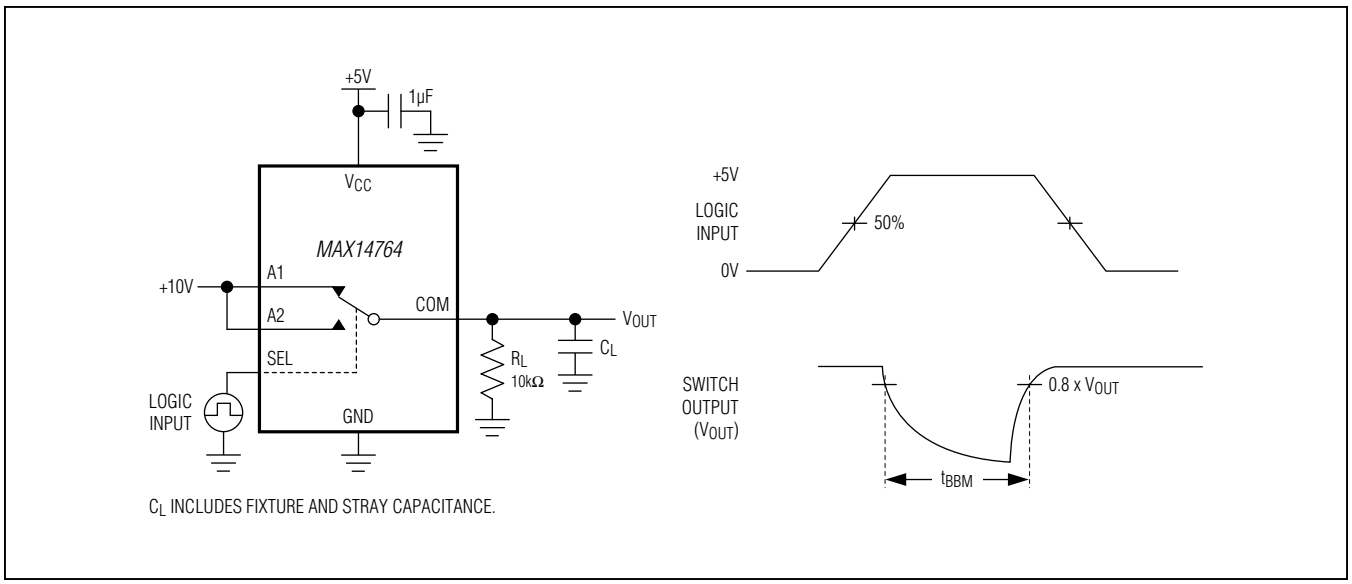


Figure 3. Break-Before-Make

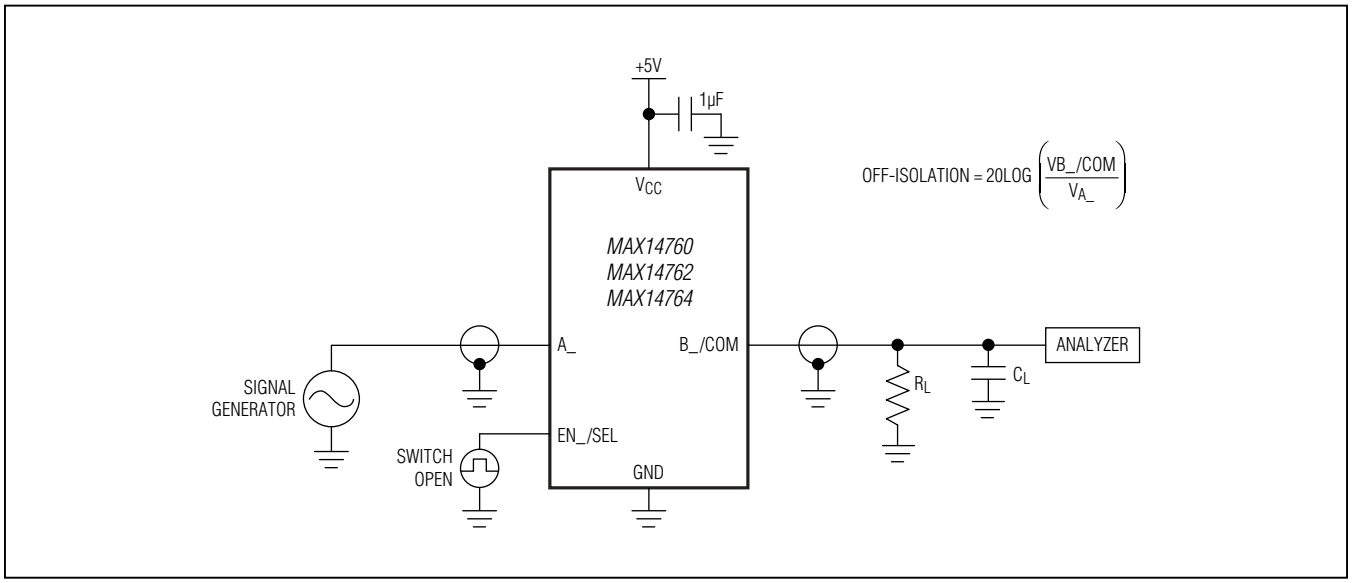


Figure 4. Off-Isolation

Test Circuits/Timing Diagrams (continued)

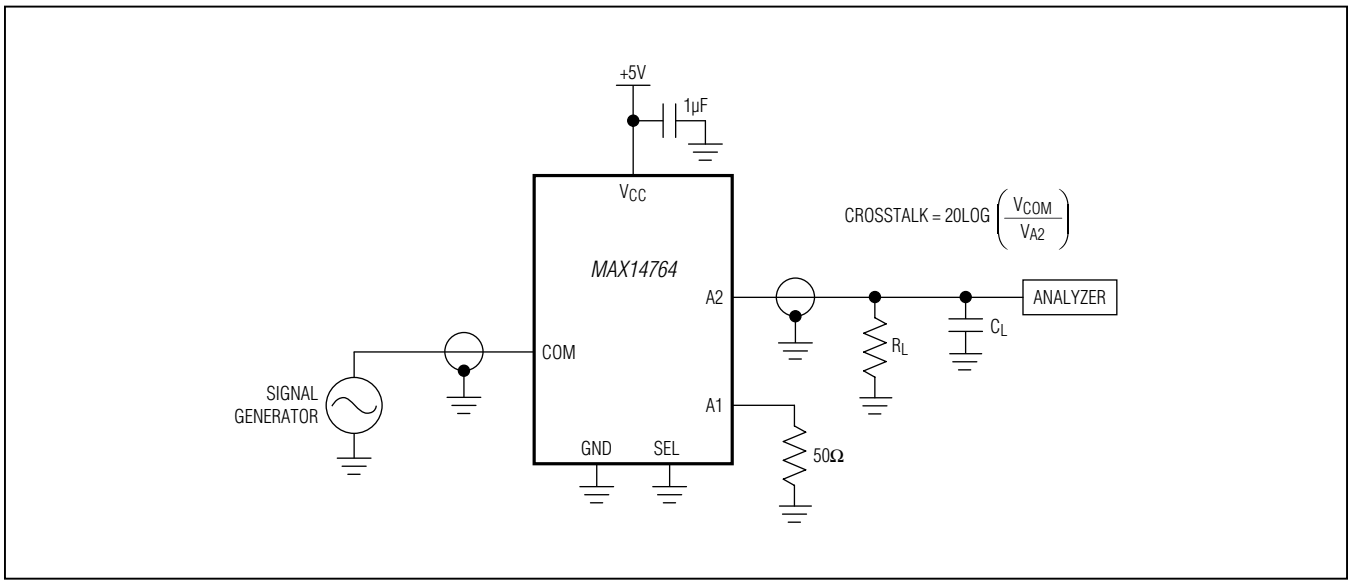


Figure 5. Crosstalk

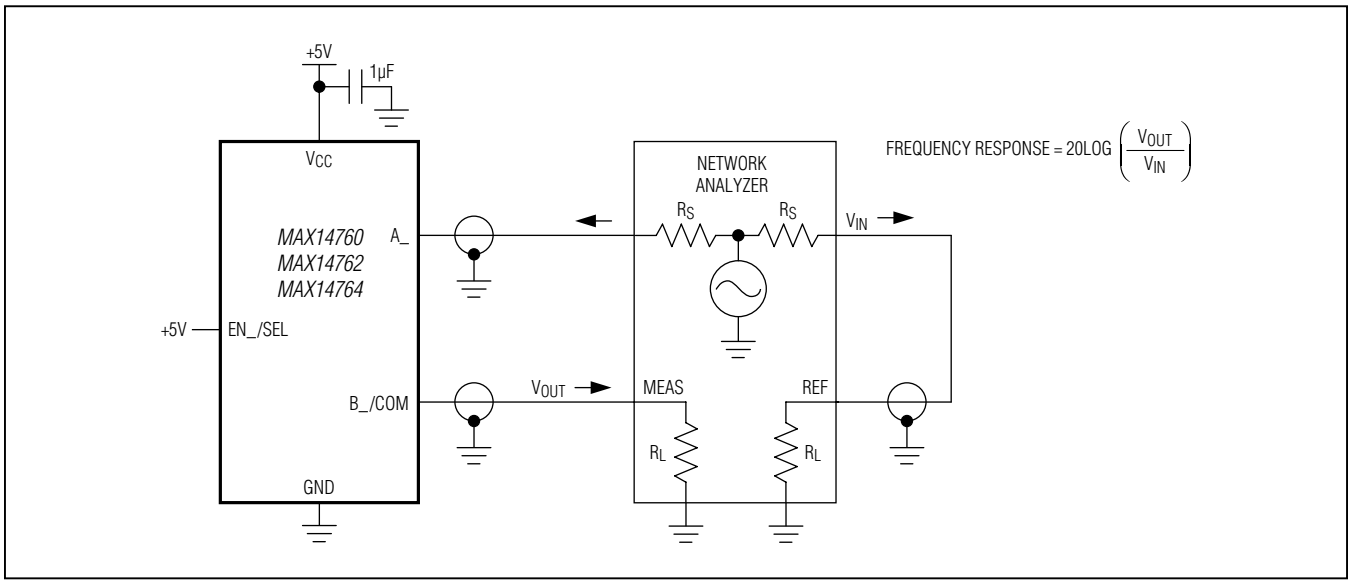


Figure 6. Insertion Loss

Test Circuits/Timing Diagrams (continued)

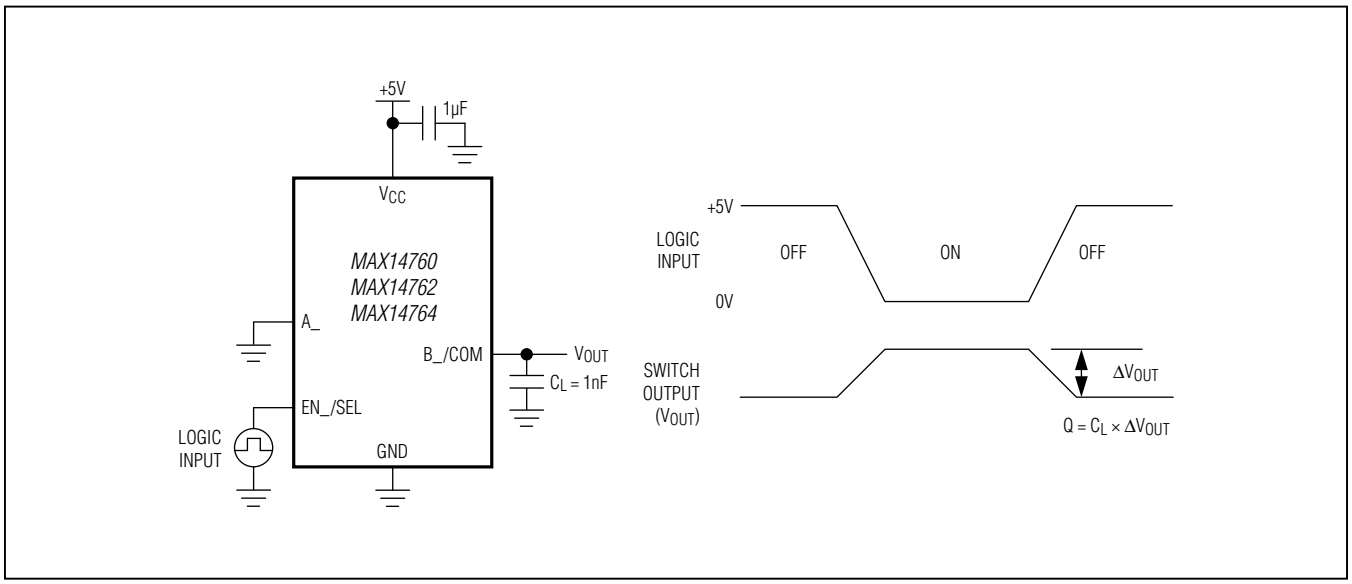
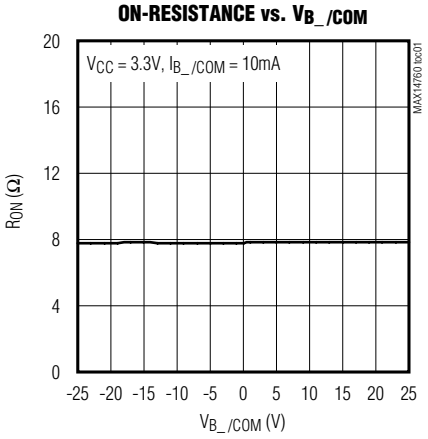
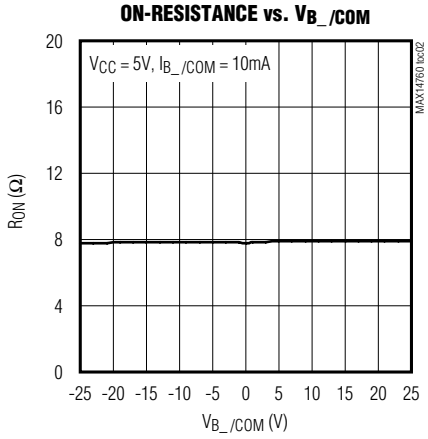


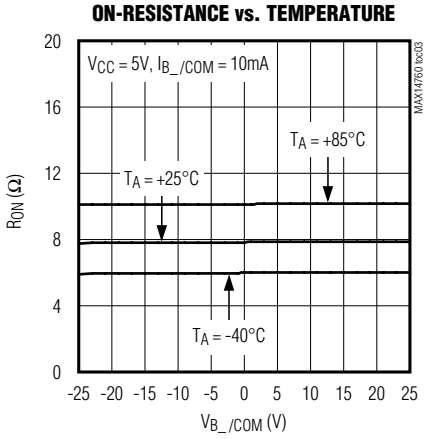
Figure 7. Charge Injection

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



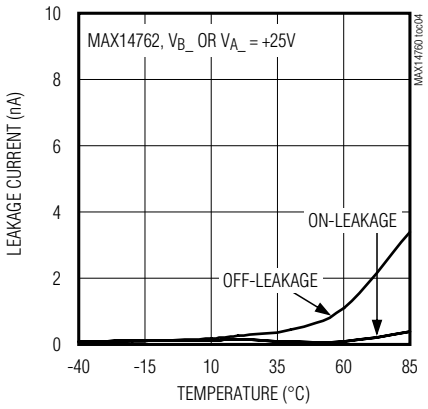




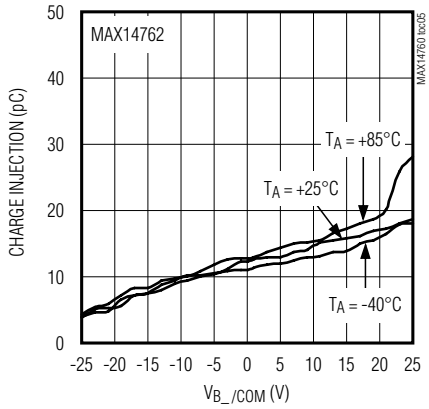
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

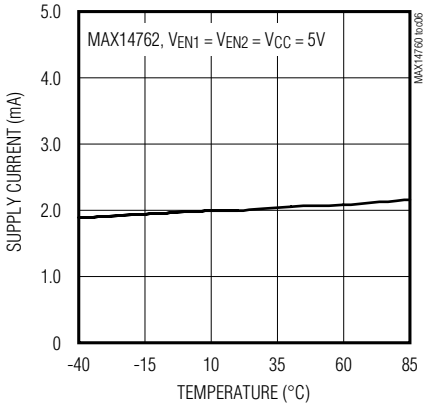
LEAKAGE CURRENT vs. TEMPERATURE



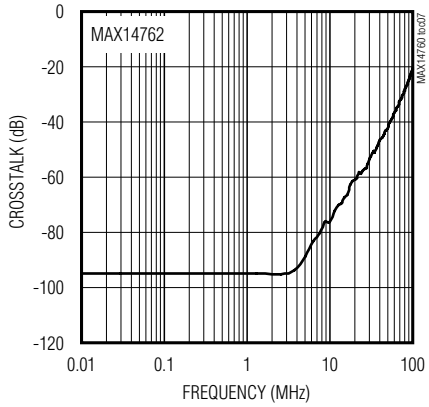
CHARGE INJECTION vs. $V_{B\_/COM}$



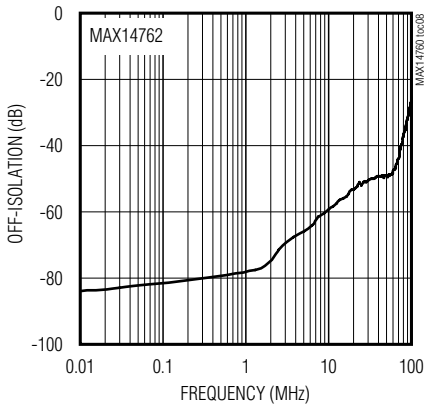
SUPPLY CURRENT vs. TEMPERATURE



CROSSTALK vs. FREQUENCY



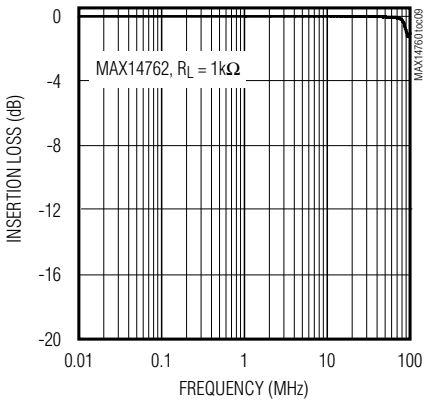
OFF-ISOLATION vs. FREQUENCY



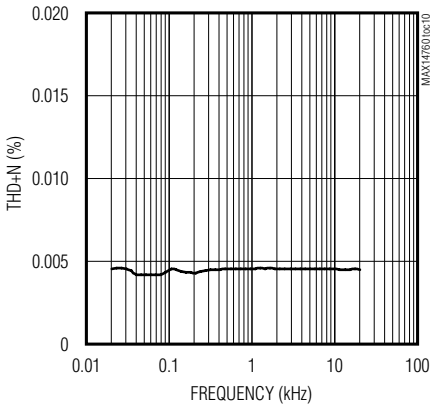
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

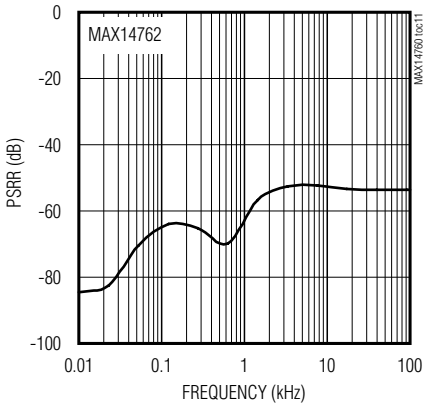
INSERTION LOSS vs. FREQUENCY



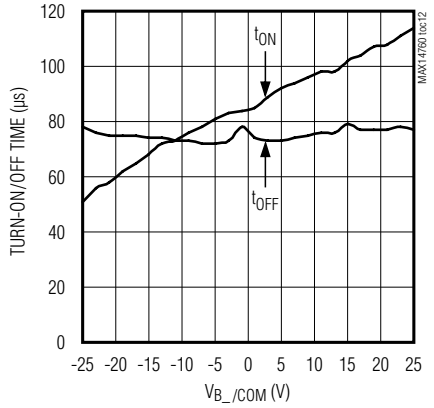
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



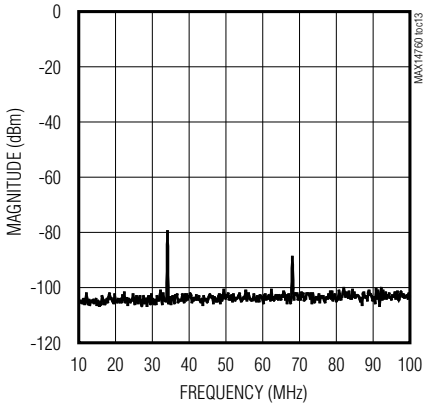
PSRR vs. FREQUENCY



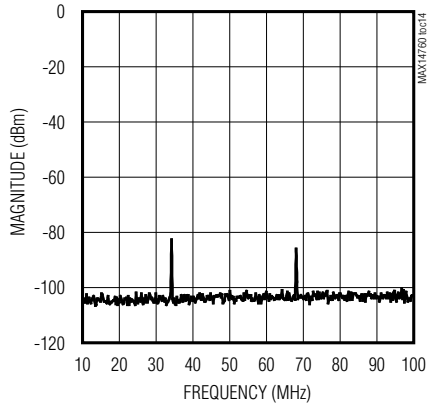
TURN-ON/OFF TIME vs. $V_{B\_/COM}$



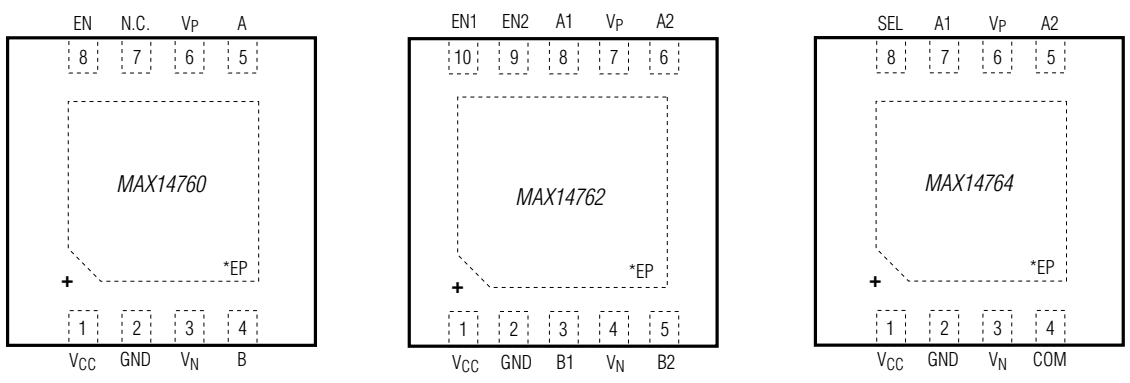
MAX14762 CHARGE PUMP NOISE (SWITCH DISABLED)



MAX14762 CHARGE PUMP NOISE (SWITCH ENABLED)



Pin Configurations



TDFN

*CONNECT EXPOSED PAD (EP) TO V_N.

Pin Description

PIN			NAME	FUNCTION
MAX14760	MAX14762	MAX14764		
1	1	1	V_{CC}	Positive-Supply Voltage Input. Bypass V_{CC} to GND with a 1µF ceramic capacitor placed as close as possible to the device.
2	2	2	GND	Ground
3	4	3	V_N	Negative Voltage Output. Bypass V_N to GND with a 0.1µF 50V ceramic capacitor placed as close as possible to the device.
4	—	—	B	Analog Switch Common Terminal
—	—	4	COM	Analog Switch Common Terminal
5	—	—	A	Analog Switch Normally Open Terminal
6	7	6	V_P	Positive Voltage Output. Bypass V_P to GND with a 0.1µF 50V ceramic capacitor placed as close as possible to the device.
7	—	—	N.C.	No Connection. Leave unconnected.
8	—	—	EN	Switch Control Input. Drive EN high to close the switch or drive EN low to open the switch.
—	8	7	A1	Analog Switch 1 Normally Closed Terminal

Pin Description (continued)

PIN			NAME	FUNCTION
MAX14760	MAX14762	MAX14764		
—	3	—	B1	Analog Switch 1 Common Terminal
—	6	5	A2	Analog Switch 2 Normally Open Terminal
—	5	—	B2	Analog Switch 2 Common Terminal
—	10	—	EN1	Switch 1 Control Input. Drive EN1 high to open switch 1 or drive EN1 low to close switch 1.
—	9	—	EN2	Switch 2 Control Input. Drive EN2 high to close switch 2 or drive EN2 low to open switch 2.
—	—	8	SEL	Switch Control Input. Drive SEL low to connect the COM terminal to A1 or drive SEL high to connect the COM terminal to A2.
—	—	—	EP	Exposed Pad. Connect EP to V_N; EP is not intended as an electrical connection.

Detailed Description

The MAX14760/MAX14762/MAX14764 analog switches are capable of handling signals above and below their rails. These devices operate from a single +3.0V to +5.5V supply and support signals in the -25V to +25V range.

Integrated Bias Generation

The MAX14760/MAX14762/MAX14764 contain a total of three charge pumps to generate bias voltages for the internal switches: a 5V regulated charge pump, a positive high-voltage (+35V) charge pump, and a negative high-voltage (-27V) charge pump. When V_{DD} is above 4.7V (typ), the 5V regulated charge pump is bypassed, and V_{DD} provides the input for the high-voltage charge pumps, reducing overall supply current. An external 0.1µF capacitor is required for each high-voltage charge pump between V_P/V_N and GND.

Analog Signal Range

The devices switch signals in the range from -25V to +25V that are above and below their rails. The on-resistance for these devices exhibits a high degree of flatness (58mΩ) over the whole input voltage range of -25V to +25V. The analog switches allow bidirectional current flow, so A, A1, A2, B, B1, B2, and COM, can be used as either inputs or outputs.

Bypass Capacitors

Bias-stabilizing capacitors are required on the V_P and V_N pins. 1µF ceramic capacitors are suggested for effective operation. V_P and V_N are not intended as a power supply for other circuitry.

Applications Information

Nonpowered Condition

The MAX14760/MAX14762/MAX14764 can tolerate input voltages on the A, B, or COM pins in the ±25V range when it is not powered. When V_{DD} = 0V, the DC input leakage current into the A, B, or COM pins is typically below 1µA. Some devices can have a larger leakage current up to the mA range due to technology spread.

With V_{DD} not powered, internal diodes between the analog pins and the V_P and V_N will charge up the external capacitors on V_P and V_N when positive and/or negative voltages are applied to these pins. This causes transient input current flow.

Large dv/dt on the inputs causes large capacitive charging currents, which have to be limited to 300mA to avoid destroying the internal diodes. Hence, the 100nF capacitors on V_P and V_N, the dv/dt must be limited to 3V/µs. Once the capacitors reach their final voltage the input current decays to the leakage current levels mentioned above.

Above- and Below-the-Rails Low-Leakage Analog Switches

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	FUNCTION	R_{ON} (MAX) (Ω)
MAX14760ETA+	-40°C to +85°C	8 TDFN-EP*	1 x SPST	20
MAX14762ETB+	-40°C to +85°C	10 TDFN-EP*	2 x SPST	20
MAX14764ETA+	-40°C to +85°C	8 TDFN-EP*	1 x SPDT	20

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO
8 TDFN	T833+2	21-0137	90-0059
10 TDFN	T1033+1	21-0137	90-0003

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—
1	8/12	Updated *Electrical Characteristics* table, updated Figures 1–7, added TOCs 13 and 14, updated *Pin Configuration* table, added *Integrated Bias Generation* and *Nonpowered Condition* sections	3–7, 9–11